



MICROCHIP PIC18F87J50 FAMILY

PIC18F87J50 Family Rev. A2 Silicon Errata

The PIC18F87J50 Family Rev. A2 parts you have received conform functionally to the Device Data Sheet (DS39775B), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F87J50 Family will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F87J50 Family devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F65J50	0100 0001 000	0 0010
PIC18F66J50	0100 0001 010	0 0010
PIC18F66J55	0100 0001 011	0 0010
PIC18F67J50	0100 0001 100	0 0010
PIC18F85J50	0100 0001 101	0 0010
PIC18F86J50	0100 0001 111	0 0010
PIC18F86J55	0100 0010 000	0 0010
PIC18F87J50	0100 0010 001	0 0010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F87J50 Family silicon.

1. Module: Oscillator Configuration

The CPU divide-by-6 mode, selected when CPDIV1:CPDIV0 (CONFIG1H<1:0>) = 00, does not work properly and should not be used.

Work around

Use a different CPU divider setting.

Date Codes that pertain to this issue:

All engineering and production devices.

PIC18F87J50 FAMILY

REVISION HISTORY

Rev A Document (4/2007)

Initial release of this document. Silicon issues 1 (Oscillator Configuration) and 2 (USB).

Rev B Document (5/2007)

Removed silicon issue 2 (USB).

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