PIC18F85J11 FAMILY

PIC18F85J11 Family Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39774**C**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F85J11 Family will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: I/O Ports

The following text and table are changed as indicated by the bold text.

10.1.1 INPUT PINS AND VOLTAGE CONSIDERATIONS

The voltage tolerance of pins used as device inputs is dependent on the pin's input function. **Most** pins that are used as digital only inputs are able to handle DC voltages up to 5.5V, a level typical for digital logic circuits. **The digital pins that cannot exceed VDD are RE0, RE1, RE2, RG0, RG2 and RG3**.

In contrast, pins that also have analog input functions of any kind can only tolerate voltages up to VDD. Voltage excursions beyond VDD on these pins should be avoided.

Table 10-1 summarizes the input voltage capabilities. Refer to **Section 25.0 "Electrical Characteristics"** for more details.

TABLE 10-1: INPUT VOLTAGE TOLERANCE

Port or Pin	Tolerated Input	Description
PORTA<7:5>	VDD	Only VDD input levels tolerated.
PORTA<3:0>		
PORTC<1:0>		
PORTE<2:0>		
PORTF<7:1>		
PORTG<3:2>		
PORTG<0>		
PORTA<4>	5.5V	Tolerates input levels above VDD, useful for most standard logic.
PORTB<7:0>		
PORTC<7:2>		
PORTD<7:0>		
PORTE<7:3>		
PORTG<4>		
PORTG<1>		
PORTH<7:0>(1)		
PORTJ<7:0>(1)		

Note 1: Not available on 64-pin devices.

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2. Module: EUSART

Changes in the BAUDCONx registers are made In the following sections:

- In Register 17-3: BAUDCON1: Baud Rate Control Register 1, bit 6 is renamed and bits 5 and 4 are changed and renamed, as shown in bold text.

REGISTER 17-3: BAUDCON1: BAUD RATE CONTROL REGISTER 1

R/W-0	R-1	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is active

bit 5 **RXDTP**: **Data/Receive Polarity Select bit**
Asynchronous mode:
1 = Receive data (RXx) is inverted (active-low)
0 = Receive data (RXx) is not inverted (active-high)
Synchronous mode:
1 = Data (DTx) is inverted (active-low)
0 = Data (DTx) is not inverted (active-high)

bit 4 **TXCKP**: Synchronous Clock Polarity Select bit
Asynchronous mode:
1 = Idle state for transmit (TXx) is a low level
0 = Idle state for transmit (TXx) is a high level
Synchronous mode:
1 = Idle state for clock (CKx) is a high level
0 = Idle state for clock (CKx) is a low level

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH1 and SPBRG1
0 = 8-bit Baud Rate Generator – SPBRG1 only (Compatible mode), SPBRGH1 value ignored

bit 2 **Unimplemented:** Read as ‘0’

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX1 pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RX1 pin not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed
Synchronous mode:
Unused in this mode.

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- Bits 6, 5 and 4 are renamed In the following tables:
  - Table 17-2: Registers Associated with the Baud Rate Generator
  - Table 17-5: Registers Associated with Asynchronous Transmission
  - Table 17-6: Registers Associated with Asynchronous Reception

TABLE 17-2: REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	54
SPBRGH1	EUSART Baud Rate Generator Register High Byte								54
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the BRG.

TABLE 17-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	53
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	53
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
TXREG1	EUSART Transmit Register								53
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	**ABDEN**	54
SPBRGH1	EUSART Baud Rate Generator Register High Byte								54
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53
LATG	U2OD	U1OD	—	LATG4	LATG3	LATG2	LATG1	LATG0	54

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

TABLE 17-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	—	TMR2IF	TMR1IF	53
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	—	TMR2IE	TMR1IE	53
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	—	TMR2IP	TMR1IP	53
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	53
RCREG1	EUSART Receive Register								53
TXSTA1	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	53
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	54
SPBRGH1	EUSART Baud Rate Generator Register High Byte								54
SPBRG1	EUSART Baud Rate Generator Register Low Byte								53

Legend: — = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

- The values for the Resets and WDT wake-up and interrupt are changed in the fourth page of Table 4-2: Initialization Conditions for All Registers, as shown by bold text.

TABLE 4-2: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets CM Resets	Wake-up via WDT or Interrupt
...					
SPBRGH1	PIC18F6XJ11	PIC18F8XJ11	0000 0000	0000 0000	uuuu uuuu
BAUDCON1	PIC18F6XJ11	PIC18F8XJ11	**0100 0-00**	**0100 0-00**	**uuuu u-uu**
CCPR1H	PIC18F6XJ11	PIC18F8XJ11	xxxx xxxx	uuuu uuuu	uuuu uuuu
...					

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

4: See Table 4-1 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read as '0'.

- Bits 6, 5 and 4 are renamed and the POR/BOR value changed in the last page of Table 5-4: PIC18F85J11 Family Register File Summary, as shown in bold text.

TABLE 5-4: PIC18F85J11 FAMILY REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
...										
SPBRGH1	EUSART Baud Rate Generator High Byte								0000 0000	54, 221
BAUDCON1	ABDOVF	**RCIDL**	**RXDTP**	**TXCKP**	BRG16	—	WUE	ABDEN	**0100 0-00**	54, 220
CCPR1H	Capture/Compare/PWM Register 1 High Byte								xxxx xxxx	54, 164
...										

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify

Note 1: Bit 21 of the PC is only available in Test mode and Serial Programming modes.

2: These registers and/or bits are available only on 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset states shown are for 80-pin devices.

3: Alternate names and definitions for these bits when the MSSP module is operating in I^2C™ Slave mode. See Section 16.4.3.2 "Address Masking" for details.

4: The PLLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See Section 2.4.3 "PLL Frequency Multiplier" for details.

5: RA6/RA7 and their associated latch and direction bits are configured as port pins only when the internal oscillator is selected as the default clock source (FOSC2 Configuration bit = 0); otherwise, they are disabled and these bits read as '0'.

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3. Module: Electrical Characteristics

- Parameter VPEW (D132B) in Table 25-1: Memory Programming Requirements, is changed, as shown by the bold text
- The maximum value of parameter VIOFF (D300) is changed in Table 25-2, Comparator Specifications

TABLE 25-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	100	1k	—	E/W	-40°C to +85°C
D131	VPR	VDD for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132B	VPEW	**Voltage for Self-Timed Erase or Write**					
		VDD	**2.70**	**—**	**3.6**	**V**	**ENVREG tied to VDD**
		VDDCORE	**2.25**	**—**	**2.7**	**V**	**ENVREG tied to VSS**
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	3	7	mA	
D1xxx	TWE	Writes per Erase Cycle	—	—	1		Per one physical word address

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 25-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V ≤ VDD ≤ 3.6V, -40°C ≤ TA ≤ +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±5.0	**±25**	mV	
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
300	TRESP	Response Time(1)	—	150	—	ns	
301	TMC2OV	Comparator Mode Change to Output Valid	—	10	—	µs	

Note 1: Response time measured with one comparator input at (AVDD – 1.5)/2, while the other input transitions from VSS to VDD.

4. Module: Reset

Bit 2 and the POR/BOR value are changed for register PORTE in Table 5-4, PIC18F85J11 Family Register File Summary, as shown in bold text.

TABLE 5-4: PIC18F85J11 FAMILY REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page
...										
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	—	xxxx xxx-	54, 138
PORTE	RE7	RE6	RE5	RE4	RE3	**RE2**	RE1	RE0	**xxxx xxxx**	54, 136
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	54, 133
...										

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition, r = reserved, do not modify

Note 1: Bit 21 of the PC is only available in Test mode and Serial Programming modes.

2: These registers and/or bits are available only on 80-pin devices; otherwise, they are unimplemented and read as '0'. Reset states shown are for 80-pin devices.

3: Alternate names and definitions for these bits when the MSSP module is operating in I^2C™ Slave mode. See Section 16.4.3.2 "Address Masking" for details.

4: The PLLEN bit is only available in specific oscillator configurations; otherwise, it is disabled and reads as '0'. See Section 2.4.3 "PLL Frequency Multiplier" for details.

5: RA6/RA7 and their associated latch and direction bits are configured as port pins only when the internal oscillator is selected as the default clock source (FOSC2 Configuration bit = 0); otherwise, they are disabled and these bits read as '0'.

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REVISION HISTORY

Rev A Document (7/2008)

Initial release of this errata. Includes Data Sheet Clarifications 1 (I/O Ports), 2 (EUSART), 3 (Electrical Characteristics) and 4 (Reset).

NOTES:

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