



# MICROCHIP PIC18F2423/2523/4423/4523

## PIC18F2423/2523/4423/4523 Data Sheet Errata

In the Device Data Sheet (DS39755B), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2423/2523/4423/4523 family of devices will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

### 1. Module: EUSART

Since the last revision of the Device Data Sheet, the EUSART module of the PIC18F2423/2523/4423/4523 family of devices has been revised to add new functionality. These changes are:

- The bit, BAUDCON<5>, previously unimplemented, is now implemented with the name RXDTP. Its function is to select the active polarity of the RX/DT pin. Its default state on device Reset is '0'.
- The bit, BAUDCON<4>, previously implemented as SCKP, is now renamed TXCKP. Its function has been expanded to select the active polarity of the TX/CK pin. Its default state on device Reset remains '0'.

The Device Data Sheet is amended as follows:

Register 18-3 (BAUDCON Register) is amended as shown, to include the new bit and bit function descriptions (changes in **bold**).

Table 4-4 of the Device Data Sheet (Initialization Conditions for All Registers) is also amended to show the new Reset conditions of the register, as shown (changes in **bold**).

Throughout the entire Device Data Sheet, all table references to the BAUDCON registers are amended to include RXDTP and TXCKP in bit positions 5 and 4, respectively.

# PIC18F2423/2523/4423/4523

**REGISTER 18-3: BAUDCON: BAUD RATE CONTROL REGISTER (EXCERPT)**

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 5                      **RXDTP: Data/Receive Polarity Select bit**  
Asynchronous mode:  
 1 = Receive data (RX) is inverted (active-low)  
 0 = Receive data (RX) is not inverted (active-high)

Synchronous mode:  
 1 = Data (DT) is inverted (active-low)  
 0 = Data (DT) is not inverted (active-high)

bit 4                      **TXCKP: Clock and Data Polarity Select bit**  
Asynchronous mode:  
 1 = Idle state for transmit (TX) is a low level  
 0 = Idle state for transmit (TX) is a high level  
Synchronous mode:  
 1 = Idle state for clock (CK) is a high level  
 0 = Idle state for clock (CK) is a low level

**TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (EXCERPT)**

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
BAUDCON	2423	2523	4423	4523	0100 0-00	0100 0-00	uuuu u-uu

## REVISION HISTORY

Rev A Document (5/2007)

Original version of this document. Includes Data Sheet  
Clarification 1 (EUSART).

# PIC18F2423/2523/4423/4523

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NOTES:

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