# PIC18F2455/2550/4455/4550 Rev. B6 Silicon Errata

The PIC18F2455/2550/4455/4550 Rev. B6 parts you have received conform functionally to the Device Data Sheet (DS39632**D**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2455/2550/4455/4550 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

**The following silicon errata apply only to PIC18F2455/2550/4455/4550 devices with these Device/Revision IDs:**

| Part Number | Device ID | Revision ID |
|---|---|---|
| PIC18F2455 | 0001 0010 011 | 0 0110 |
| PIC18F2550 | 0001 0010 010 | 0 0110 |
| PIC18F4455 | 0001 0010 001 | 0 0110 |
| PIC18F4550 | 0001 0010 000 | 0 0110 |

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2455/2550/4455/4550 silicon.

## 1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 28-17 and Table 28-18. The updated specification is shown in bold in Table 1.

The minimum time between $\overline{SS}$ pin low and an SSPBUF write is also 3 TCY. If the falling edge of the $\overline{SS}$ pin occurs greater than 3 TCY, before the first SCK edge or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the $\overline{SS}$ pin going low, the peripheral will function correctly.

**Work around**

None.

**Date Codes that pertain to this issue:**

All engineering and production devices.

**TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)**

| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| 70 | TssL2scH, TssL2scL | $\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input | **3 TCY** | — | ns | |

### 2. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

**Work around**

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 3. Module: ECCP (PWM Mode)

When configured for half-bridge operation with dead band (CCPxCON<7:6> = 10), the PWM output may be corrupted for certain values of the PWM duty cycle. This can occur when these additional criteria are also met:

- A non-zero dead-band delay is specified (PDC6:PDC0 > 0)
- The duty cycle has a value of 0 through 3, or 4n + 3 (n ≥ 1)

**Work around**

None.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 4. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 20-3 has been changed to function as shown.

**Work around**

None required.

**Date Codes that pertain to this issue:**

All engineering and production devices of silicon revision B4 or later have the added functionality. The RXDTP bit is not implemented, and the SCKP bit has no effect in Asynchronous mode, on all silicon revision A3 devices.

**REGISTER 20-3: BAUDCON: BAUD RATE CONTROL REGISTER**

| R/W-0 | R-1 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ABDOVF | RCIDL | RXDTP | TXCKP | BRG16 | — | WUE | ABDEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Receive Data Polarity Select bit
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of receive data (RX). Idle state is a high level.
Synchronous mode:
1 = Data (DT) is inverted. Idle state is a low level.
0 = No inversion of data (DT). Idle state is a high level.

bit 4 **TXCKP**: Transmit/Clock Polarity Select bit
Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level.
0 = No inversion of transmit data (TX). Idle state is a high level.
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

bit 3 **BRG16:** 16-bit Baud Rate Register Enable bit
1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode); SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = EUSART will continue to sample the RX pin with the interrupt generated on the falling edge; bit cleared in hardware on following rising edge
0 = RX pin is not monitored or rising edge detected
Synchronous mode:
Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed
Synchronous mode:
Unused in this mode.

### 5. Module: Electrical Characteristics (BOR)

Certain operating conditions can move the effective Brown-out Reset (BOR) threshold outside of the range specified in the electrical characteristics of the device data sheet (parameter D005).

The BOR threshold has been observed to increase with high device operating frequencies, some table read operations and heavy loading on the USB voltage regulator. When all of these conditions are present, BOR has been observed with $V_{DD}$ 20 percent higher than the $V_{BOR}$ value specified for a given <BORV1:BORV0> setting.

The BOR threshold may decrease under other conditions, such as during Sleep, where it may not occur until $V_{DD}$ is 120 mV below the specified minimums.

**Work around**

None.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 6. Module: MSSP (SPI Slave)

If configured in SPI Slave mode, the MSSP may not successfully recognize data packets generated by an external master processor. This applies to all SPI Slave modes (CKE/CKP = `1` or `0`), whether or not slave select is enabled (SSPM3:SSPM0 = `010x`).

**Work around**

Insert a series resistor between the SPI master Serial Data Out (SDO) and the corresponding SPI slave Serial Data In (SDI) input line of the microcontroller. The required value for the resistor varies with the application system's characteristics and the process variations between the microcontrollers.

Experimentation and thorough testing are encouraged.

**Date Codes that pertain to this issue:**

All engineering and production devices.

## 7. Module: MSSP

If the application firmware is expecting to receive valid data – in either SPI slave or Master mode – the firmware must read from the SSPBUF register before writing the next byte to transmit to SSPBUF.

If the firmware does not read from SSPBUF, the BF bit (SSPSTAT<0>) can still be set from the previous transaction. If the BF bit is set, the incoming data byte is blocked from transferring from the SSPSR shift register to the SSPBUF register. If the firmware then reads from SSPBUF, the data read will not match the data most recently received on the SDI pin.

In earlier silicon revisions (A3, B4, and B5), incoming data bytes received on the SDI pin are always transferred from SSPSR to SSPBUF, regardless of the state of the BF bit.

**Work around**

If the firmware expects to receive valid data, always clear the BF bit by reading from SSPBUF prior to writing to SSPBUF, even when the current data in SSPBUF is not important. Sample work-around code, suitable for all silicon revisions, is given in Example 1 (Assembly language) and Example 2 (C language).

**Date Codes that pertain to this issue:**

All engineering and production devices.

**EXAMPLE 1: SAMPLE ASSEMBLY CODE FOR TRANSFERRING SPI DATA**

```
WriteSPI:
BCF    PIR1, SSPIF
MOVF   SSPBUF, w     ;Perform read, even if the data in SSPBUF is not important
MOVLW  0xA5          ;In this example, let's send "0xA5" to the other SPI device.
MOVWF  SSPBUF

WaitXmitComplete:
BTFSS  PIR1, SSPIF
BRA    WaitXmitComplete

MOVF   SSPBUF, w     ;The data received should be valid.
```

**EXAMPLE 2: SAMPLE C CODE FOR TRANSFERRING SPI DATA**

```
unsigned char WriteSPI(unsigned char ByteToSend)
{
   unsigned char TempVariable;

   PIR1bits.SSPIF = 0;
   TempVariable = SSPBUF;     // Reads from SSPBUF, ensures BF bit is clear before
   SSPBUF = ByteToSend;       // sending the next byte.

   while(!PIR1bits.SSPIF);    // Wait until the transmission is complete.
   return SSPBUF;             // The data received should be valid.
}
```

## REVISION HISTORY

Rev A Document (8/2007)
Initial release of this document. Silicon issues 1-2 (MSSP), 3 (ECCP – PWM Mode) and 4 (EUSART).

Rev B Document (3/2008)
Added silicon issue 5 Electrical Characteristics (BOR).

Rev C Document (4/2008)
Added silicon issue 6 (MSSP – SPI Slave).

Rev D Document (5/2008)
Added silicon issue 7 (MSSP).

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