PIC18F2455/2550/4455/4550 Rev. B4 Silicon Errata

The PIC18F2455/2550/4455/4550 Rev. B4 parts you have received conform functionally to the Device Data Sheet (DS39632**D**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2455/2550/4455/4550 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2455/2550/4455/4550 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2455	0001 0010 011	0 0100
PIC18F2550	0001 0010 010	0 0100
PIC18F4455	0001 0010 001	0 0100
PIC18F4550	0001 0010 000	0 0100

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = 0100), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 28-17 and Table 28-18. The updated specification is shown in bold in Table 1.

The minimum time between $\overline{SS}$ pin low and an SSPBUF write is also 3 TCY. If the falling edge of the $\overline{SS}$ pin occurs greater than 3 TCY, before the first SCK edge or loading SSPBUF, the peripheral will function correctly. Also, if SSPBUF is written prior to the $\overline{SS}$ pin going low, the peripheral will function correctly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	**3 TCY**	—	ns	

2. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: ECCP (PWM Mode)

When configured for half-bridge operation with dead band (CCPxCON<7:6> = 10), the PWM output may be corrupted for certain values of the PWM duty cycle. This can occur when these additional criteria are also met:

- a non-zero dead-band delay is specified (PDC6:PDC0 > 0); and
- the duty cycle has a value of 0 through 3, or 4n + 3 (n ≥ 1).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Timer1 and Timer3

For Timer1 or Timer3, if the TMRxH and TMRxL registers are written to in consecutive instruction cycles, the timer may not be updated with the correct value when configured for externally clocked 8-Bit Asynchronous mode (T1CON<7:0> or T3CON<7:0> = 0xxx x111).

For the purposes of this issue, instructions that directly affect the contents of the Timer registers are considered to be writes. This includes CLRF, SETF and MOVF instructions.

Work around

Insert a delay of one or more instruction cycles between writes to TMRxH and TMRxL. This delay can be a NOP, or any instruction that does not access the Timer registers (Example 1).

EXAMPLE 1:

```
CLRF    TMR1H
MOVLW   T1Offset  ; 1 Tcy delay
MOVWF   TMR1L
```

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: ADC

When the A/D clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select a different A/D clock source (4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC, 64 TOSC) and avoid selecting the 2 TOSC or RC modes.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: EUSART

In Synchronous Master mode, while transmitting the Most Significant data bit, the data line (DT) may change state before the bit finishes transmitting. If the receiver samples the data line later than 0.5 bit times + 1.5 TCY (of the master) after the starting edge of the MSb, the bit may be read incorrectly.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: EUSART

One bit has been added to the BAUDCON register and one bit has been renamed.

- Added bit – RXDTP, in the location BAUDCON<5>
- Renamed bit – TXCKP (formerly named SCKP), in the location BAUDCON<4>

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 20-3 is changed to function as shown.

Work around

None required.

Date Codes that pertain to this issue:

All engineering and production devices of silicon revision B4 or later have the added functionality. The RXDTP bit is not implemented, and the SCKP bit has no effect in Asynchronous mode, on all silicon revision A3 devices.

REGISTER 20-3: BAUDCON: BAUD RATE CONTROL REGISTER

R/W-0	R-1	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **ABDOVF**: Auto-Baud Acquisition Rollover Status bit
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Received Data Polarity Select bit
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of received or transmitted data.
Synchronous modes:
1 = Received data is inverted, transmitted data is *not* inverted.
0 = No inversion of received or transmitted data.

REGISTER 20-3: BAUDCON: BAUD RATE CONTROL REGISTER (CONTINUED)

bit 4 **TXCKP**: Clock and Data Polarity Select bit

Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level.
0 = No inversion of transmit data. Idle state is a high level.

Synchronous modes:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

bit 3 **BRG16:** 16-Bit Baud Rate Register Enable bit

1 = 16-bit Baud Rate Generator – SPBRGH and SPBRG
0 = 8-bit Baud Rate Generator – SPBRG only (Compatible mode), SPBRGH value ignored

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit

Asynchronous mode:
1 = EUSART will continue to sample the RX pin – interrupt generated on falling edge; bit cleared in hardware on following rising edge
0 = RX pin not monitored or rising edge detected

Synchronous mode:
Unused in this mode.

bit 0 **ABDEN**: Auto-Baud Detect Enable bit

Asynchronous mode:
1 = Enable baud rate measurement on the next character. Requires reception of a Sync field (55h); cleared in hardware upon completion.
0 = Baud rate measurement disabled or completed

Synchronous mode:
Unused in this mode.

8. Module: Electrical Characteristics (BOR)

Certain operating conditions can move the effective Brown-out Reset (BOR) threshold outside of the range specified in the electrical characteristics of the device data sheet (parameter D005).

The BOR threshold has been observed to increase with high device operating frequencies, some table read operations and heavy loading on the USB voltage regulator. When all of these conditions are present, BOR has been observed with V_{DD} 20 percent higher than the V_{BOR} value specified for a given <BORV1:BORV0> setting.

The BOR threshold may decrease under other conditions, such as during Sleep, where it may not occur until V_{DD} is 120 mV below the specified minimums.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

9. Module: MSSP (SPI Slave)

If configured in SPI Slave mode, the MSSP may not successfully recognize data packets generated by an external master processor. This applies to all SPI Slave modes (CKE/CKP = 1 or 0), whether or not slave select is enabled (SSPM3:SSPM0 = 010x).

Work around

Insert a series resistor between the SPI master Serial Data Out (SDO) and the corresponding SPI slave Serial Data In (SDI) input line of the microcontroller. The required value for the resistor varies with the application system's characteristics and the process variations between the microcontrollers.

Experimentation and thorough testing are encouraged.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: MSSP

When operated in I^2C™ Master mode, the I^2C baud rate may be somewhat slower than predicted by the following formula:

$$I^2C \text{ Master mode, clock} = \frac{F_{OSC}}{4 \bullet (SSPADD + 1)}$$

Work around

If the target application is sensitive to the baud rate and requires more precision, the SSPADD value can be adjusted to compensate.

If this work around is going to be used, it is recommended that the firmware first check the Revision ID by reading the DEVID1 value at address 3FFFFEh. Silicon revisions B6 and B7 will match the I^2C baud rate predicted by the given formula.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (08/2006)
First revision of this document. Silicon issues 1-2 (MSSP) and 3 (ECCP – PWM Mode).

Rev B Document (10/2006)
Added silicon issue 4 (Timer1 and Timer3).

Rev C Document (7/2007)
Added silicon issue 5 (ADC) and 6-7 (EUSART).

Rev D Document (3/2008)
Added silicon issue 8 Electrical Characteristics (BOR).

Rev E Document (4/2008)
Added silicon issue 9 (MSSP – SPI Slave).

Rev F Document (9/2008)
Added silicon issue 10 (MSSP).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

01/02/08