PIC16F882/883/884/886/887 Silicon/Data Sheet Errata

The PIC16F88X parts you have received conform functionally to the Device Data Sheet (DS41291**D**), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16F88X silicon.

1. Module: Low-Voltage In-Circuit Serial Programming™

If LVP (Low-Voltage Programming) mode is enabled, programming the device using the V_{PP} pin while holding high or toggling the port pin RB3/PGM during Program mode could disrupt the programming sequence.

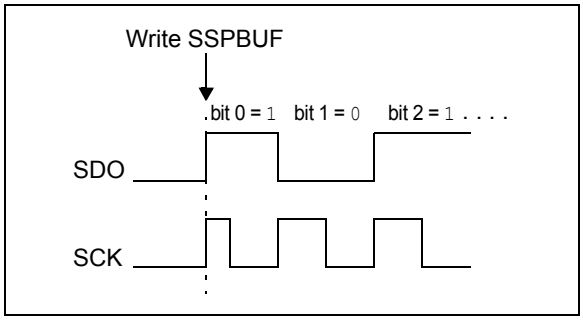
Work around

Pull down pin RB3/PGM using external circuitry during programming of the device.

2. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 1 for sample code.

EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS  SSPSTAT, BF     ;Data received?
                            ;(Xmit complete?)
     GOTO   LOOP            ;No
     MOVF   SSPBUF, W       ;W = SSPBUF
     MOVWF  RXDATA          ;Save in user RAM
     MOVF   TXDATA, W       ;W = TXDATA
     BCF    T2CON, TMR2ON   ;Timer2 off
     CLRF   TMR2            ;Clear Timer2
     MOVWF  SSPBUF          ;Xmit New data
     BSF    T2CON, TMR2ON   ;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Analog-To-Digital Converter (ADC) Module

Selecting the VP6 reference as the analog input source (CHS<3:0> = 1111) for the ADC conversion after sampling another analog channel with input voltages approximately greater than 3.6V can temporarily disturb the HFINTOSC oscillator.

Note:	This only occurs when selecting the VP6 reference ADC channel using the CHS<3:0> bits in the ADCON0 register and NOT during the start of an actual ADC conversion using the GO/$\overline{\text{DONE}}$ bit in the ADCON0 register.

Work around

Select an ADC channel with input voltages lower than 3.6V prior to selecting the VP6 reference voltage input. Any analog channel can be used, even if that channel is configured as a digital I/O (configured as an output) that is driving the output pin low. An alternative is to configure the CVREF module to output a voltage less than 3.6V and then selecting that analog channel CHS<3:0> = 1110 as the analog input source.

EXAMPLE 2: AVOID DISTURBING THE HFINTOSC OSCILLATOR

```
BANKSEL    ADCON0        ;
MOVLW      B'XX111001'   ;Select ADC
MOVWF      ADCON0        ;Channel CVREF
MOVLW      B'XX111101'   ;Select ADC
MOVWF      ADCON0        ;Channel VP6
```

Silicon Fix

None.

4. Module: MSSP (SPI Master Mode)

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

5. Module: MSSP (I^2C™ Slave Mode)

When the master device wants to terminate receiving any more data from the slave device, it will do so by sending a NACK in response to the last data byte received from the slave. When the slave receives the NACK, the R/W bit of the SSPSTAT register remains set improperly.

Work around

Use the CKP bit of the SSPCON register to determine when the master has responded with a NACK. The CKP bit will be clear when the response is an ACK, and set when the response is a NACK. The CKP bit is automatically cleared to stretch the clock when the master responds to received data with an ACK. This gives the slave time to load the SSPBUF register before setting the CKP bit to release the clock stretching. When the master responds to received data with a NACK the CKP bit properly remains set, and there is no clock stretching.

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: MSSP (I^2C™ Master Mode)

When the MSSP is I^2C™ Master mode with a slave device stretching the clock, the clock generation does not function as described in the data sheet.

When a slave device is performing clock stretching by pulling the SCL line low, the master device should continuously sample the SCL line to determine when all slaves have released SCL. When SCL is released, the master device should wait one BRG period to ensure a constant SCL high time.

The current implementation does not guarantee accurate SCL high time. During clock stretch, the MSSP device will erroneously continue running the BRG counter. At the end of the clock stretch the BRG counter continues to count down for the remainder of the BRG period, and then the MSSP device will immediately resume transmitting the data.

Figure 1 illustrates an expected I^2C transmission in which the SCL line is completely controlled by the master device and the slave device does not attempt to stretch the clock period.

Figure 2 illustrates the expected operation of an I^2C transmission in which the slave device has stretched the clock period by holding the SCL line low. The high time of the SCL pulse is constant, regardless of the duration of the clock stretch.

Figure 3 and Figure 4 illustrate an actual I^2C transmission in which the slave has stretched the clock period by holding the SCL line low. Note that the high time of the SCL signal has shortened from the expected time.

FIGURE 1: ACTUAL (CORRECT) OPERATION WITHOUT CLOCK STRETCHING

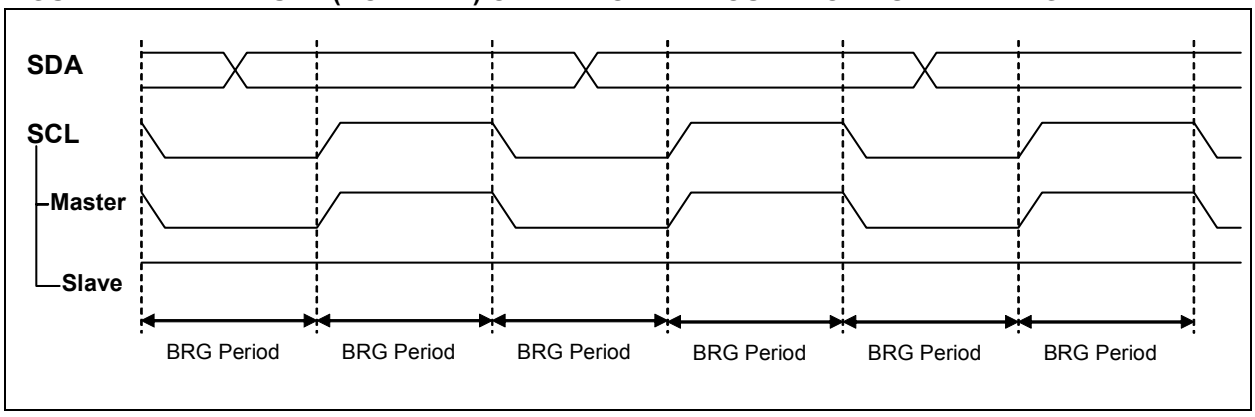


FIGURE 2: EXPECTED OPERATION WITH CLOCK STRETCHING

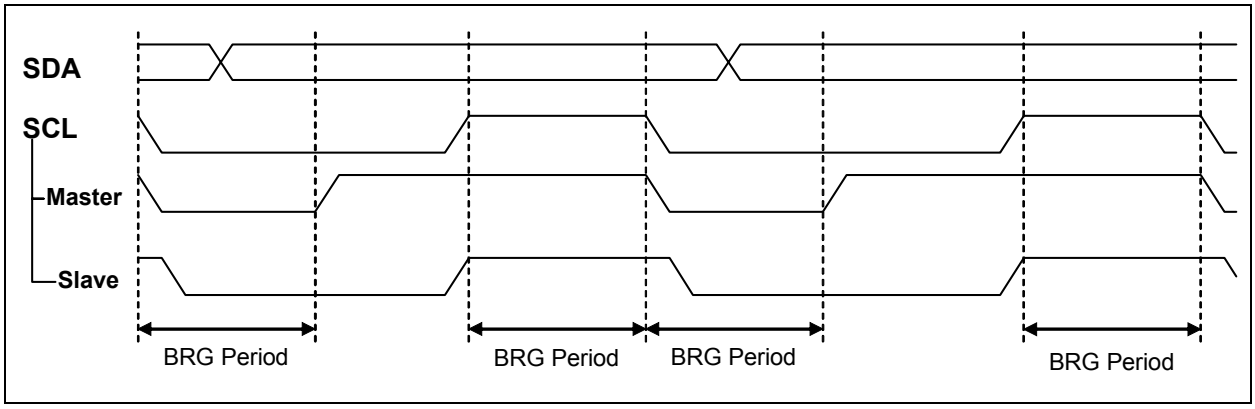


FIGURE 3: ACTUAL (INCORRECT) OPERATION WITH CLOCK STRETCHING – EXAMPLE 1

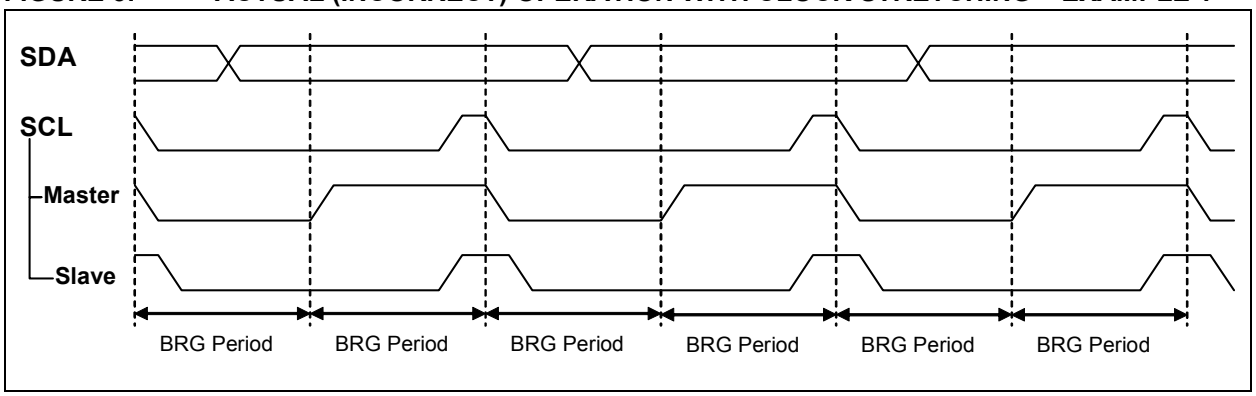
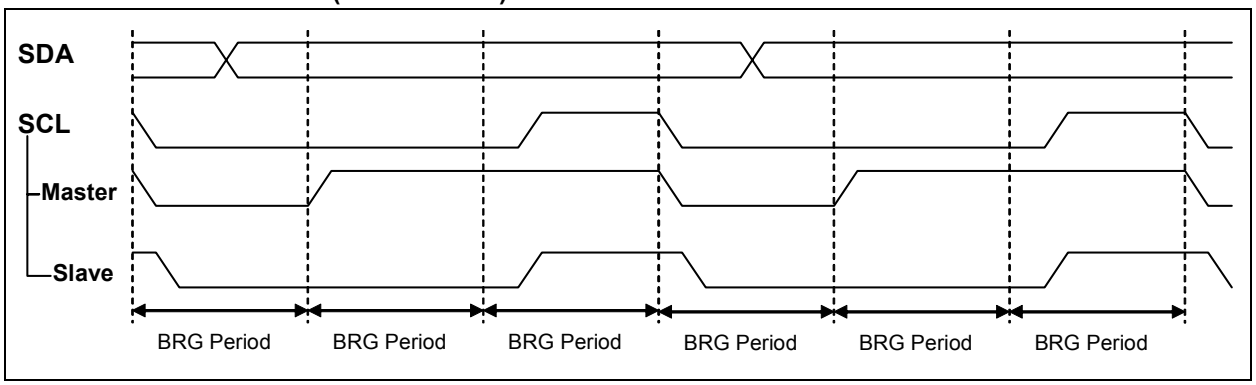


FIGURE 4: ACTUAL (INCORRECT) OPERATION WITH CLOCK STRETCHING – EXAMPLE 2



Work around

Set the communication speed to match the slowest device on the bus. This ensures that no slave device will perform clock stretching.

It is possible to dynamically adjust the communication speed to match the device being addressed by modifying the BRG register. However, the behavior of slower slave devices must be understood and speed adjustments made such that no slave performs clock stretching.

Date Codes that pertain to this issue:

All production devices.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41291**D**), the following clarifications and corrections should be noted.

1. Module: Product Identification System

Updated Device and Note sections in Product Identification System Table. Added SP; Skinny Plastic Dip to Package section (in bold).

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:	PIC16F882, PIC16F882T(1), PIC16F883, PIC16F883T(1), PIC16F884, PIC16F884T(1), PIC16F886, PIC16F886T(1), PIC16F887, PIC16F887T(1) VDD range 2.0V to 5.5V	
Temperature Range:	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package:	ML = Quad Flat No Leads (QFN) P = Plastic DIP PT = Plastic Thin-Quad Flatpack (TQFP) SO = Plastic Small Outline (SOIC) (300 mil) **SP = Skinny Plastic DIP** SS = Plastic Shrink Small Outline	
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16F883-E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301

b) PIC16F883-I/SO = Industrial Temp., SOIC package, 20 MHz

Note 1: T = In tape and reel TSSOP, SOIC and QFN packages only.

2. Module: Electrical Specification (Supply Current)

Updated the Electrical Specification for Supply Current (I_{DD}) and Power-down Base Current (I_{PD}) as indicated below (in bold).

17.2 DC Characteristics: PIC16F882/883/884/886/887-I (Industrial) PIC16F882/883/884/886/887-E (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	**Supply Current (I_{DD})(1, 2)**	—	**13**	**19**	µA	2.0	FOSC = 32 kHz LP Oscillator mode
		—	**22**	**30**	µA	3.0	
		—	**33**	**60**	µA	5.0	
D011*		—	**180**	**250**	µA	2.0	FOSC = 1 MHz XT Oscillator mode
		—	**290**	400	µA	3.0	
		—	**490**	650	µA	5.0	
D012		—	**280**	380	µA	2.0	FOSC = 4 MHz XT Oscillator mode
		—	**480**	670	µA	3.0	
		—	**0.9**	1.4	mA	5.0	
D013*		—	**170**	**295**	µA	2.0	FOSC = 1 MHz EC Oscillator mode
		—	**280**	**480**	µA	3.0	
		—	**470**	**690**	µA	5.0	
D014		—	**290**	**450**	µA	2.0	FOSC = 4 MHz EC Oscillator mode
		—	**490**	**720**	µA	3.0	
		—	**0.85**	**1.3**	mA	5.0	
D015		—	8	20	µA	2.0	FOSC = 31 kHz LFINTOSC mode
		—	16	40	µA	3.0	
		—	31	65	µA	5.0	
D016*		—	**416**	**520**	µA	2.0	FOSC = 4 MHz HFINTOSC mode
		—	**640**	**840**	µA	3.0	
		—	**1.13**	**1.6**	mA	5.0	
D017		—	**0.65**	**0.9**	mA	2.0	FOSC = 8 MHz HFINTOSC mode
		—	**1.01**	**1.3**	mA	3.0	
		—	**1.86**	**2.3**	mA	5.0	
D018		—	**340**	580	µA	2.0	FOSC = 4 MHz EXTRC mode(3)
		—	**550**	**900**	µA	3.0	
		—	**0.92**	**1.4**	mA	5.0	
D019		—	**3.8**	**4.7**	mA	4.5	FOSC = 20 MHz HS Oscillator mode
		—	**4.0**	**4.8**	mA	5.0	

17.3 DC Characteristics: PIC16F882/883/884/886/887-I (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D026	**Power-down Base Current (IPD)(2)**	—	**2.0**	**5.0**	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	**2.5**	**5.5**	µA	3.0	
		—	**3.0**	**7.0**	µA	5.0	

17.4 DC Characteristics: PIC16F882/883/884/886/887-I (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D026E	**Power-down Base Current (IPD)(2)**	—	**3.5**	**18**	µA	2.0	T1OSC Current(1), 32.768 kHz
		—	**4**	**21**	µA	3.0	
		—	**5**	**24**	µA	5.0	

APPENDIX A: REVISION HISTORY

Rev. A Document (2/2007)

First revision of this document.

Added Module 1: Low-Voltage In-Circuit Serial Programming™ (PIC16F884/883 Silicon Rev. A0); Added Module 2: MSSP (SPI Mode).

Clarifications/Corrections to the Data Sheet - Added Module 1: Product Identification System.

Rev. B Document (5/2007)

Clarifications/Corrections to the Data Sheet - Added Module 2: Electrical Specification - Supply Current.

Rev. C Document (7/2007)

Added Module 3: Analog-to-Digital Converter (ADC) Module.

Rev. D Document (8/2007)

Added Module 4: MSSP (SPI Master Mode), Module 5: MSSP (I^2C Slave Mode) and Module 6: MSSP (I^2C Master Mode).

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