

## PIC12F510 Rev. A Silicon/Data Sheet Errata

The PIC12F510 parts you have received conform functionally to the Device Data Sheet (DS41268D), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC12F510 silicon.

### 1. Module: Analog-to-Digital (ADC) Converter

For PIC12F510 silicon Rev. A3, the specifications listed in Table 1 supersede Table 13-3 in DS41268D. The PIC12F510 will meet the performance specifications stated in Table 1 below if the device is operated as described in this Errata.

#### Work around

None.

**TABLE 1: A/D CONVERTER CHARACTERISTICS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A03	EIL	Integral Error	—	—	±1.5	LSB	VDD = 5.0V
A04	EDL	Differential Error	—	—	-1 < EdL ≤ +1.5	LSB	VDD = 5.0V
A06	E <sub>OFF</sub>	Offset Error	—	—	±1.5	LSB	VDD = 5.0V
A07	E <sub>GN</sub>	Gain Error	—	—	±1.5	LSB	VDD = 5.0V

† Data in “Typ” column is at 5.0V 25°C unless otherwise stated. The typical parameters are for design guidance only and are not tested.

# PIC12F510

## Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41268D), the following clarifications and corrections should be noted.

### 1. Module: Analog-to-Digital Converter (ADC)

**Section 9.1 “Clock Divisors”**, paragraph 1 should read as follows as shown in bold.

The ADC has 4 clock source settings, ADCS<1:0>. There are 3 divisor values, **16**, **8** and **4**. The fourth setting is INTOSC with a divisor of 4.

Table 9-2 below should replace the current Table 9-2 in the data sheet.

**TABLE 9-2: TAD FOR ADCS SETTINGS WITH VARIOUS OSCILLATORS<sup>(1)</sup>**

Source	ADCS<1:0>	Divisor	8 MHz	4 MHz	1 MHz	500 kHz	350 kHz	200 kHz	100 kHz	32 kHz
INTOSC	11	<b>4</b>	.5 $\mu$ s	1 $\mu$ s	—	—	—	—	—	—
FOSC	10	<b>4</b>	.5 $\mu$ s	1 $\mu$ s	4 $\mu$ s	8 $\mu$ s	11 $\mu$ s	20 $\mu$ s	40 $\mu$ s	125 $\mu$ s
FOSC	01	<b>8</b>	1 $\mu$ s	2 $\mu$ s	8 $\mu$ s	16 $\mu$ s	23 $\mu$ s	40 $\mu$ s	80 $\mu$ s	250 $\mu$ s
FOSC	00	<b>16</b>	2 $\mu$ s	4 $\mu$ s	16 $\mu$ s	32 $\mu$ s	46 $\mu$ s	80 $\mu$ s	160 $\mu$ s	500 $\mu$ s

**Note 1:** Operation of the ADC module clock in any of the shaded regions shown in this table (Table 9-2) may result in linearity errors exceeding the limits stated in Table 1 of this Errata. (page 1).

### 2. Module: Analog-to-Digital Converter (ADC)

**Section 9.1.5 “Sleep”**, bullets should read as follows (changes in bold).

- For accurate conversions, TAD must meet the following:
- **$2 \mu\text{s} \leq \text{TAD} < 80 \mu\text{s}$**
- $\text{TAD} = 1/(\text{FOSC}/\text{divisor})$

Delete paragraph, “Shaded areas indicate...for the ADC clock source.”

### 3. Module: Analog-to-Digital Converter (ADC)

Examples 9-1 and 9-2 changes shown in bold below.

#### EXAMPLE 9-1: PERFORMING AN ANALOG-TO-DIGITAL CONVERSION

```

;Sample code operates out of BANK0
        MOVLW 0xF1      ;configure A/D
        MOVWF ADCON0
        BSF ADCON0, 1  ;start conversion
loop0   NOOP
        BTFSC ADCON0, 1;wait for 'DONE'
        GOTO loop0
        MOVF ADRES, W  ;read result
        MOVWF result0 ;save result

        BSF ADCON0, 2 ;setup for read of
                        ;channel 1
        BSF ADCON0, 1 ;start conversion
loop1   NOOP
        BTFSC ADCON0, 1;wait for 'DONE'
        GOTO loop1
        MOVF ADRES, W  ;read result
        MOVWF result1 ;save result

        BSF ADCON0, 3 ;setup for read of
        BCF ADCON0, 2 ;channel 2
        BSF ADCON0, 1 ;start conversion
loop2   NOOP
        BTFSC ADCON0, 1;wait for 'DONE'
        GOTO loop2
        MOVF ADRES, W  ;read result
        MOVWF result2 ;save result
    
```

#### EXAMPLE 9-2: CHANNEL SELECTION CHANGE DURING CONVERSION

```

        MOVLW 0xF1      ;configure A/D
        MOVWF ADCON0
        BSF ADCON0, 1  ;start conversion
        BSF ADCON0, 2  ;setup for read of
                        ;channel 1
loop0   NOOP
        BTFSC ADCON0, 1;wait for 'DONE'
        GOTO loop0
        MOVF ADRES, W  ;read result
        MOVWF result0 ;save result

        BSF ADCON0, 1  ;start conversion
        BSF ADCON0, 3  ;setup for read of
        BCF ADCON0, 2  ;channel 2
loop1   NOOP
        BTFSC ADCON0, 1;wait for 'DONE'
        GOTO loop1
        MOVF ADRES, W  ;read result
        MOVWF result1 ;save result

        BSF ADCON0, 1  ;start conversion
loop2   NOOP
        BTFSC ADCON0, 1;wait for 'DONE'
        GOTO loop2
        MOVF ADRES, W  ;read result
        MOVWF result2 ;save result
        CLRF ADCON0   ;optional: returns
                        ;pins to Digital mode and turns off
                        ;the ADC module
    
```

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## REVISION HISTORY

### Rev A Document (03/2006)

First Revision – Module 1: Analog-to-Digital Converter.

### Rev B Document (08/2006)

Clarifications/Corrections to the Data Sheet: Added Module 1: Analog-to Digital Converter: Correction to Section 9.1 Clock Divisors, paragraph 1; Table 9-2, TAD for ADCS.

### Rev C Document (03/2008)

Updated Module 1 by removing 25°C from Conditions and updated paragraph.

Clarifications/Corrections to the Data Sheet: Updated Module 1: Analog-to Digital Converter by rewording and adding Table 9-2 updates. Added Modules 2 and 3 (Analog-to Digital Converter).

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