dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 Rev. A1 Silicon Errata

The dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 (Rev. A1) devices you have received were found to conform to the specifications and functionality described in the following documents:

- "*dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 Data Sheet*" (DS70292)
- "*dsPIC30F/33F Programmer's Reference Manual*" (DS70157)

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC33FJ128GP804
- dsPIC33FJ128GP802
- dsPIC33FJ128GP204
- dsPIC33FJ128GP202
- dsPIC33FJ64GP804
- dsPIC33FJ64GP802
- dsPIC33FJ64GP204
- dsPIC33FJ64GP202
- dsPIC33FJ32GP304
- dsPIC33FJ32GP302

dsPIC33FJ32GP302/304, dsPIC33FJ64GPX02/X04, and dsPIC33FJ128GPX02/X04 Rev. A1 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 with MPLAB IDE v7.40 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*. The resulting DEVREV register value for Rev. A1 silicon is 0x3001.

The errata described in this document will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail in the remainder of this document.

1. UART Module

   The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.

2. UART Module

   When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

3. SPI Module

   The SPI transmit buffer full (SPITBF) flag does not get set immediately after writing to the buffer.

4. SPI Module in Frame Master Mode

   The SPI module will generate incorrect frame synchronization pulses in Frame Master mode if FRMDLY = 1.

5. I^2C™ Module

   The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.

6. I^2C Module

   The ACKSTAT bit is cleared shortly after being set following a slave transmit.

7. I^2C Module: 10-bit Addressing Mode

   When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.

The following sections describe the errata and work around to these errata, where they may apply.

1. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

2. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

3. Module: SPI

The SPI transmit buffer full (SPITBF) flag does not get set immediately after writing to the buffer.

Work around

After a write to the SPI buffer, poll the SPITBF flag until the flag gets set, indicating that the transmit buffer is not full. Afterwards, poll the SPITBF flag again until the flag gets cleared, indicating that the transmit has started and that the transmit buffer is empty and another write can occur.

4. Module: SPI

The SPI module will generate incorrect frame synchronization pulses when configured in Frame Master mode if the start of data is selected to coincide with the start of the frame synchronization pulse (FRMEN = 1, SPIFSD = 0, FRMDLY = 1). However, the module functions correctly in Frame Slave mode, and also in Frame Master mode if FRMDLY = 0.

Work around

If DMA is not being used, manually drive the SSx pin (x = 1 or 2) high using the associated PORT register, and then drive it low after the required 1 bit time pulse width. This operation needs to be performed when the transmit buffer is written.

If DMA is being used, and if no other peripheral modules are using DMA transfers, use a timer interrupt to periodically generate the frame synchronization pulse (using the method described above) after every 8 or 16-bit periods (depending on the data word size, configured using the MODE16 bit).

If FRMDLY = 0, no work around is needed.

5. Module: I^2C

The BCL bit in I2CSTAT can only be cleared with Word instructions, and can be corrupted with byte instructions and bit operations.

Work around

Use Word instructions to clear BCL.

6. Module: I^2C

During I^2C communication, after a device operating in Slave mode transmits data to the master, the ACKSTAT bit in the I2CxSTAT register is set or cleared depending on whether the master sent an ACK or NACK after the byte of data. If the ACKSTAT bit is set, it will be cleared again after some delay.

Work around

Store the value of the ACKSTAT bit immediately after an I^2C interrupt occurs.

7. Module: I^2C

If there are two I^2C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I^2C devices, the addresses as well as bits A10 and A9 should be different.

APPENDIX A: REVISION HISTORY

Revision A (03/2008)

This is the initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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