dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304

dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 Rev. A2/A3 Silicon Errata

The dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 (Rev. A2/A3) devices you received were found to conform to the specifications and functionality described in the following documents:

- DS70283 – "*dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 Data Sheet*"
- DS70157 – "*dsPIC30F/33F Programmer's Reference Manual*"

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC33FJ32MC202
- dsPIC33FJ32MC204
- dsPIC33FJ16MC304

dsPIC33FJ32MC202/204 and dsPIC33FJ16MC304 Rev. A2/A3 silicon is identified by performing a "Reset and Connect" operation to the device using MPLAB® ICD 2 or MPLAB REAL ICE™ in-circuit emulator, with MPLAB IDE v7.60 or later. The output window will show a successful connection to the device specified in *Configure>Select Device*. The resulting DEVREV register values for Rev. A2/A3 silicon are 0x3001 and 0x3002, respectively.

The errata described in this document will be addressed in future revisions of silicon.

Silicon Errata Summary

The following list summarizes the errata described in further detail through the remainder of this document:

1. JTAG Programming

   JTAG programming does not work.

2. UART

   The auto-baud feature may not calculate the correct baud rate when the Baud Rate Generator (BRG) is set up for 4x mode.

3. UART

   With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

4. UART

   The auto-baud feature measures baud rate inaccurately for certain baud rate and clock speed combinations.

5. UART

   When an auto-baud is detected, the receive interrupt may occur twice.

6. Motor Control PWM - PWM Counter Register

   PTMR does not keep counting down after halting code execution in Debug mode.

7. Quadrature Encoder Interface (QEI) Module

   The QEI module does not generate an interrupt in a particular overflow condition.

8. UART Module

   The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.

9. UART Module

   When the UART is in 4x mode (BRGH = `1`) and using two Stop bits (STSEL = `1`), it may sample the first Stop bit instead of the second one.

10. SPI Module

    The SPIxCON1 DISSCK bit does not influence port functionality.

11. I^2C Module

    The BCL bit in I2CSTAT can be cleared only with 16-bit operation and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

12. I^2C Module

    The ACKSTAT bit is cleared shortly after being set following a slave transmit.

13. I^2C Module: 10-bit addressing mode

    When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C device A10 and A9 bits may not work as expected.

14. Product Identification

    Revision A2 devices marked as extended temperature range (E) devices, support only industrial temperature range (I).

The following sections describe the errata and work around to these errata, where they may apply.

1. Module: JTAG Programming

JTAG programming does not work.

Work around

None.

2. Module: UART

The auto-baud feature may not calculate the correct baud rate when the High Baud Rate Enable bit, BRGH, is set. With the BRGH bit set, the baud rate calculation used is the same as BRG = `0`.

Work around

If the auto-baud feature is needed, use the Low Baud Rate mode by clearing the BRGH bit.

3. Module: UART

With the auto-baud feature selected, the Sync Break character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync Break character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = `1`).

4. Module: UART

The auto-baud feature may miscalculate for certain baud rate and clock speed combinations, resulting in a BRG value that is greater than or less than the expected value by 1. This may result in reception or transmission failures.

Work around

Test the auto-baud rate at various clock speed and baud rate combinations that would be used in an application. If an inaccurate BRG value is generated, manually correct the baud rate in user software.

EXAMPLE 1:

```
unsigned int POSCNT_b15 = 0;
unsigned int Motor_Position = 0;

int main(void)
{
           // ... User's code

           MAXCNT = 0x7FFF;       // Instead of 0xFFFF

           Motor_Position = POSCNT_b15 + POSCNT;

           // ... User's code
}
void __attribute__((__interrupt__)) _QEIInterrupt(void)
{
           IFSxbits.QEIIF = 0;    // Clear QEI interrupt flag
                                  // x=2 for dsPIC30F
                                  // x=3 for dsPIC33F
           POSCNT_b15 ^= 0x8000;  // Overflow or Underflow
}
```

5. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If an extra interrupt is detected, ignore the additional interrupt.

6. Module: Motor Control PWM - PWM Counter Register

If the PTDIR bit is set (when PTMR is counting down), and the CPU execution is halted (after a breakpoint is reached), PTMR will start counting up, as if PTDIR was zero.

Work around

None.

7. Module: QEI Interrupt Generation

The Quadrature Encoder Interface (QEI) module does not generate an interrupt when MAXCNT is set to 0xFFFF and the following events occur:

1. POSCNT underflows from 0x0000 to 0xFFFF.
2. POSCNT stops.
3. POSCNT overflows from 0xFFFF to 0x0000.

This sequence of events occurs when the motor is running in one direction, which causes POSCNT to underflow to 0xFFFF. Once this happens, the motor stops and starts to run in the opposite direction, which generates an overflow from 0xFFFF to 0x0000. The QEI module does not generate an interrupt when this condition occurs.

Work around

To prevent this condition from occurring, set MAXCNT to 0x7FFF, which will cause an interrupt to be generated by the QEI module.

In addition, a global variable could be used to keep track of bit 15, so that when an overflow or underflow condition is present on POSCNT, the variable will toggle bit 15. Example 2 shows the code required for this global variable.

EXAMPLE 2:

```
unsigned int POSCNT_b15 = 0;
unsigned int Motor_Position = 0;

int main(void)
{
            // ... User's code

            MAXCNT = 0x7FFF;       // Instead of 0xFFFF

            Motor_Position = POSCNT_b15 + POSCNT;

            // ... User's code
}
void __attribute__((__interrupt__)) _QEIInterrupt(void)
{
            IFSxbits.QEIIF = 0;    // Clear QEI interrupt flag
                                   // x=2 for dsPIC30F
                                   // x=3 for dsPIC33F
            POSCNT_b15 ^= 0x8000;  // Overflow or Underflow
}
```

8. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = `11`), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an idle state.

9. Module: UART

When the UART is in 4x mode (BRGH = `1`) and using two Stop bits (STSEL = `1`), it may sample the first Stop bit instead of the second one. This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = `0`) and adjust the baud rate accordingly.

10. Module: SPI

When the SPI module is enabled, setting the DISSCK bit in the SPIxCON1 register does not allow the user application to use the SCK pin as a general purpose I/O pin.

Work around

None.

11. Module: I^2C

The BCL bit in I2CSTAT can be cleared only with 16-bit operation and can be corrupted with 1-bit or 8-bit operations on I2CSTAT.

Work around

Use 16-bit operations to clear BCL.

12. Module: I^2C

During I^2C communication, after a device operating in Slave mode transmits data to the master, the ACKSTAT bit in the I2CxSTAT register is set or cleared depending on whether the master sent an ACK or NACK after the byte of data. If the ACKSTAT bit is set it will be cleared again after some delay.

Work around

Store the value of the ACKSTAT bit immediately after an I^2C interrupt occurs.

13. Module: I^2C

If there are two I^2C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. Suppose that both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses. When the Slave select address is sent from the Master, both the Master and Slave acknowledges it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

Use different addresses including the higher two bits (A10 and A9) for different modules.

14. Module: Product Identification

Revision A2 devices marked as extended temperature range (E) devices, support only industrial temperature range (I).

Work around

Use Revision A3 devices marked as extended temperature range (E) devices.

APPENDIX A: REVISION HISTORY

Revision A (8/2007)

Initial release of this document, which includes silicon issues 1 (JTAG Programming) and 2-4 (UART).

Revision B (11/2007)

Added silicon issues 5 (UART) and 6 (Motor Control PWM - PWM Counter Register).

Revision C (4/2008)

Added silicon issues 7 (QEI Interrupt Generation), 8-9 (UART), 10 (SPI), 11-13 (I^2C), and 14 (Product Identification).

NOTES:

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