STM32F101xC/D/E and STM32F103xC/D/E Errata sheet

STM32F101xC/D/E and STM32F103xC/D/E revision Z High-density device limitations

Silicon identification

This errata sheet applies to the revision Z of the STMicroelectronics STM32F101xC/D/E access line and STM32F103xC/D/E performance line High-density products. These families feature an ARM™ 32-bit Cortex®-M3 core, for which an errata notice is also available (see *Section 1* for details).

The full list of root part numbers is shown in *Table 2*. The products are identifiable as shown in *Table 1*:

- by the Revision code marked below the Sales Type on the device package
- by the last three digits of the Internal Sales Type printed on the box label

Table 1. Device Identification(1)

Sales type	Revision code(2) marked on device
STM32F103xC, STM32F103xD, STM32F103xE	"Z"
STM32F101xC, STM32F101xD, STM32F101xE	"Z"

1. The REV_ID bits in the DBGMCU_IDCODE register show the revision code of the device (see the STM32F10xxx reference manual for details on how to find the revision code).
2. Refer to *Appendix A: Revision code on device marking* for details on how to identify the Revision code on the different packages.

Table 2. Device summary

Reference	Part number
STM32F101xCDE	STM32F101RC STM32F101VC STM32F101ZC
	STM32F101RD STM32F101VD STM32F101ZD
	STM32F101RE STM32F101VE STM32F101ZE
STM32F103xCDE	STM32F103RC STM32F103VC STM32F103ZC
	STM32F103RD STM32F103VD STM32F103ZD
	STM32F103RE STM32F103VE STM32F103ZE

1 ARM™ 32-bit Cortex®-M3 limitations

An errata notice of the STM32F10xxx core is available from the following web address: *http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.eat0420a/*.
The direct link to the errata notice pdf is:
http://infocenter.arm.com/help/topic/com.arm.doc.eat0420a/Cortex-M3-Errata-r1p1-v0.2.pdf.
All the described limitations are minor and related to the revision r1p1-01rel0 of the Cortex-M3 core.

2 STM32F10xxx silicon limitations

2.1 Voltage glitch on ADC input 0

Description

A low-amplitude voltage glitch may be generated (on ADC input 0) on the PA0 pin, when the ADC is converting with injection trigger. It is generated by internal coupling and synchronized to the beginning and the end of the injection sequence, whatever the channel(s) to be converted.

The glitch amplitude is less than 150 mV with a typical duration of 10 ns (measured with the I/O configured as high-impedance input and left unconnected). If PA0 is used as a digital output, this has no influence on the signal. If PA0 is used has a digital input, it will not be detected as a spurious transition, providing that PA0 is driven with an impedance lower than 5 kΩ This glitch does not have any influence on the remaining port A pin or on the ADC conversion injection results, in single ADC configuration.

When using the ADC in dual mode with injection trigger, and in order to avoid any side effect, it is advised to distribute the analog channels so that Channel 0 is configured as an injected channel.

Workaround

None.

2.2 Flash memory read after WFI/WFE instruction

Conditions

- Flash prefetch on
- Flash memory timing set to 2 wait states
- FLITF clock stopped in Sleep mode

Description

If a WFI/WFE instruction is executed during a Flash memory access and the Sleep duration is very short (less than 2 clock cycles), the instruction fetch from the Flash memory may be corrupted on the next wakeup event.

Workaround

When using the Flash memory with two wait states and prefetch on, the FLITF clock must *not* be stopped during the Sleep mode – the FLITFEN bit in the RCC_AHBENR register must be set (keep the reset value).

2.3 Debug registers cannot be read by user software

Description

The DBGMCU_IDCODE and DBGMCU_CR debug registers are accessible only in debug mode (not accessible by the user software). When these registers are read in user mode, the returned value is 0x00.

Workaround

None.

2.4 Alternate function

In some specific cases, some potential weakness may exist between alternate functions mapped onto the same pin.

2.4.1 USART1_RTS and CAN_TX

Conditions

- USART1 is clocked
- CAN is not clocked
- I/O port pin PA12 is configured as an alternate function output.

Description

Even if CAN_TX is not used, this signal is set by default to 1 if I/O port pin PA12 is configured as an alternate function output.

In this case USART1_RTS cannot be used.

Workaround

When USART1_RTS is used, the CAN must be remapped to either another IO configuration when the CAN is used, or to the unused configuration (CAN_REMAP[1:0] set to “01”) when the CAN is not used.

2.4.2 SPI1 in slave mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal), if SPI1 is used in slave mode.

Workaround

None.

2.4.3 SPI1 in master mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal) if SPI1 is used in master mode and SP1_NSS is configured in software mode. In this case USART2_CK is not output on the pin.

Workaround

In order to output USART2_CK, the SSOE bit in the SPI1_CR2 register must be set to configure the pin in output mode.

2.4.4 SPI2 in slave mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in slave mode.

Workaround

None.

2.4.5 SPI2 in master mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in master mode and SP2_NSS is configured in software mode. In this case USART3_CK is not output on the pin.

Workaround

In order to output USART3_CK, the SSOE bit in the SPI2_CR2 register must be set to configure the pin in output mode,

2.4.6 SDIO with TIM8

Description

Conflicts occur when:

- the SDIO is configured in 1- or 4-bit mode and TIM8_CH4 is configured as an output

The signals that conflict are the following:

- TIM8_CH4 and SDIO_D1

Workaround

Do not use TIM8_CH4 as an output when the SDIO is being used.

2.4.7 SDIO and TIM3_REMAP

Description

When SDIO is configured in 1- or 4-bit mode, and TIM3 channels are remapped to PC6 to PC9, and configured as outputs, a conflict occurs between:

- TIM3_CH4 and SDIO_D1

Workaround

Do not use TIM3_CH4 as an output when the SDIO is being used.

2.4.8 SDIO with USART3 remapped and UART4

Description

When SDIO is configured in 1-bit mode, there are conflicts with the USART3_TX pin remapped and with the UART4_TX pin. Conflicts are between the following signals:

- USART3_TX and SDIO_D2
- UART4_TX and SDIO_D2

Workaround

Use USART3_TX either in the default configuration (on the PB10 I/O) or remap USART3_TX to PD8 when the SDIO is being used.

Do not use UART4_TX when the SDIO is being used.

2.4.9 FSMC with I2C1 and TIM4_CH2

Description

When the FSMC is being used, the NADV signal is set to 1 by default when the alternate function output is selected for this pin. TIM4_CH2 and the I2C1 SDA signal are in conflict with the NADV signal.

Workaround

Do not use TIM4_CH2 when the FSMC is being used.

Concerning I2C1, it is possible to use the remap functionality available on the PB8 and PB9 pins.

2.4.10 FSMC with USART2 remapped

Description

When the FSMC is being used, the NE1 signal is set to 1 by default when the alternate function output is selected for this pin.

There is a conflict between the CK signal of USART2 and NE1.

Workaround

Use the USART2 default configuration (no remap).

Appendix A Revision code on device marking

Figure 1, *Figure 2*, *Figure 3*, *Figure 4* and *Figure 5* show the marking compositions for the LFBGA144, LFBGA100, LQFP144, LQFP100 and LQFP64 packages, respectively. Only the Additional field containing the Revision code is shown.

Figure 1. LFBGA144 top package view

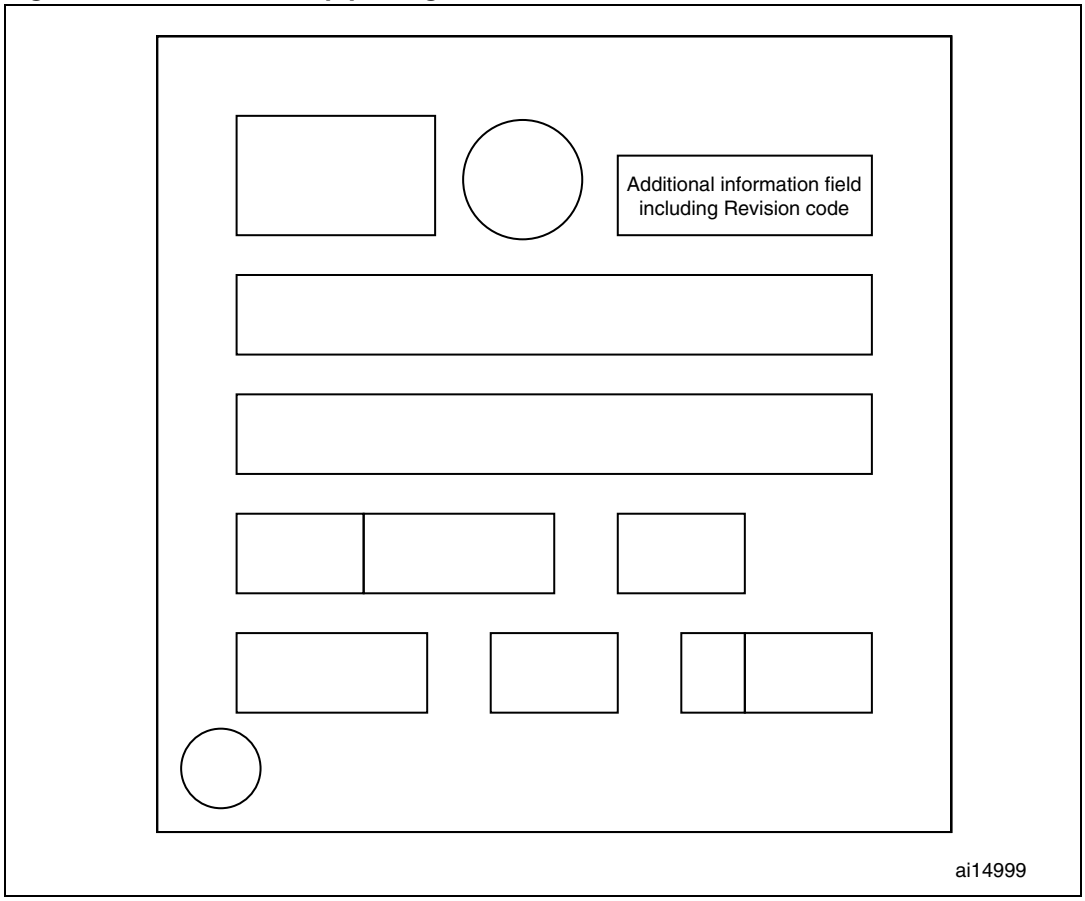


Figure 2. LFBGA100 top package view

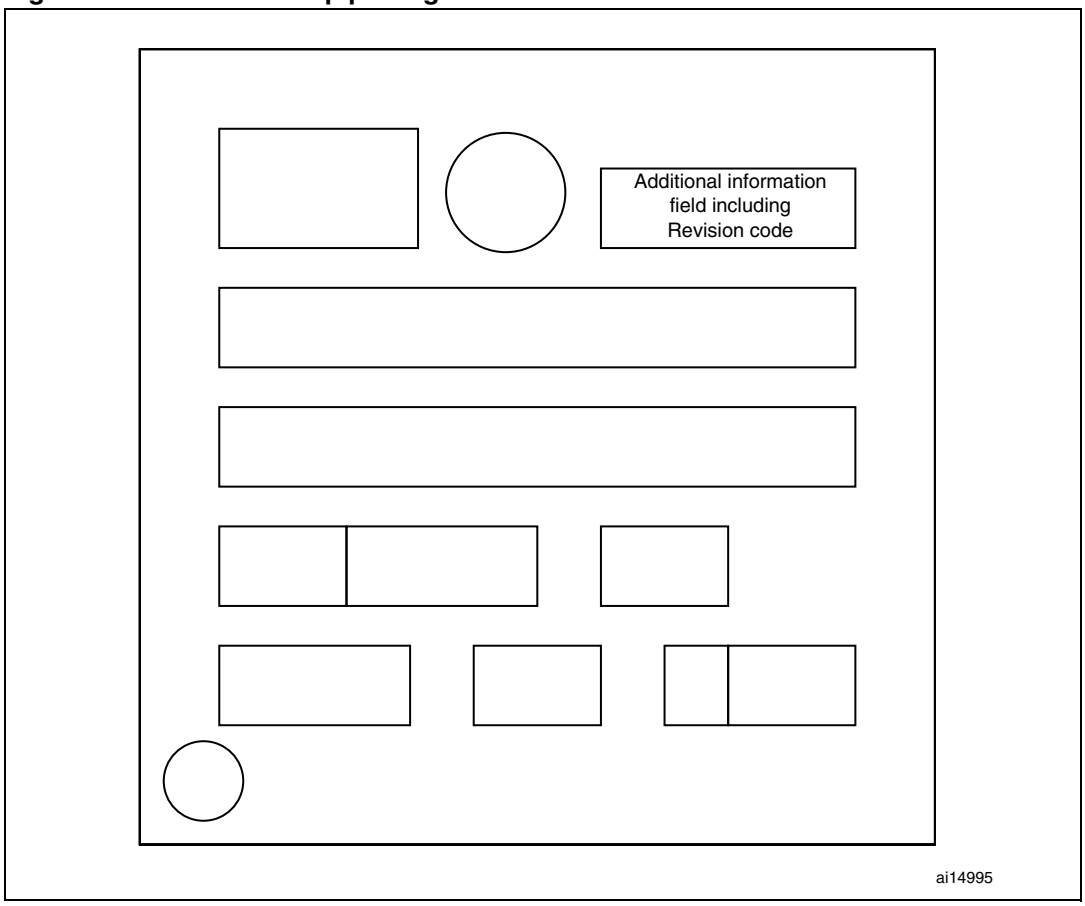


Figure 3. LQFP144 top package view

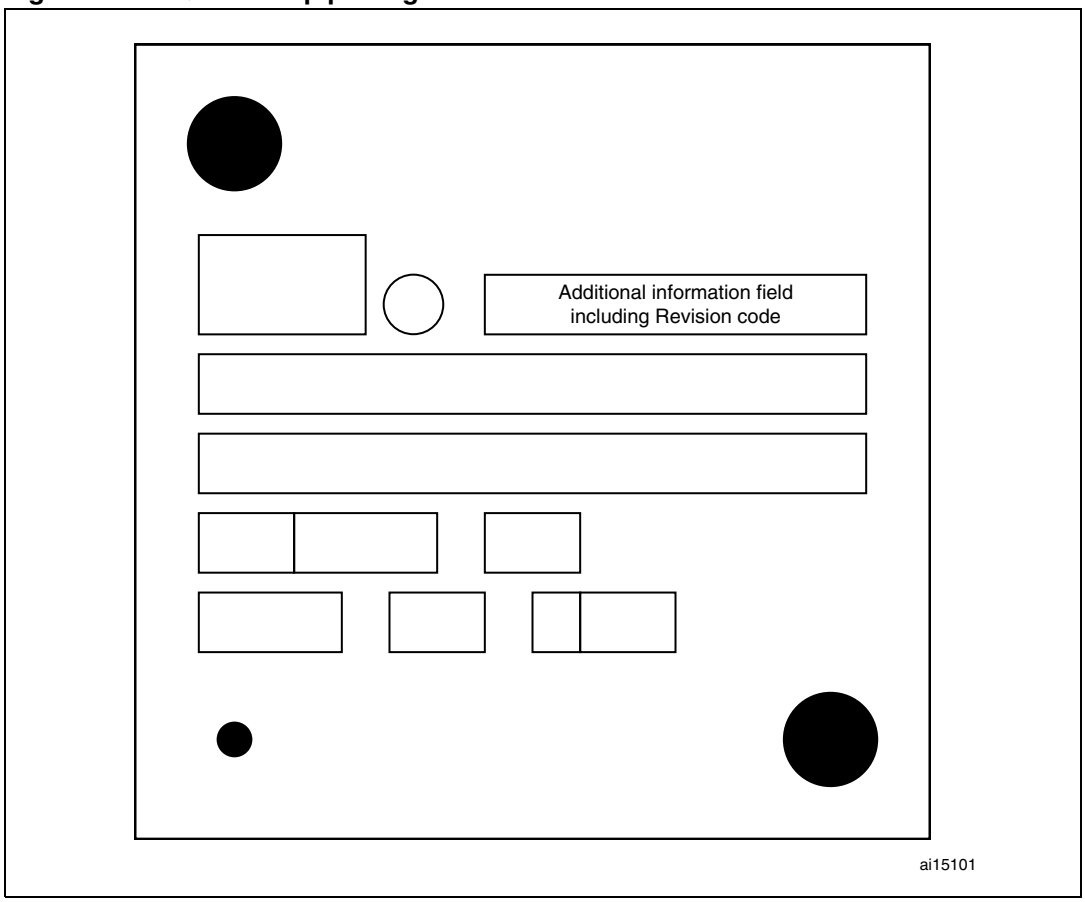


Figure 4. LQFP100 top package view

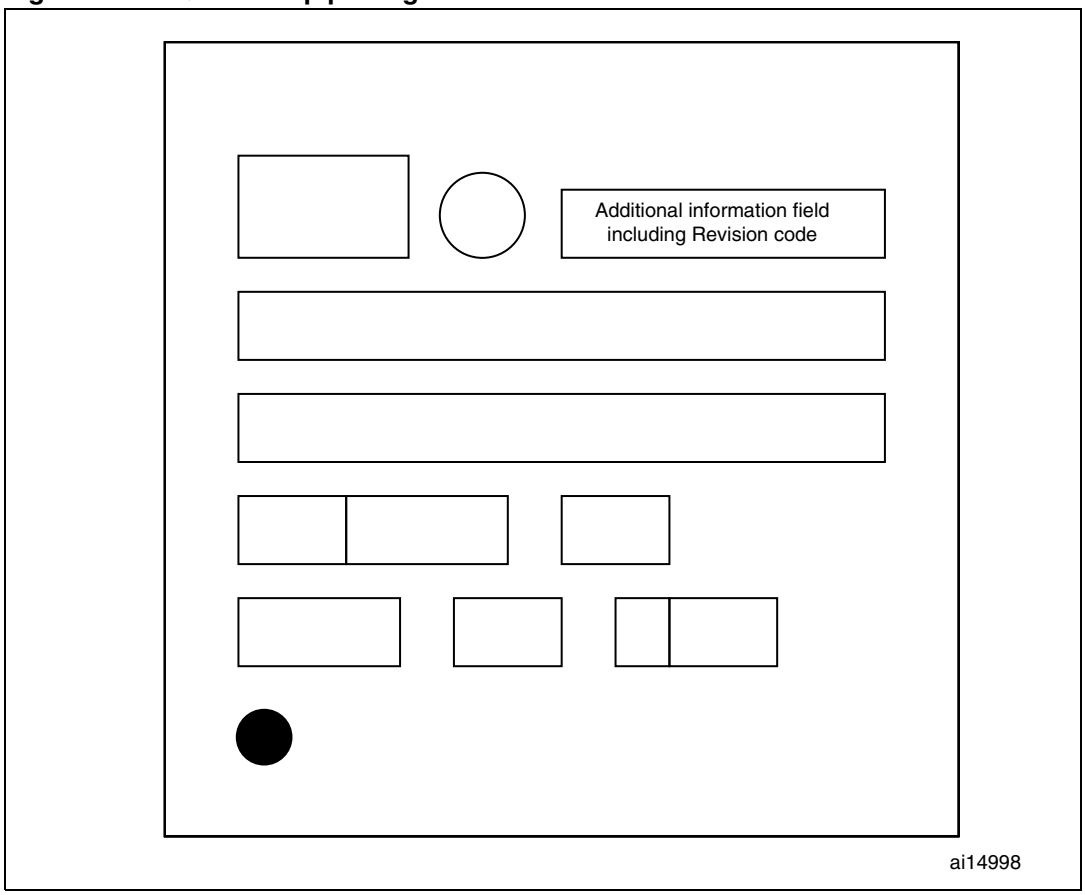
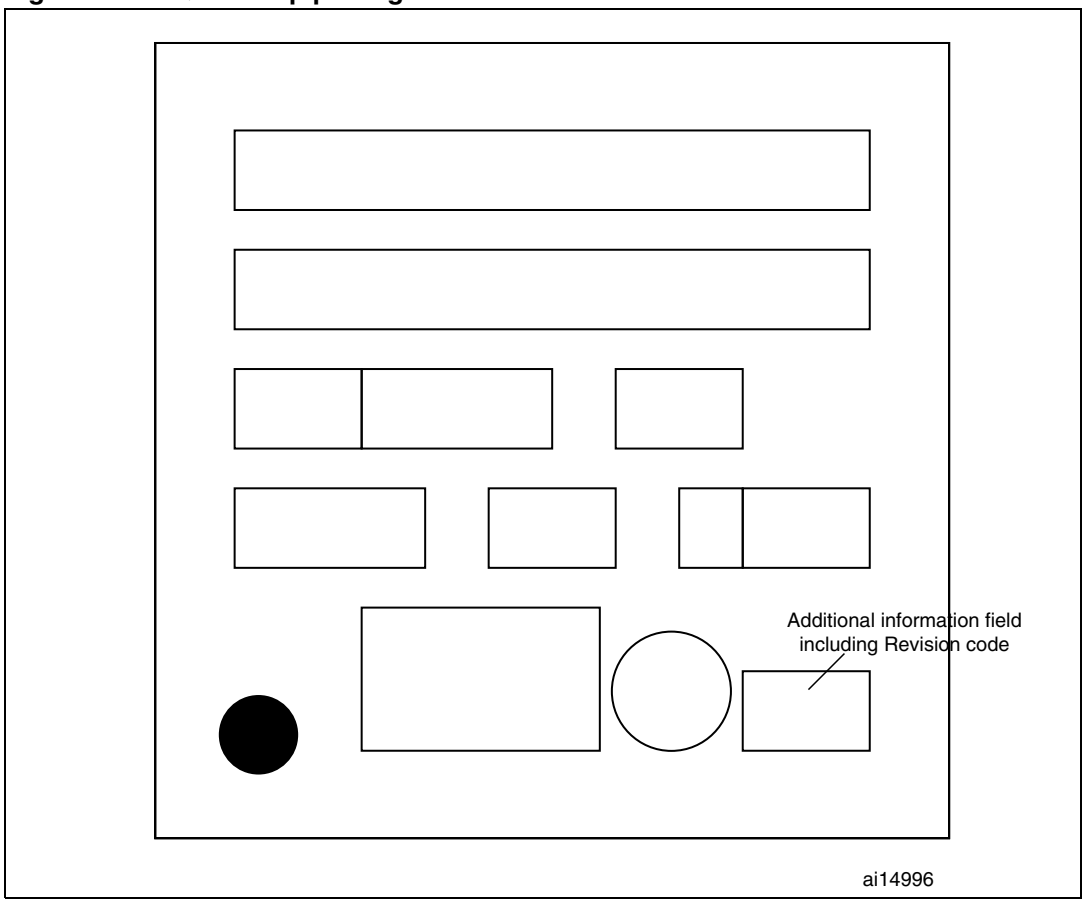


Figure 5. LQFP64 top package view



Revision history

Table 3. Document revision history

Date	Revision	Changes
23-May-2008	1	Initial release.

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