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1. System Overview

C8051F31x devices are fully integrated mixed-signal System-on-a-Chip MCUs. Highlighted features are listed below. Refer to Table 1.1 for specific product feature selection.

- High-speed pipelined 8051-compatible microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 10-bit 200 ksps 25-channel single-ended/differential ADC with analog multiplexer (C8051F310/1/2/3/6)
- Precision programmable 25 MHz internal oscillator
- 16 kB (C8051F310/1/6/7) or 8 kB (C8051F312/3/4/5) of on-chip Flash memory
- 1280 bytes of on-chip RAM
- SMBus/I2C, Enhanced UART, and Enhanced SPI serial interfaces implemented in hardware
- Four general-purpose 16-bit timers
- Programmable Counter/Timer Array (PCA) with five capture/compare modules and Watchdog Timer function
- On-chip Power-On Reset, V_{DD} Monitor, and Temperature Sensor
- On-chip Voltage Comparators (2)
- 29/25/21 Port I/O (5 V tolerant)

With on-chip Power-On Reset, V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F31x devices are truly stand-alone System-on-a-Chip solutions. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. User software has complete control of all peripherals, and may individually shut down any or all peripherals for power savings.

The on-chip Silicon Labs 2-Wire (C2) Development Interface allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using C2. The two C2 interface pins can be shared with user functions, allowing in-system programming and debugging without occupying package pins.

Each device is specified for 2.7-to-3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/O and $\overline{\text{RST}}$ pins are tolerant of input signals up to 5 V. The C8051F31x are available in 32-pin LQFP, 28-pin QFN, and 24-pin QFN packages. See Table 1.1 for ordering part numbers. Note: QFN packages are also referred to as MLP or MLF packages.

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	Calibrated Internal 24.5 MHz Oscillator	SMBus/I2C	Enhanced SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/Os	10-bit 200 ksps ADC	Temperature Sensor	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F310	25	16	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	-	LQFP-32
C8051F310-GQ	25	16	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	✓	LQFP-32
C8051F311	25	16	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	-	QFN-28
C8051F311-GM	25	16	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	✓	QFN-28
C8051F312	25	8	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	-	LQFP-32
C8051F312-GQ	25	8	1280	✓	✓	✓	✓	✓	✓	29	✓	✓	2	✓	LQFP-32
C8051F313	25	8	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	-	QFN-28
C8051F313-GM	25	8	1280	✓	✓	✓	✓	✓	✓	25	✓	✓	2	✓	QFN-28
C8051F314	25	8	1280	✓	✓	✓	✓	✓	✓	29	-	-	2	-	LQFP-32
C8051F314-GQ	25	8	1280	✓	✓	✓	✓	✓	✓	29	-	-	2	✓	LQFP-32
C8051F315	25	8	1280	✓	✓	✓	✓	✓	✓	25	-	-	2	-	QFN-28
C8051F315-GM	25	8	1280	✓	✓	✓	✓	✓	✓	25	-	-	2	✓	QFN-28
C8051F316-GM	25	16	1280	✓	✓	✓	✓	✓	✓	21	✓	✓	2	✓	QFN-24
C8051F317-GM	25	16	1280	✓	✓	✓	✓	✓	✓	21	-	-	2	✓	QFN-24

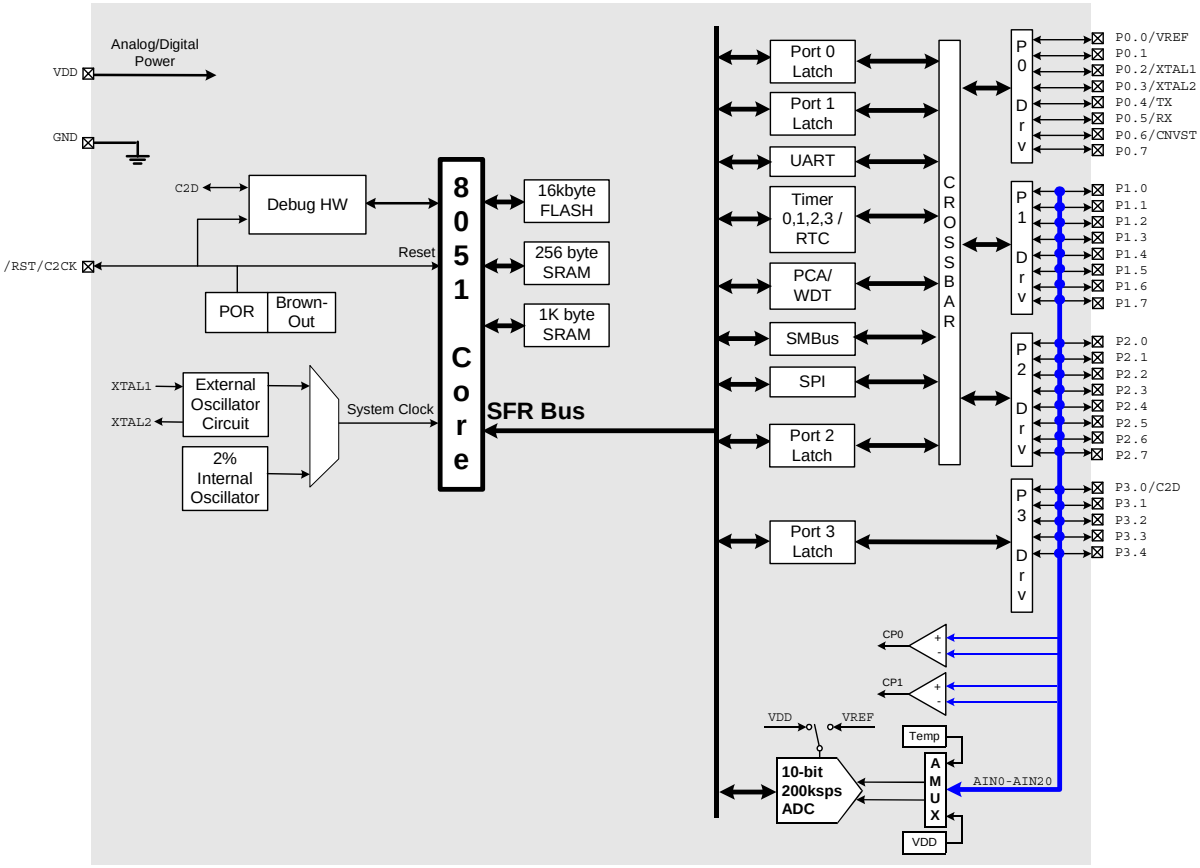

Figure 1.1. C8051F310 Block Diagram

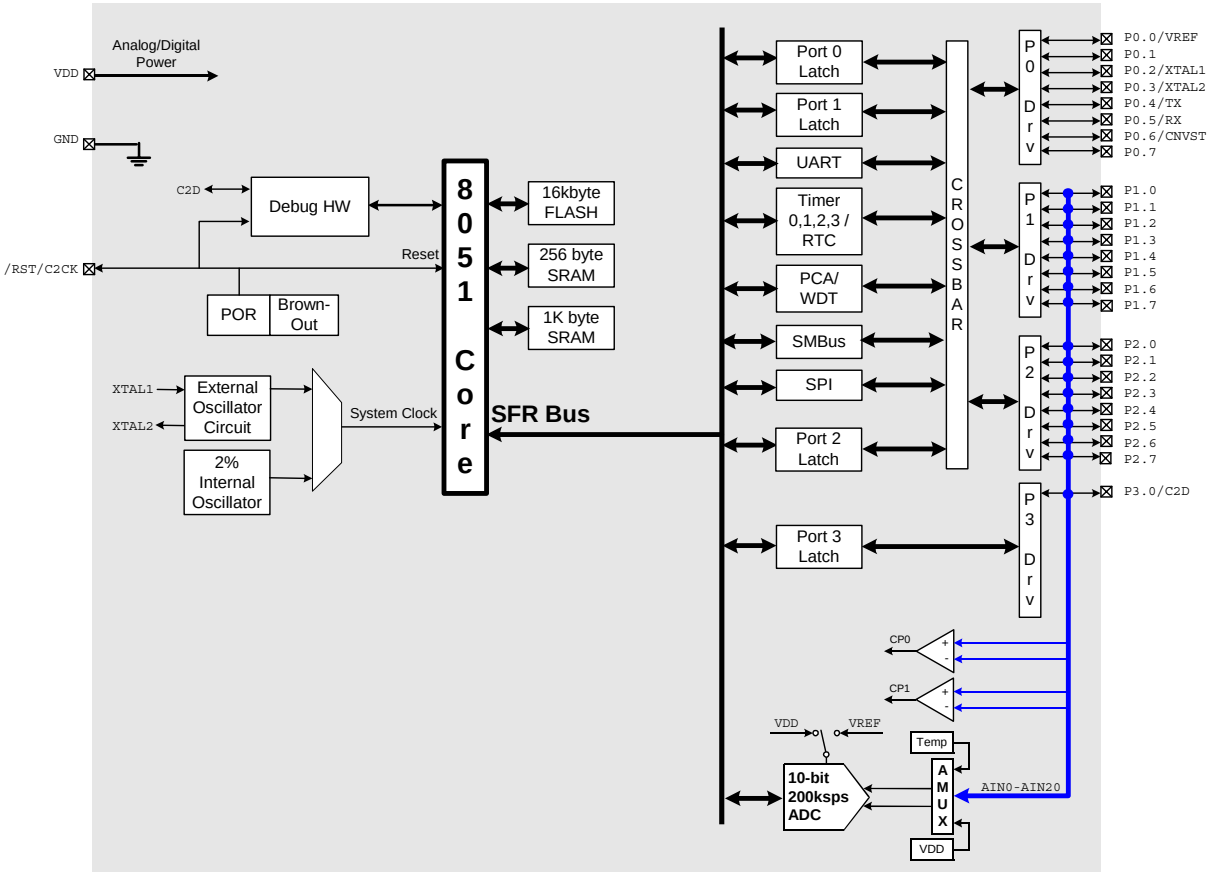

Figure 1.2. C8051F311 Block Diagram

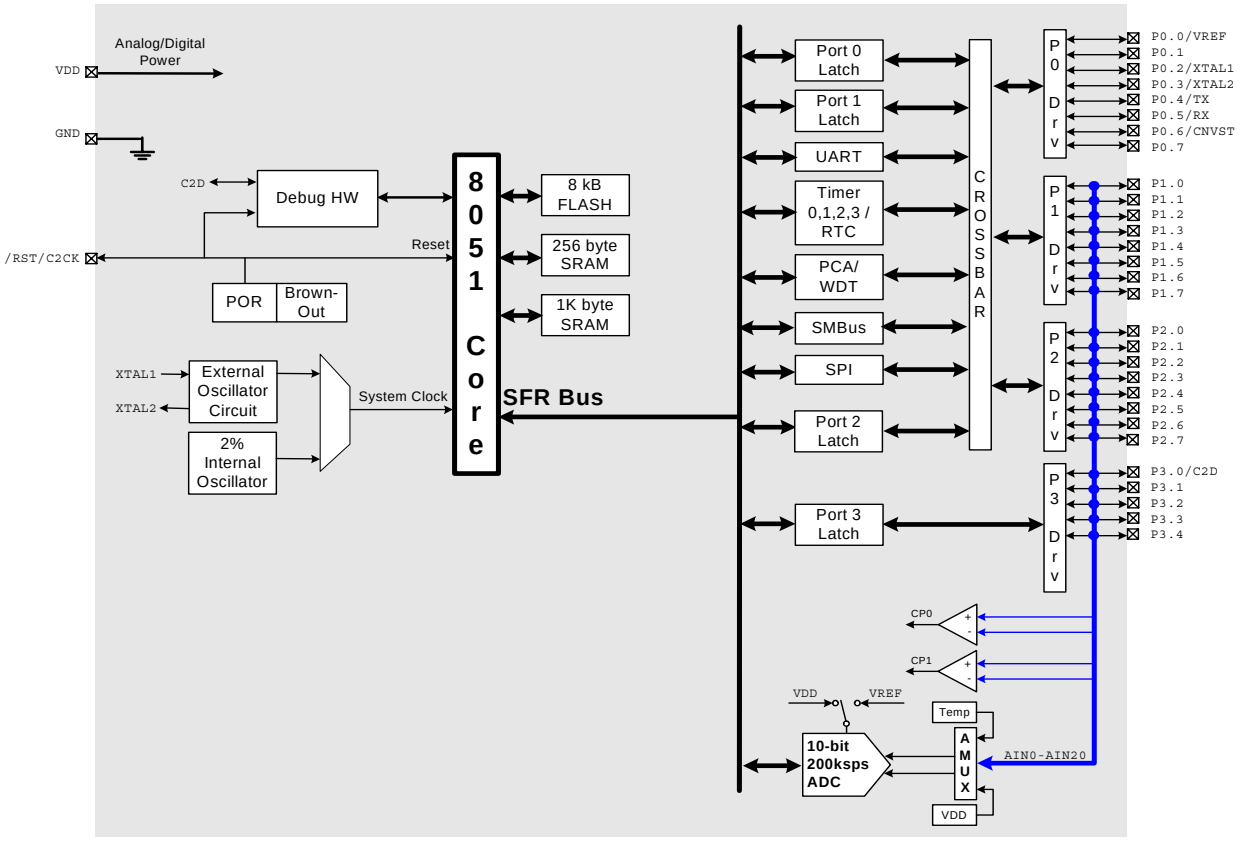

Figure 1.3. C8051F312 Block Diagram

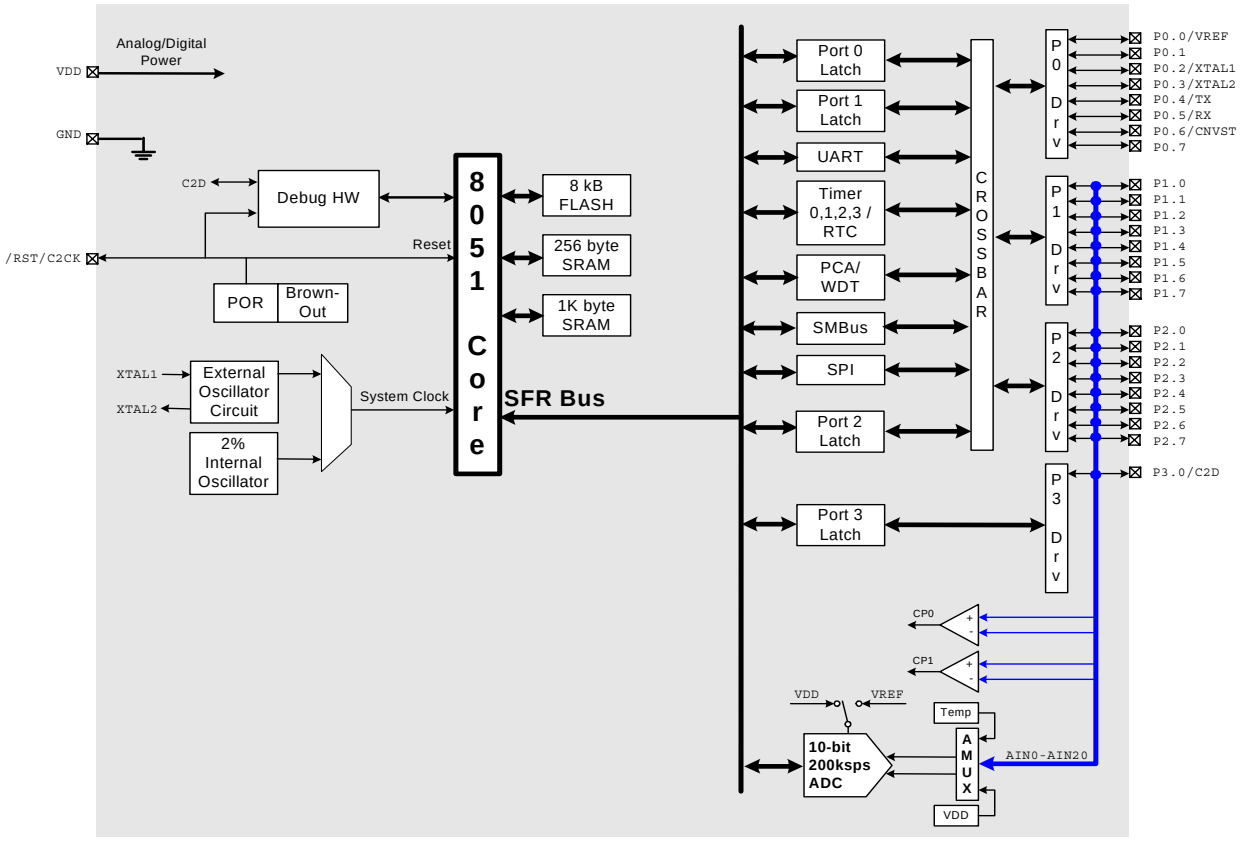

Figure 1.4. C8051F313 Block Diagram

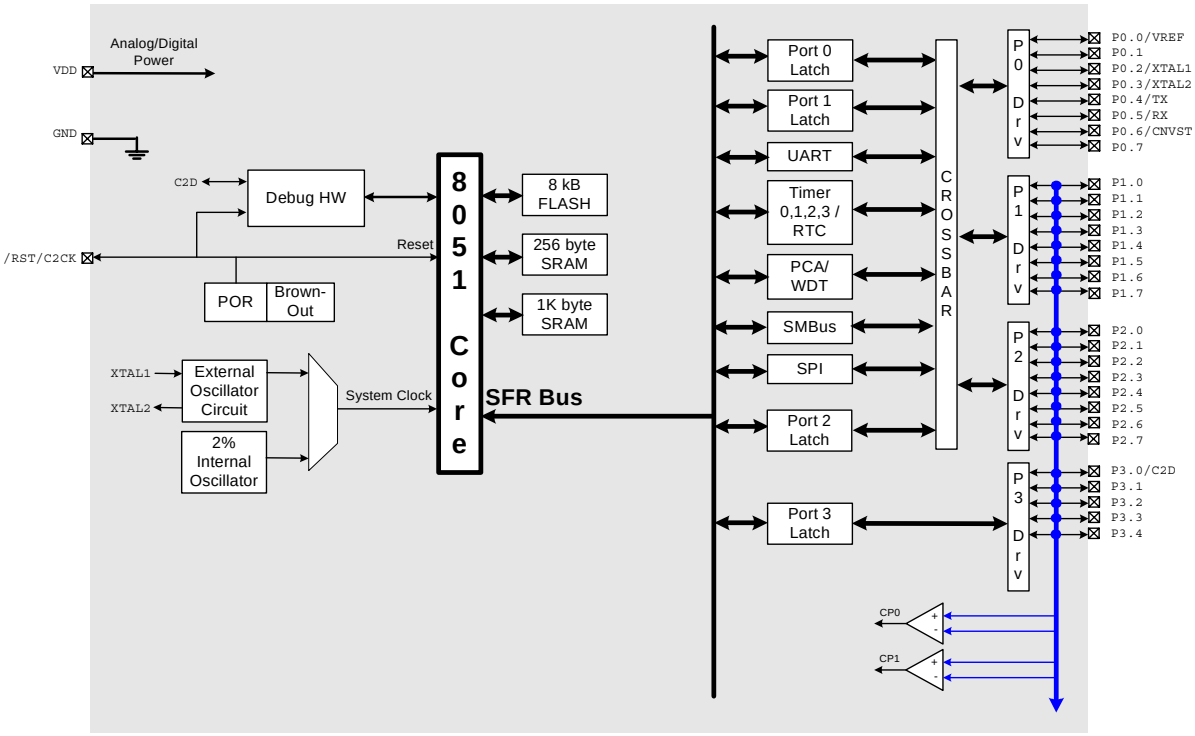

Figure 1.5. C8051F314 Block Diagram

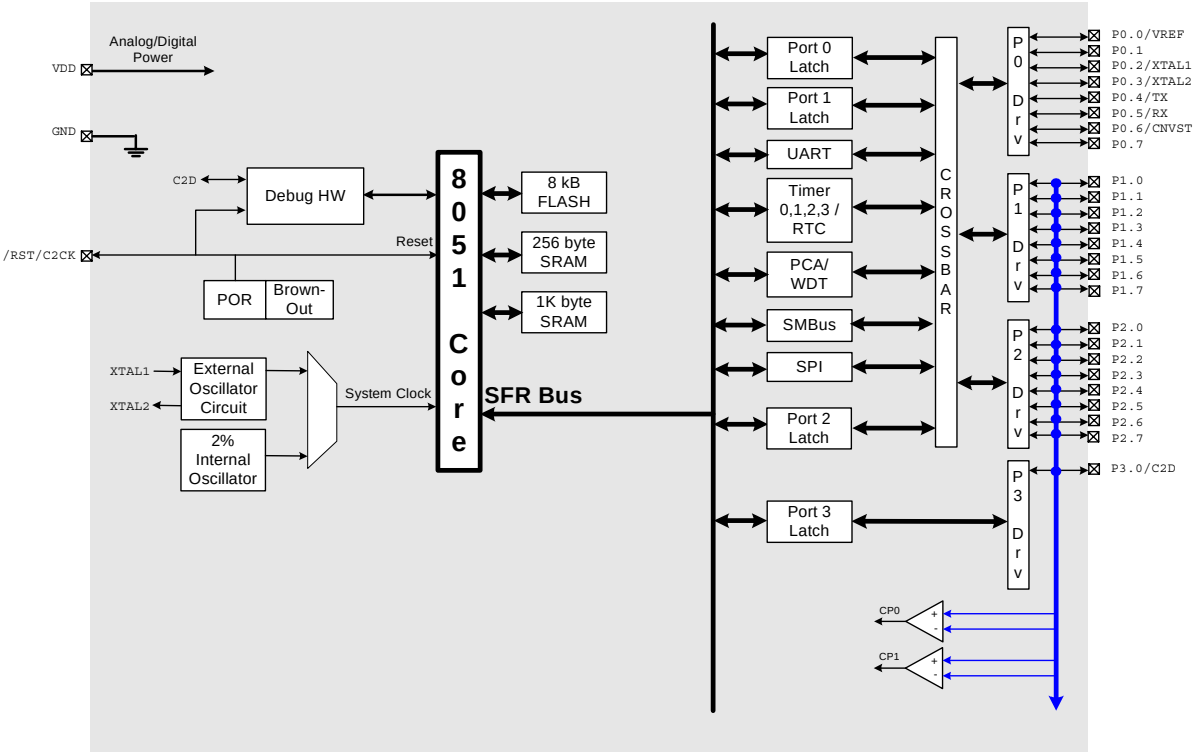

Figure 1.6. C8051F315 Block Diagram

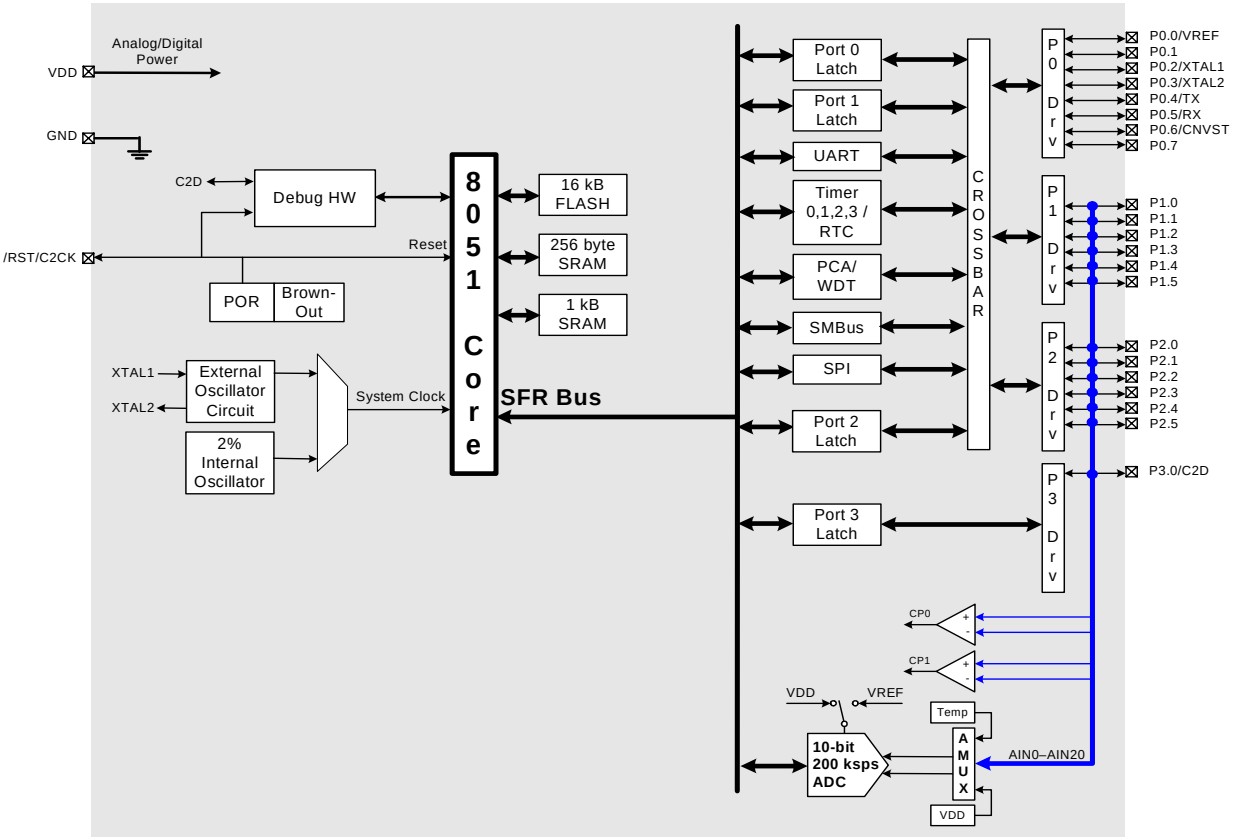

Figure 1.7. C8051F316 Block Diagram

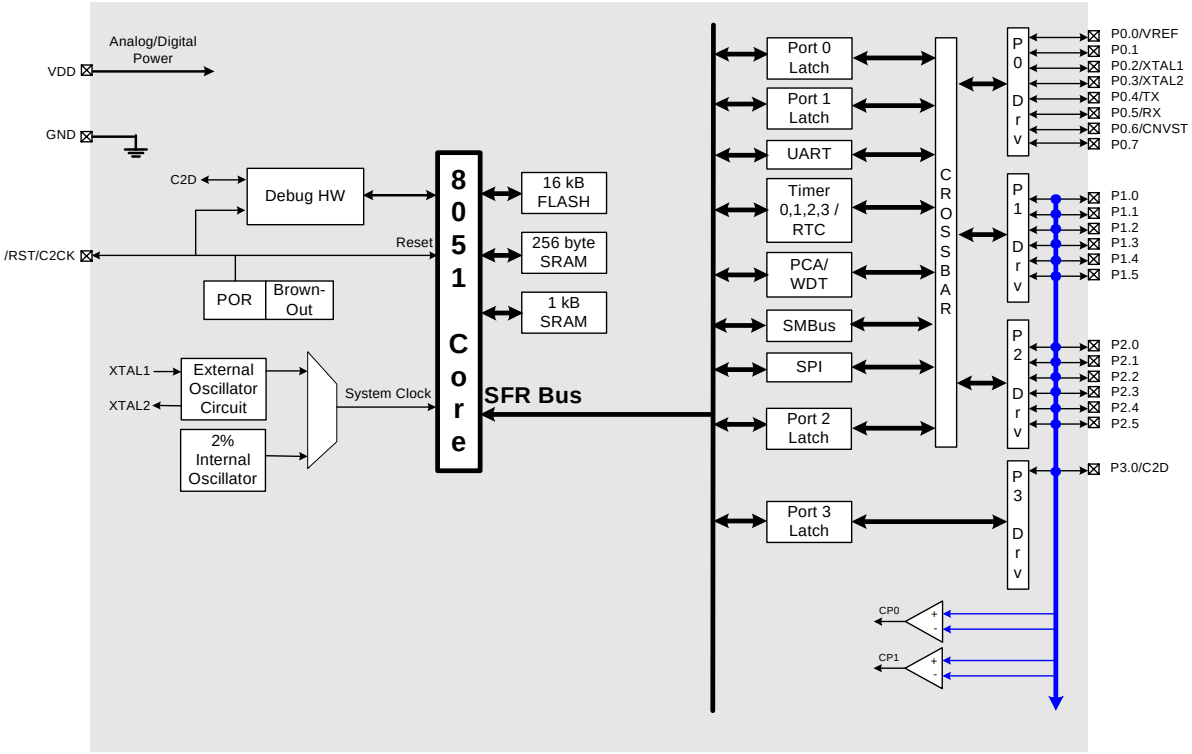

Figure 1.8. C8051F317 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F31x family utilizes Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052, including four 16-bit counter/timers, a full-duplex UART with extended baud rate configuration, an enhanced SPI port, 1280 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and 29/25/21 I/O pins.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.9 shows a comparison of peak throughputs for various 8-bit microcontroller cores with their maximum system clocks.

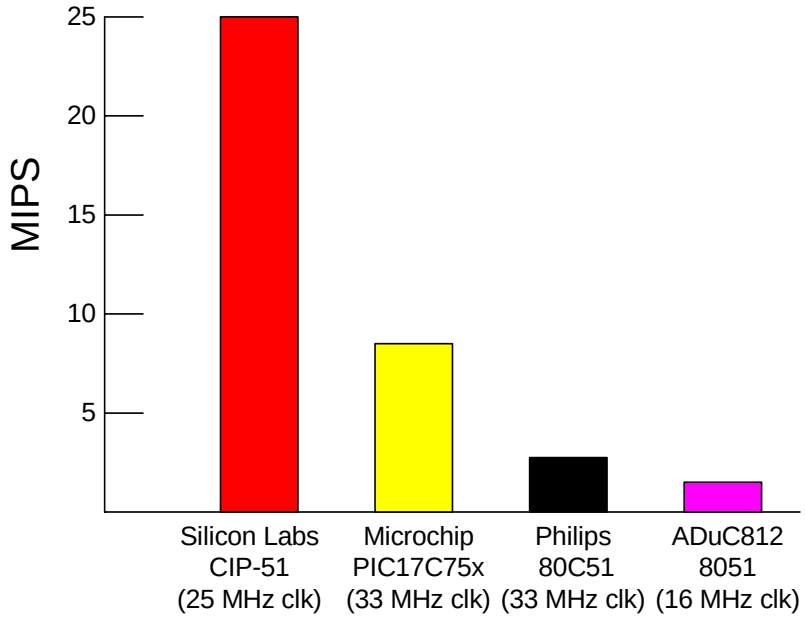

Figure 1.9. Comparison of Peak MCU Execution Speeds

1.1.3. Additional Features

The C8051F31x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 14 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 9.1 on page 110), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an errant Flash read/write protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator is factory calibrated to 24.5 MHz ±2%. An external oscillator drive circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between the internal and external oscillator circuits. An external oscillator can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast internal oscillator as needed.

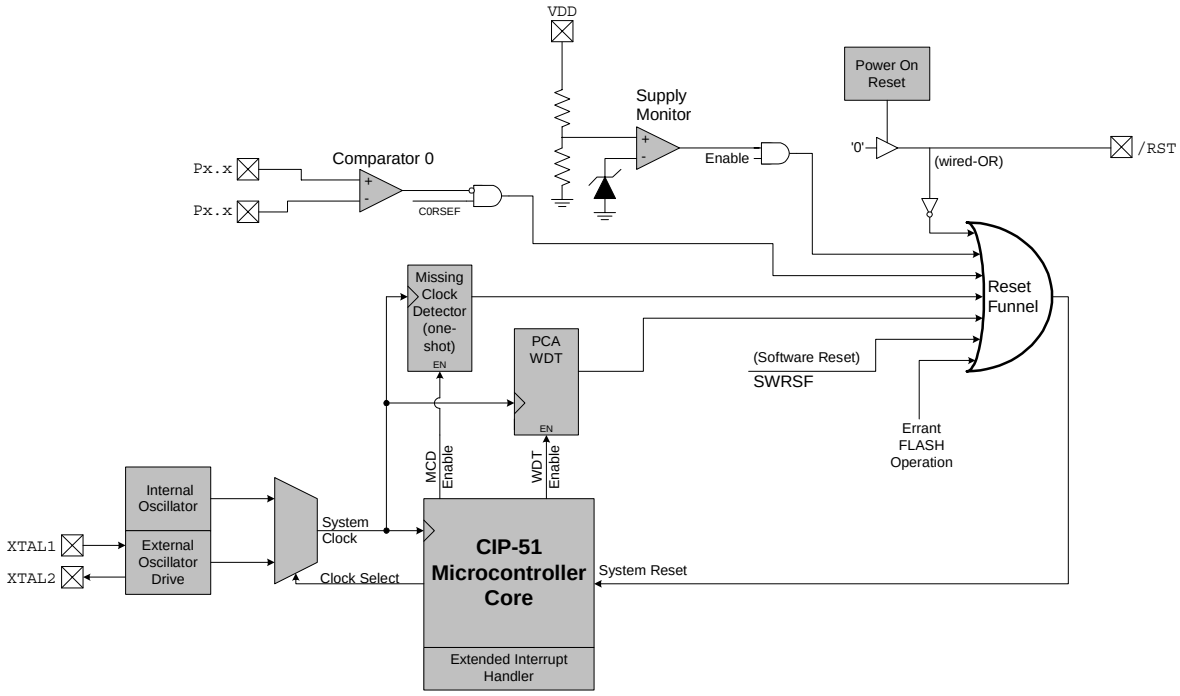

Figure 1.10. On-Chip Clock and Reset

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 8 or 16 kB of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. See Figure 1.11 for the MCU system memory map.

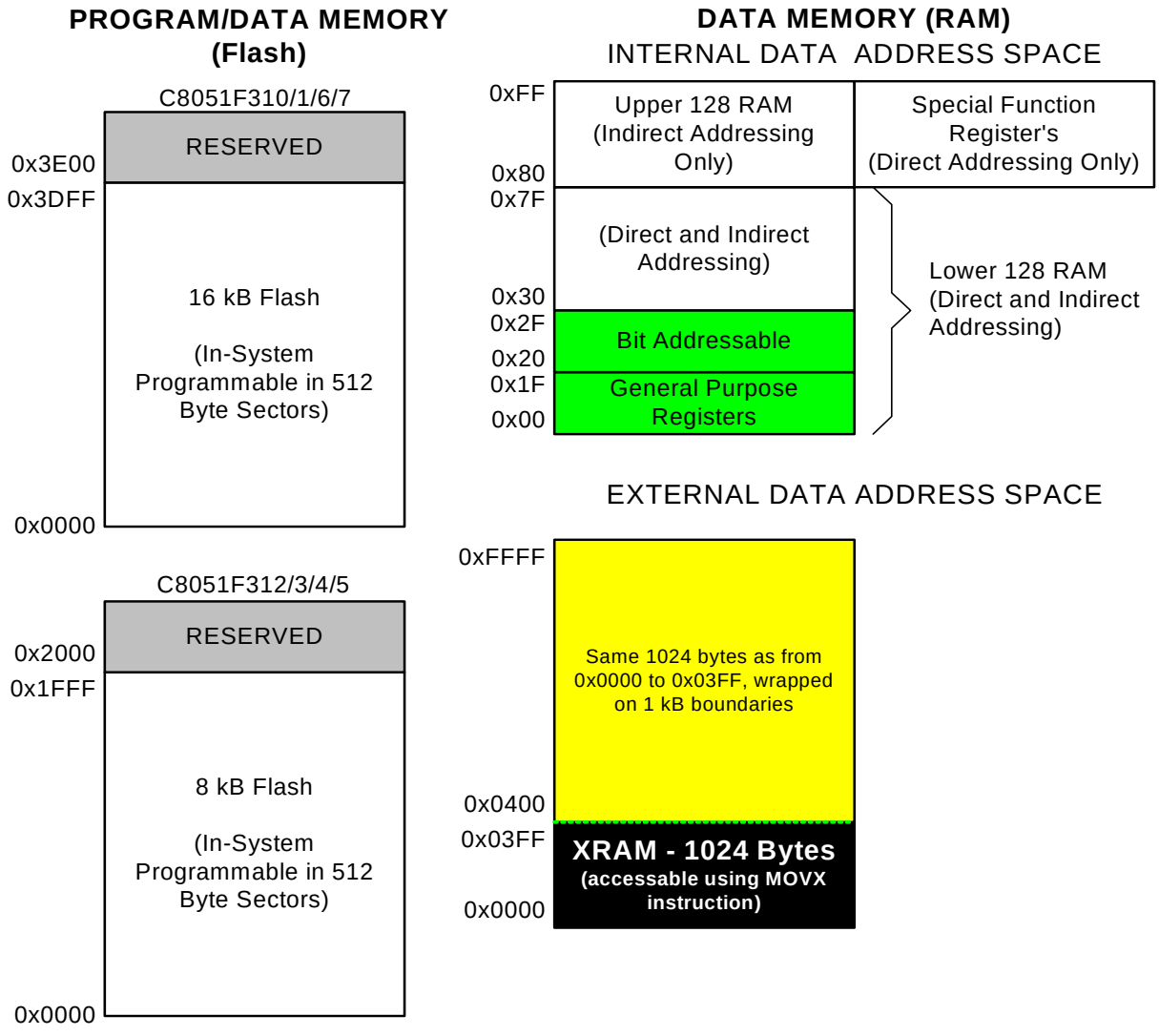

Figure 1.11. On-Board Memory Map

1.3. On-Chip Debug Circuitry

The C8051F31x devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F310DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F31x MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, a debug adapter, a target application board with the associated MCU installed, and the required cables and wall-mount power supply.

The Silicon Labs IDE interface is a vastly superior developing and debugging configuration, compared to standard MCU emulators that use on-board "ICE Chips" and require the MCU in the application board to be socketed. Silicon Labs' debug paradigm increases ease of use and preserves the performance of the precision analog peripherals.

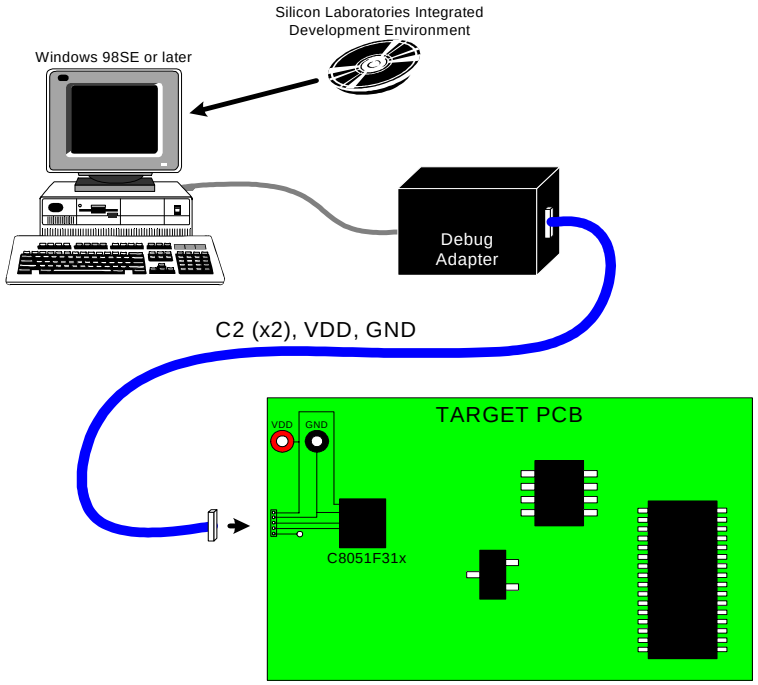

Figure 1.12. Development/In-System Debug Diagram

1.4. Programmable Digital I/O and Crossbar

C8051F310/2/4 devices include 29 I/O pins (three byte-wide Ports and one 5-bit-wide Port); C8051F311/3/5 devices include 25 I/O pins (three byte-wide Ports and one 1-bit-wide Port); C8051F316/7 devices include 21 I/O pins (one byte-wide Port, two 6-bit-wide Ports and one 1-bit-wide Port). The C8051F31x Ports behave like typical 8051 Ports with a few enhancements. Each Port pin may be configured as an analog input or a digital I/O pin. Pins selected as digital I/Os may additionally be configured for push-pull or open-drain output. The “weak pullups” that are fixed on typical 8051 devices may be globally disabled, providing power savings capabilities.

The Digital Crossbar allows mapping of internal digital system resources to Port I/O pins (See Figure 1.13). On-chip counter/timers, serial buses, HW interrupts, comparator output, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

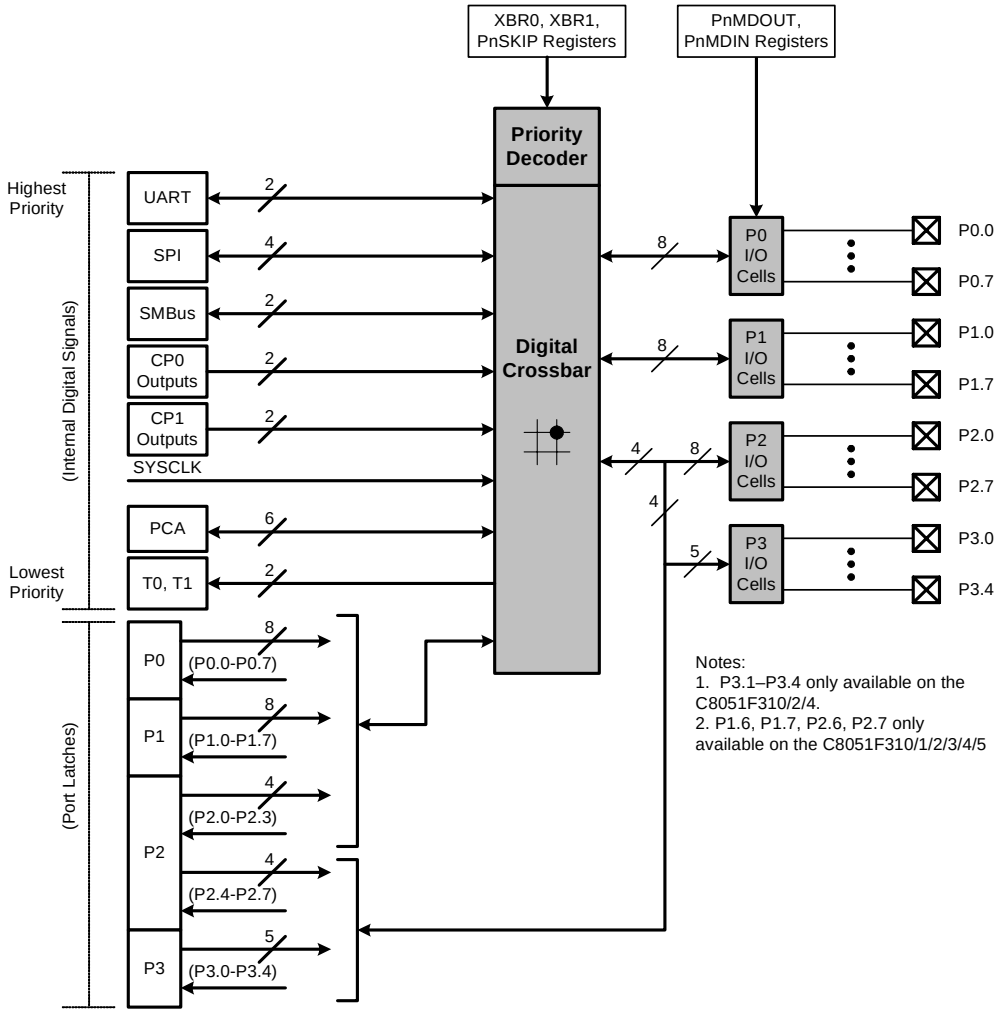

Figure 1.13. Digital Crossbar Diagram

1.5. Serial Ports

The C8051F31x Family includes an SMBus/I2C interface, a full-duplex UART with enhanced baud rate configuration, and an Enhanced SPI interface. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little CPU intervention.

1.6. Programmable Counter Array

An on-chip Programmable Counter/Timer Array (PCA) is included in addition to the four 16-bit general purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer time base with five programmable capture/compare modules. The PCA clock is derived from one of six sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflows, an External Clock Input (ECI), the system clock, or the external oscillator clock source divided by 8. The external clock source selection is useful for real-time clock functionality, where the PCA is clocked by an external source while the internal oscillator drives the system clock.

Each capture/compare module can be configured to operate in one of six modes: Edge-Triggered Capture, Software Timer, High Speed Output, 8- or 16-bit Pulse Width Modulator, or Frequency Output. Additionally, Capture/Compare Module 4 offers watchdog timer (WDT) capabilities. Following a system reset, Module 4 is configured and enabled in WDT mode. The PCA Capture/Compare Module I/O and External Clock Input may be routed to Port I/O via the Digital Crossbar.

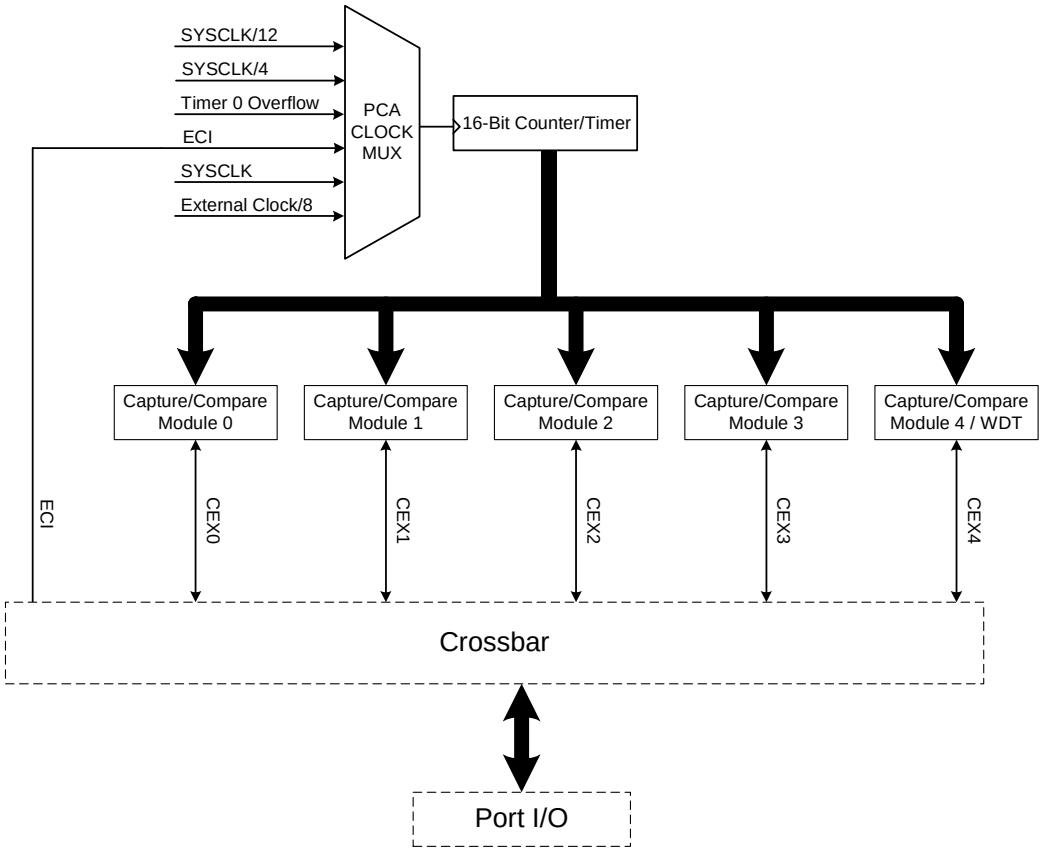

Figure 1.14. PCA Block Diagram

1.7. 10-Bit Analog to Digital Converter

The C8051F310/1/2/3/6 devices include an on-chip 10-bit SAR ADC with a 25-channel differential input multiplexer. With a maximum throughput of 200 ksps, the ADC offers true 10-bit accuracy with an INL of ±1LSB. The ADC system includes a configurable analog multiplexer that selects both positive and negative ADC inputs. Ports1-3 are available as an ADC inputs; additionally, the on-chip Temperature Sensor output and the power supply voltage (V_{DD}) are available as ADC inputs. User firmware may shut down the ADC to save power.

Conversions can be started in six ways: a software command, an overflow of Timer 0, 1, 2, or 3, or an external convert start signal. This flexibility allows the start of conversion to be triggered by software events, a periodic signal (timer overflows), or external HW signals. Conversion completions are indicated by a status bit and an interrupt (if enabled). The resulting 10-bit data word is latched into the ADC data SFRs upon completion of a conversion.

Window compare registers for the ADC data can be configured to interrupt the controller when ADC data is either within or outside of a specified range. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within/outside the specified range.

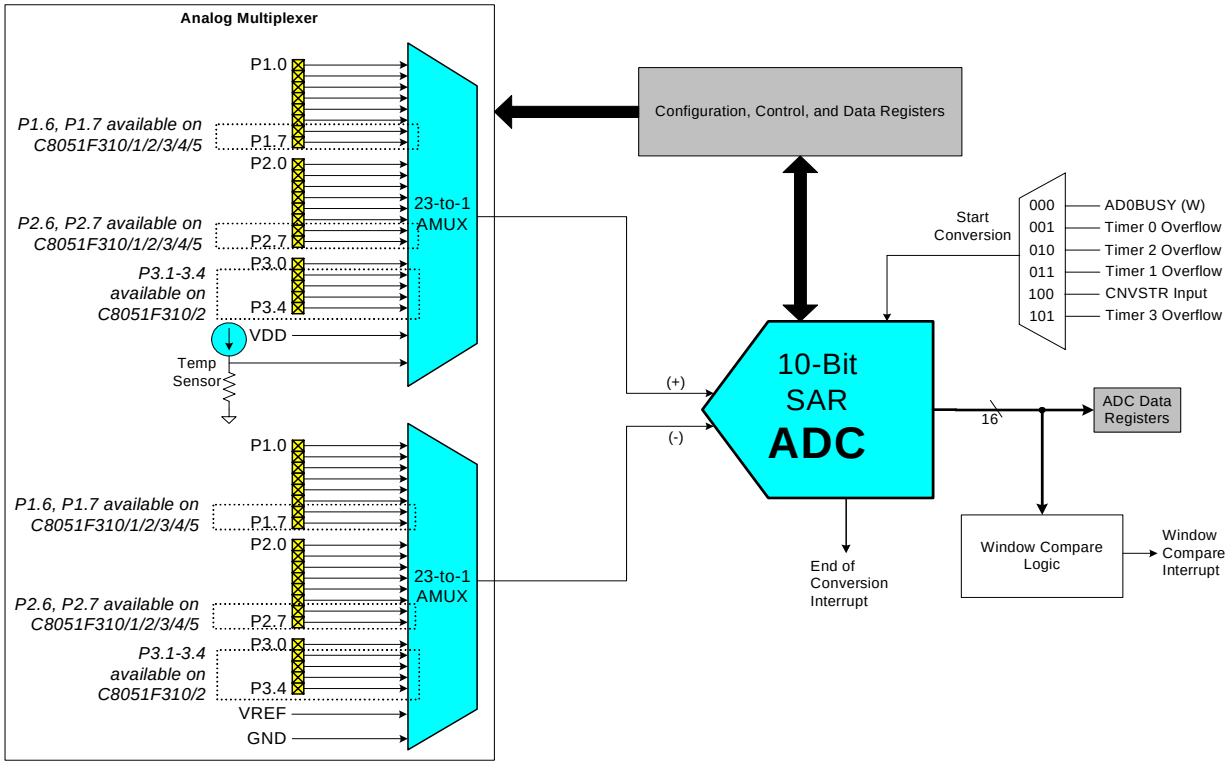

Figure 1.15. 10-Bit ADC Block Diagram

1.8. Comparators

C8051F31x devices include two on-chip voltage comparators that are enabled/disabled and configured via user software. Port I/O pins may be configured as comparator inputs via a selection mux. Two comparator outputs may be routed to a Port pin if desired: a latched output and/or an unlatched (asynchronous) output. Comparator response time is programmable, allowing the user to select between high-speed and low-power modes. Positive and negative hysteresis are also configurable.

Comparator interrupts may be generated on rising, falling, or both edges. When in IDLE mode, these interrupts may be used as a “wake-up” source. Comparator0 may also be configured as a reset source. Figure 1.16 shows he Comparator0 block diagram.

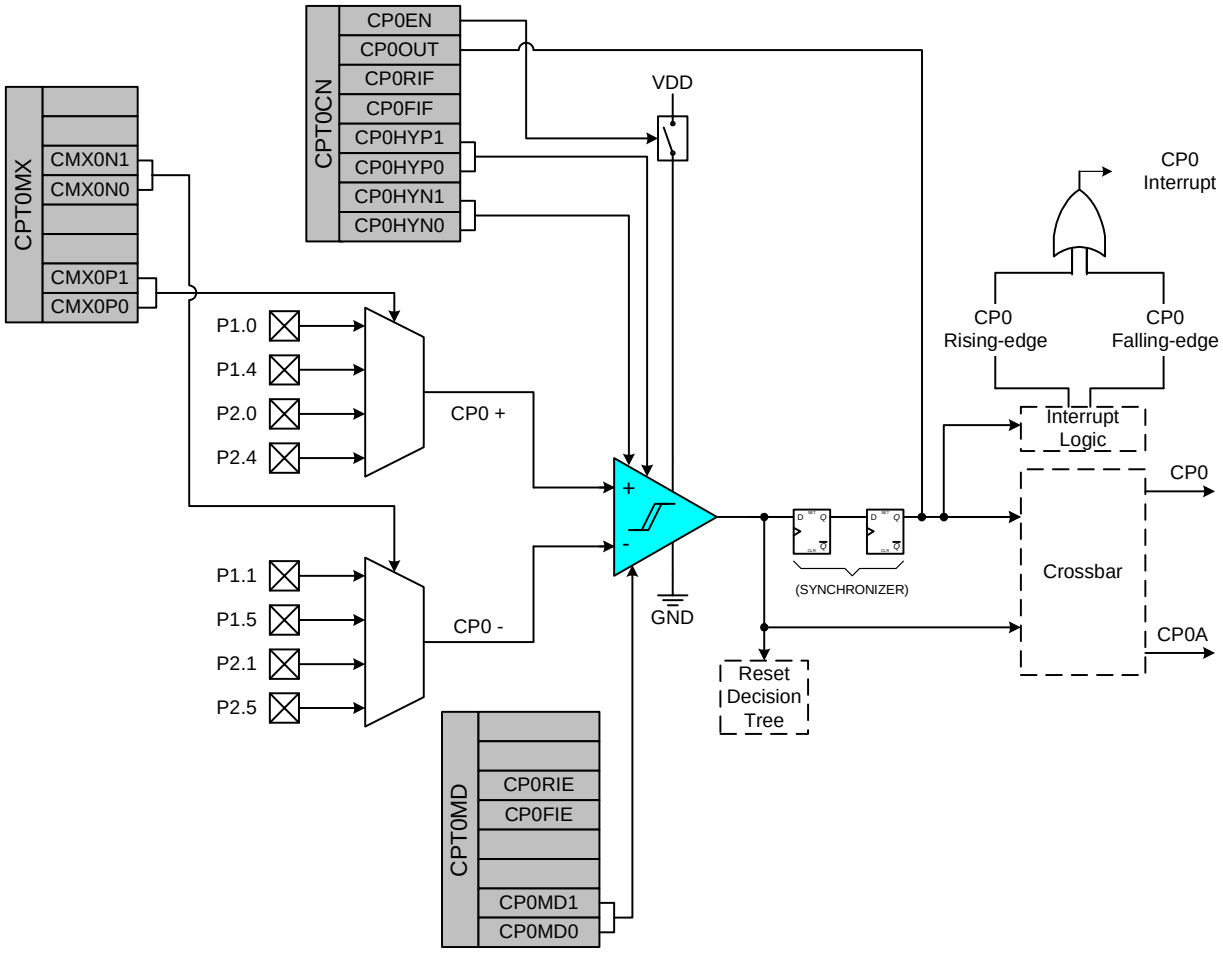

Figure 1.16. Comparator0 Block Diagram

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Port I/O Pin or $\overline{\text{RST}}$ with respect to GND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to GND		–0.3	—	4.2	V
Maximum Total current through V_{DD} and GND		—	—	500	mA
Maximum output current sunk by $\overline{\text{RST}}$ or any Port pin		—	—	100	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40°C to +85°C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Voltage		V_{RST}[1]	3.0	3.6	V
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
Specified Operating Temperature Range		–40	—	+85	°C
SYSCLK (system clock frequency)		0[2]	—	25	MHz
Tsysl (SYSCLK low time)		18	—	—	ns
Tsysh (SYSCLK high time)		18	—	—	ns
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD} (Note 3)	V_{DD} = 3.0 V, F = 25 MHz	—	7.8	8.6	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.38	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	31	—	µA
	V_{DD} = 3.6 V, F = 25 MHz	—	10.7	12.1	mA
I_{DD} Supply Sensitivity (Note 3, Note 4)	F = 25 MHz	—	67	—	%/V
	F = 1 MHz	—	62	—	%/V
I_{DD} Frequency Sensitivity (Note 3, Note 5)	V_{DD} = 3.0 V, F ≤ 15 MHz, T = 25 ºC	—	0.39	—	mA/MHz
	V_{DD} = 3.0 V, F > 15 MHz, T = 25 ºC	—	0.21	—	mA/MHz
	V_{DD} = 3.6 V, F ≤ 15 MHz, T = 25 ºC	—	0.55	—	mA/MHz
	V_{DD} = 3.6 V, F > 15 MHz, T = 25 ºC	—	0.27	—	mA/MHz

Notes:

1. Given in Table 9.1 on page 110.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization data, not production tested.
4. Active and Inactive I_{DD} at voltages and frequencies other than those specified can be calculated using the I_{DD} Supply Sensitivity. For example, if the V_{DD} is 3.3 V instead of 3.0 V at 25 MHz: I_{DD} = 7.8 mA typical at 3.0 V and f = 25 MHz. From this, I_{DD} = 7.8 mA + 0.67 x (3.3 V – 3.0 V) = 8 mA at 3.3 V and f = 25 MHz.
5. I_{DD} can be estimated for frequencies ≤ 15 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} for > 15 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example:
   V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 7.8 mA – (25 MHz – 20 MHz) x 0.21 mA/MHz = 6.75 mA.
6. Idle I_{DD} can be estimated for frequencies ≤ 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate Idle I_{DD} for > 1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example:
   V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 4.8 mA – (25 MHz – 5 MHz) x 0.15 mA/MHz = 1.8 mA.

Table 3.1. Global DC Electrical Characteristics (Continued)

–40°C to +85°C, 25 MHz System Clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
I_{DD} (Note 3)	V_{DD} = 3.0 V, F = 25 MHz	—	3.8	4.3	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.20	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	16	—	µA
	V_{DD} = 3.6 V, F = 25 MHz	—	4.8	5.3	mA
I_{DD} Supply Sensitivity (Note 3, Note 4)	F = 25 MHz	—	44	—	%/V
	F = 1 MHz	—	56	—	%/V
I_{DD} Frequency Sensitivity (Note 3, Note 6)	V_{DD} = 3.0 V, F ≤ 1 MHz, T = 25 °C	—	0.21	—	mA/MHz
	V_{DD} = 3.0 V, F > 1 MHz, T = 25 °C	—	0.15	—	mA/MHz
	V_{DD} = 3.6 V, F ≤ 1 MHz, T = 25 °C	—	0.28	—	mA/MHz
	V_{DD} = 3.6 V, F > 1 MHz, T = 25 °C	—	0.19	—	mA/MHz
Digital Supply Current (Stop Mode, shutdown)	Oscillator not running, V_{DD} Monitor Disabled	—	< 0.1	—	µA

Notes:

1. Given in Table 9.1 on page 110.
2. SYSCLK must be at least 32 kHz to enable debugging.
3. Based on device characterization data, not production tested.
4. Active and Inactive I_{DD} at voltages and frequencies other than those specified can be calculated using the I_{DD} Supply Sensitivity. For example, if the V_{DD} is 3.3 V instead of 3.0 V at 25 MHz: I_{DD} = 7.8 mA typical at 3.0 V and f = 25 MHz. From this, I_{DD} = 7.8 mA + 0.67 x (3.3 V – 3.0 V) = 8 mA at 3.3 V and f = 25 MHz.
5. I_{DD} can be estimated for frequencies ≤ 15 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} for > 15 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example:
   V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 7.8 mA – (25 MHz – 20 MHz) x 0.21 mA/MHz = 6.75 mA.
6. Idle I_{DD} can be estimated for frequencies ≤ 1 MHz by multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate Idle I_{DD} for > 1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example:
   V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 4.8 mA – (25 MHz – 5 MHz) x 0.15 mA/MHz = 1.8 mA.

Other electrical characteristics tables are found in the data sheet section corresponding to the associated peripherals. For more information on electrical characteristics for a specific peripheral, refer to the page indicated in Table 3.2.

Table 3.2. Electrical Characteristics Quick Reference

Peripheral Electrical Characteristics	Page No.
ADC0 Electrical Characteristics	65
External Voltage Reference Circuit Electrical Characteristics	68
Comparator Electrical Characteristics	78
Reset Electrical Characteristics	110
Flash Electrical Characteristics	112
Internal Oscillator Electrical Characteristics	123
Port I/O DC Electrical Characteristics	143

4. Pinout and Package Definitions

Table 4.1. Pin Definitions for the C8051F31x

Name	Pin Numbers			Type	Description
	‘F310/2/4	‘F311/3/5	‘F316/7		
V_{DD}	4	4	4		Power Supply Voltage.
GND	3	3	3		Ground.
RST/ C2CK	5	5	5	D I/O D I/O	Device Reset. Open-drain output of internal POR. An external source can initiate a system reset by driving this pin low for at least 10 µs. Clock signal for the C2 Debug Interface.
P3.0/ C2D	6	6	6	D I/O D I/O	Port 3.0. See **Section 13** for a complete description. Bi-directional data signal for the C2 Debug Interface.
P0.0/ VREF	2	2	2	D I/O A In	Port 0.0. See **Section 13** for a complete description. External VREF input. (‘F310/1/2/3 only)
P0.1	1	1	1	D I/O	Port 0.1. See **Section 13** for a complete description.
P0.2/ XTAL1	32	28	24	D I/O A In	Port 0.2. See **Section 13** for a complete description. External Clock Input. This pin is the external oscillator return for a crystal or resonator.
P0.3/ XTAL2	31	27	23	D I/O A Out or D In	Port 0.3. See **Section 13** for a complete description. External Clock Output. For an external crystal or resonator, this pin is the excitation driver. This pin is the external clock input for CMOS, capacitor, or RC oscillator configurations.
P0.4	30	26	22	D I/O	Port 0.4. See **Section 13** for a complete description.
P0.5	29	25	21	D I/O	Port 0.5. See **Section 13** for a complete description.
P0.6/ CNVSTR	28	24	20		Port 0.6. See **Section 13** for a complete description. ADC0 External Convert Start Input. (‘F310/1/2/3 only)
P0.7	27	23	19	D I/O	Port 0.7. See **Section 13** for a complete description.
P1.0	26	22	18	D I/O or A In	Port 1.0. See **Section 13** for a complete description.
P1.1	25	21	17	D I/O or A In	Port 1.1. See **Section 13** for a complete description.
P1.2	24	20	16	D I/O or A In	Port 1.2. See **Section 13** for a complete description.
P1.3	23	19	15	D I/O or A In	Port 1.3. See **Section 13** for a complete description.
P1.4	22	18	14	D I/O or A In	Port 1.4. See **Section 13** for a complete description.

Table 4.1. Pin Definitions for the C8051F31x (Continued)

Name	Pin Numbers			Type	Description
	'F310/2/4	'F311/3/5	'F316/7		
P1.5	21	17	13	D I/O or A In	Port 1.5. See **Section 13** for a complete description.
P1.6	20	16		D I/O or A In	Port 1.6. See **Section 13** for a complete description.
P1.7	19	15		D I/O or A In	Port 1.7. See **Section 13** for a complete description.
P2.0	18	14	12	D I/O or A In	Port 2.0. See **Section 13** for a complete description.
P2.1	17	13	11	D I/O or A In	Port 2.1. See **Section 13** for a complete description.
P2.2	16	12	10	D I/O or A In	Port 2.2. See **Section 13** for a complete description.
P2.3	15	11	9	D I/O or A In	Port 2.3. See **Section 13** for a complete description.
P2.4	14	10	8	D I/O or A In	Port 2.4. See **Section 13** for a complete description.
P2.5	13	9	7	D I/O or A In	Port 2.5. See **Section 13** for a complete description.
P2.6	12	8		D I/O or A In	Port 2.6. See **Section 13** for a complete description.
P2.7	11	7		D I/O or A In	Port 2.7. See **Section 13** for a complete description.
P3.1	7			D I/O or A In	Port 3.1. See **Section 13** for a complete description.
P3.2	8			D I/O or A In	Port 3.2. See **Section 13** for a complete description.
P3.3	9			D I/O or A In	Port 3.3. See **Section 13** for a complete description.
P3.4	10			D I/O or A In	Port 3.4. See **Section 13** for a complete description.

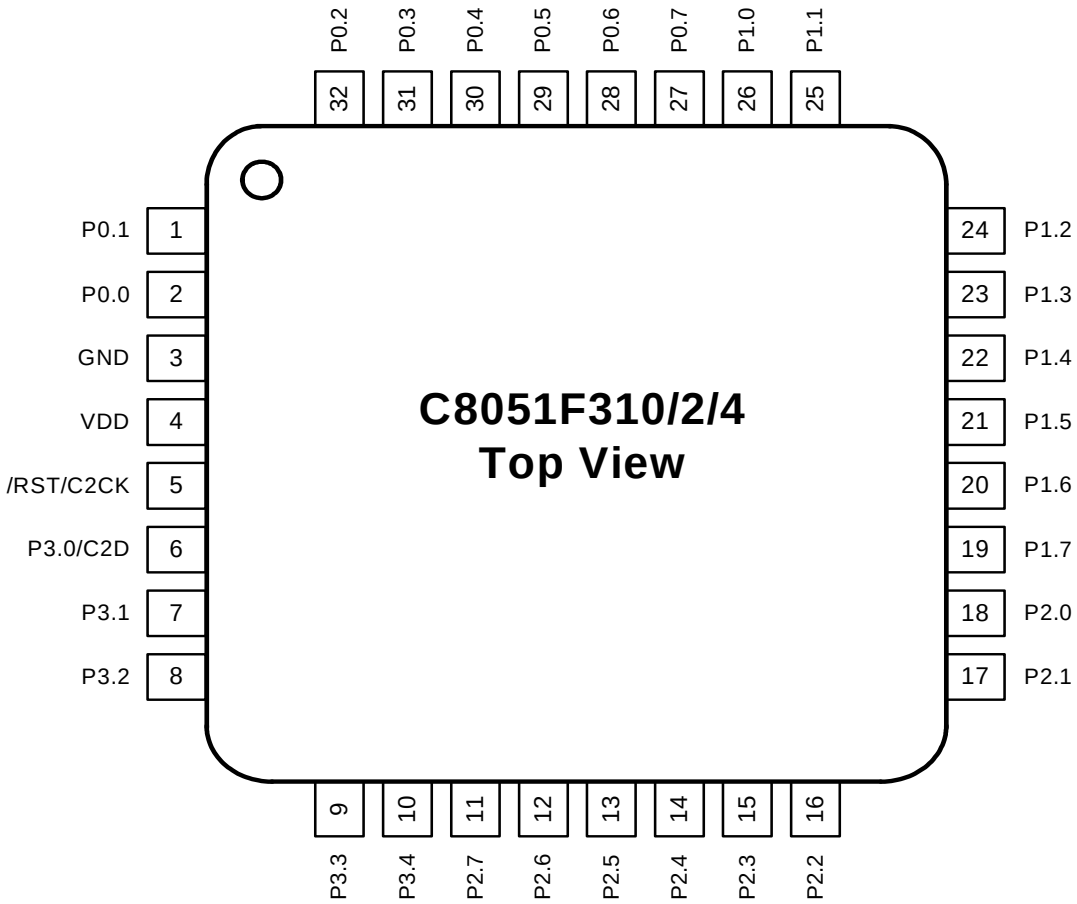

Figure 4.1. LQFP-32 Pinout Diagram (Top View)