MCF52277 Device Errata

Supports MCF52274 and MCF52277

by: Microcontroller Solutions Group

This document identifies implementation differences between the MCF5227*x* processors and the description contained in the *MCF52277 ColdFire® Reference Manual*. Refer to http://www.freescale.com/coldfire for the latest updates. The errata items listed in this document (summarized in Table 1) describe differences from the following documents:

- *MCF52277 ColdFire® Reference Manual*
- *ColdFire Microprocessor Family Programmer's Reference Manual*

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The latest version of the MCF52277 is marked as M26H.

Table 1. Summary of MCF52277 Errata

Errata ID	Module Affected	Date Errata Added	Mask Set Affected?	Errata Title
			M26H	
1	Cache	11/02/07	Yes	Possible cache corruption after setting CACR[CINV]
2	Cache	11/02/07	Yes	Incorrect operation of CACR[CFRZ]
3	LCD	11/02/07	Yes	LCD LSCLK signal misses pulse before LCD_OE asserts
4	Touchscreen	11/02/07	Yes	Resolution of ASP ADC channels
5	RTC	11/02/07	Yes	RTC operation in stop mode
6	PLL	1/22/08	Yes	PLL loss of lock and clock jitter
7	BDM	3/18/08	Yes	Level 2 trigger operation controlled by TDR[31]

You can also use the chip identification register (CIR) can to determine the silicon revision. Table 2 lists the CIR[PRN] field values that correspond to given mask sets.

Table 2. CIR[PRN] to Datecode

CIR[PRN] Value	Mask Set
0	M26H

1 Possible Cache Corruption After Clearing Cache (Setting CACR[CINV])

1.1 Description

The cache on the V2 ColdFire core was enhanced to function as a unified data and instruction cache, an instruction cache, or a data cache. The cache function and organization is controlled by the cache control register (CACR). The CACR[CINV] causes a cache clear. If the cache is configured as a unified cache and the CINV bit is set, the scope of the cache clear is controlled by two other bits in the CACR—CACR[INVI] invalidates instruction cache only and CACR[INVD] invalidates data cache only. These bits allow the entire cache, just the instruction portion of the cache, or just the data portion of the cache to be cleared. If a write to the CACR is performed to clear the cache (CACR[CINV] = 1) and only a partial clear is done (CACR[INVI] or CACR[INVD] set), then cache corruption may occur.

1.2 Workaround

All loads of the CACR that perform a cache clear operation (CACR[CINV] set) should be followed immediately by a NOP instruction. This avoids the cache corruption problem.

1.3 Status

Currently, there are no plans to fix this errata.

2 Incorrect Operation of Cache Freeze (CACR[CFRZ])

2.1 Description

The cache on the V2 ColdFire core is controlled by the cache control register (CACR). When the CACR[CFRZ] bit is set, the cache freeze function is enabled and no valid cache array entry will be displaced. However, this feature does not always work as specified, sometimes allowing valid lines to be displaced when CACR[CFRZ] is enabled.

This will not cause any corrupted accesses. However, there could be cache misses for data that was originally loaded into the cache but was subsequently deallocated, even though the CACR[CFRZ] bit was set.

Also, incoherent cache states are possible when a frozen cache is cleared via the CACR[CINV] bit in the CACR.

2.2 Workaround

- Unfreeze the cache by clearing CACR[CFRZ] when invalidating the cache using the CACR[CINV] bit.
- Use the internal SRAM to store critical code/data if the system cannot handle a potential cache miss.

2.3 Status

Currently, there are no plans to fix this errata.

3 LCD LSCLK Signal Misses Pulse Before LCD_OE Asserts

3.1 Description

When operating in 18bpp mode, the LSCLK signal will miss a clock pulse in the clock cycle before LCD_OE asserts. Since the missing clock pulse occurs when LCD_OE is negated, most LCD panels will operate correctly with no problem.

3.2 Workaround

If a continuous clock is needed even with LCD_OE negated, then 12bpp or 16bpp modes can be used. In these modes the LSCLK will not miss the pulse.

3.3 Status

Planning to fix this errata on the next silicon revision.

4 Resolution of ASP ADC Channels

4.1 Description

On the current silicon, the resolution of the ADC channels that feed into the ASP block are very low (approximately four bits of accuracy). The ADC logic is a new block, so the need for tuning of the circuit was expected and planned for in the silicon schedule.

4.2 Workaround

No workarounds.

4.3 Status

The ADC circuit will be tuned on the next silicon revision to increase the accuracy.

5 RTC Operation in Stop Mode

5.1 Description

On the current silicon, the RTC module stops counting when the device enters stop mode.

5.2 Workaround

No workarounds.

5.3 Status

On future devices the operation will be changed, so that the RTC continues to count in stop mode as long as its input clock is running. This way the RTC is able to wake up the processor from stop mode.

6 PLL Loss of Lock and Clock Jitter

6.1 Description

The current version of the PLL is sensitive to noise that can cause cycle-to-cycle jitter on the output clocks and, in some cases, cause the PLL to lose lock. This behavior of the PLL is related to the voltage used for the SDVDD rail and activity on the FlexBus.

Using a nominal SDVDD of 3.3V is the worst case. FlexBus activity can trigger a loss-of-lock condition. When a loss of lock occurs, the output clock switches to the limp mode clock. Then when lock is regained the system clocks return to using the PLL output. In addition, the output clock may also show cycle-to-cycle jitter even when the loss of lock does not occur (up to 2 ns).

At a nominal 2.5V or 1.8V SDVDD, the PLL loss of lock does not occur. However, the PLL output clock can have cycle-to-cycle jitter. The cycle-to-cycle jitter should be less than 700 ps.

6.2 Workaround

When using 3.3V for SDVDD, loss-of-lock detection by the PLL can be disabled by setting bit four in the PLL status register (PSR). This prevents the output clocks from switching to the limp mode clock, but there can still be cycle-to-cycle jitter on the output clocks. However, a loss-of-lock event can occur when booting from memory on the FlexBus before there is a chance to disable the loss-of-lock detect in software.

Freescale recommends four independent workarounds:

- Use 2.5V or 1.8V for the SDVDD supply.
- Use parallel boot, but boot the processor in limp mode. Once the loss-of-lock detect is disabled the PLL can be enabled.
- Use a serial device and the MCF5227x's serial boot facility (SBF) to configure the processor and execute code to disable the loss-of-lock detect.
- Use an asychronous non-volatile memory device for booting and disable the loss-of-lock detect in software as early as possible.

When using 2.5V or 1.8V for SDVDD, there is no workaround. If there are no sychronous devices in the system running from a clock source other than the MCF5227*x*, then no workaround should be needed.

6.3 Status

This errata is currently under investigation.

7 Level 2 Trigger Operation Controlled by TDR[31]

7.1 Description

The TDR[L2T] bit (TDR bit 15) has no effect on the level 2 trigger. Bit 31 of the TDR register provides both trigger response control and logical operation of the level 2 trigger.

7.2 Workaround

Use the TDR[31] bit to control the logical operation for the level 2 trigger as follows:

- 0 — Level 2 trigger = PC_condition & Address_range & Data_condition
- 1 — Level 2 trigger = PC_condition | (Address_range & Data_condition)

Since TDR[31] is also part of the trigger response control, only certain combinations of trigger responses and logical operations are available as shown below:

Table 3. TDR[31:30] Definitions

TDR[31:30]	Level 2 Trigger	Trigger Response
00	PC_cond & (Add_range & Data_cond)	Display on DDATA
01		Processor Halt
10	PC_cond | (Add_range & Data_cond)	Debug Interrupt
11		Reserved

7.3 Status

Will not be fixed.

8 Document Revision History

Table 4 provides a revision history for this document.

Table 4. Document Revision History

Rev. No.	Substantive Change(s)
4	Initial public revision
5	Added level 2 trigger operation errata

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