MSP430F21x2 Device Erratasheet

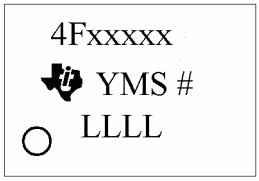
Current Version

Devices	Rev:	BCL12	FLASH19	FLASH24	FLASH27	PORT12	TA12	TA16	USCI20	USCI21	XOSC5
MSP430F2112	B	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2122	B	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2132	B	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

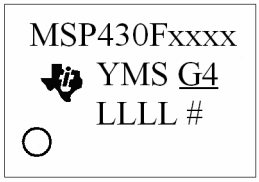
Note: See Appendix for prior revisions

Package Markings

PW28: TSSOP(PW) 28-pin

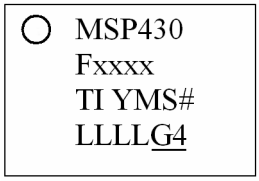


YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RHB32: QFN(RHB) 32-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

Detailed Bug Description

BCL12 BCL12 - Bug description

Module: BasicClock, Function: Switching RSEL can cause DCO dead time

After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12, the resulting clock delivered by the DCO can stop for a certain time before the new clock frequency gets applied. This dead time is in the range of 20 µs.

Workaround:
Use an intermediate step when switching RSEL from >13 to <12. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL.
14 or 15	13	Switch directly to target RSEL.
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence).
0 to 13	0 to 12	Switch directly to target RSEL.

FLASH19 FLASH19 - Bug description

Module: Flash, Function: EEI feature does not work for code execution from RAM

When the program is executed from RAM, the flash controller EEI feature does not work. The erase cycle is suspended, and the interrupt is serviced, but there is a problem while resuming with the erase cycle.
Addresses applied to flash are different than the actual values while resuming erase cycle after ISR execution.

Workaround:
None

Detailed Bug Description (continued)

FLASH24 FLASH24 - Bug description

Module: Flash, Function: Write or erase emergency exit can cause failures

When a flash write or erase is abruptly terminated, any further reliable reads by the flash controller are not ensured. The abrupt termination can be the result of one the following events:

1) The flash controller clock is configured to be SMCLK sourced by an external crystal. An oscillator fault occurs thus stopping this clock abruptly.
or
2) The Emergency Exit bit (EMEX in FCTL3), when set, forces a write or an erase operation to be terminated before normal completion.
or
3) The Enable Emergency Interrupt Exit bit (EEIEX in FCTL1), when set with GIE = 1, can lead to an interrupt causing an emergency exit during a flash operation.

Workaround:
1) Do not use SMCLK as the source for the flash controller clock if it is sourced from an external crystal.
2) After setting EMEX = 1, wait for a sufficient amount of time before flash is accessed again.
3) No workaround. Do not use EEIEX bit.

FLASH27 FLASH27 - Bug description

Module: Flash, Function: Segment erase is interrupted by FCTL1.EEI

A segment erase operation is interrupted by a pending interrupt when FCTL1.EEI = 1, although interrupts are globally disabled (GIE = 0). As GIE = 0, no ISR is executed and no RETI is generated by the CPU. However, the flash controller cannot proceed with the erase operation without a RETI instruction.

Workaround:
1) Always clear FCTL1.EEI control bit when GIE is cleared.
2) Add a loop after the dummy write, which tests FCTL3.BUSY for HIGH. When the loop is entered, generate a RETI to let the flash controller state machine continue. The loop is not entered anymore when the segment erase has been completed.

Example:

```
          mov R5,0(R5)      ; Dummy write, erase segments
LOOP      bit #BUSY,&FCTL3  ; test busy
          jmp SUB_RETI      ; generate reti
          jnz LOOP          ; loop while busy

SUB_RETI  push SR
          reti
```

Detailed Bug Description (continued)

PORT12 Port12 - Bug description

Module: Port, Function: PxIN register is getting reset for port instances 1 and 2

The P1IN and P2IN registers are cleared by a PUC reset. The registers are updated with the value of the respective pads when the PUC is deserted.

Workaround:
None

TA12 TA12 - Bug description

Module: Timer_A, Function: Interrupt is lost (slow ACLK)

Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description

Module: Timer_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

Detailed Bug Description (continued)

USCI20 USCI20 - Bug description

Module: USCI, Function: I2C Mode Multi-master transmitter issue

When configured for I2C master-transmitter mode and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following four conditions are true:

1) Two masters are generating SCL.
and
2) The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA.
and
3) The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line gets released.
and
4) The transmit buffer has not been loaded before the other master continues communication by driving SCL low.

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI interferes with the current bus activity and may cause unpredictable bus behavior.

Workaround:
1) Ensure that slave does not stretch the SCL low phase of an ACK period.
or
2) Ensure that the transmit buffer is loaded in time.
or
3) Do not use the multi-master transmitter mode.

USCI21 USCI21 - Bug description

Module: USCI, Function: UART IrDA receiver mode

IrDA reception does not function correctly at certain baud rates. This occurs only when the IrDA receive filter via the UCAxIRRCTL register is enabled and the USCI source clock (BRCLK) is higher than 6 MHz.

Workaround:
1) Set the filter length (UCIRRXFLx in UCAxIRRCTL) to the maximum value 0x3F to achieve proper functionality.
2) Reduce the frequency of the USCI source clock (BRCLK) to the IrDA module to be less than 6 MHz.

XOSC5 XOSC5 - Bug description

Module: LFXT1 Oscillator, Function: LF crystal failures may not be properly detected by the oscillator fault circuitry

The oscillator fault error detection of the LFXT1 oscillator in low frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU, i.e., OFIFG will not be set.

Workaround:
None

Appendix: Prior Versions

Devices	Rev:	BCL12	BCL13	FLASH19	FLASH24	FLASH27	PORT12	TA12	TA16	USCI20	USCI21	XOSC5
MSP430F2112	B	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2122	B	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2132	B	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2112	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2122	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2132	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Detailed Bug Description

BCL13 BCL13 - Bug description

When subject to very slow V_{CC} rise times, the device may enter into a state in which the DCO does not oscillate. No JTAG access or program execution is possible, and the device remains in a reset state until the supply voltage is disconnected.

Workaround:
Apply a V_{CC} power-on ramp ≥10 V/second under all power-on/power-cycle scenarios.

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