MSP430F23x/24x(1)/2410 Device Erratasheet

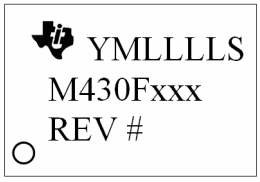
Current Version

Devices	Rev:	BCL12	CPU8	FLASH24	FLASH27	TA12	TA16	TB2	TB16	USCI20	USCI21	XOSC5	XOSC6
MSP430F233	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F235	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2410	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F247	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2471	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F248	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2481	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F249	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2491	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

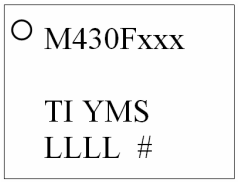
Package Markings

PM64: LQFP(PM) 64-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RGC64: QFN(RGC) 64-pin



TI = TI
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

Detailed Bug Description

BCL12 BCL12 - Bug description

Module: BasicClock, Function: Switching RSEL can cause DCO dead time

After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12, the resulting clock delivered by the DCO can stop for a certain time before the new clock frequency gets applied. This dead time is in the range of 20 µs.

Workaround:
Use an intermediate step when switching RSEL from >13 to <12. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL.
14 or 15	13	Switch directly to target RSEL.
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence).
0 to 13	0 to 12	Switch directly to target RSEL.

CPU8 CPU8 - Bug description

Module: CPU, using odd values in the SP register

The SP can be written with odd values. In the original CPU, an odd SP value could be combined with an odd offset (i.e., `mov. #value, 5(SP)`). In the new CPU, the SP can be written with an odd value, but the first time the SP is used, the LSB is forced to 0.

Workaround:
Do not use odd values with the SP.

FLASH24 FLASH24 - Bug description

Module: Flash, write or erase emergency exit can cause failures

When a flash write or erase is abruptly terminated, any further reliable reads by the flash controller are not ensured. The abrupt termination can be the result of one the following events:

1) The flash controller clock is configured to be SMCLK sourced by an external crystal. An oscillator fault occurs thus stopping this clock abruptly.
or
2) The Emergency Exit bit (EMEX in FCTL3), when set, forces a write or an erase operation to be terminated before normal completion.
or
3) The Enable Emergency Interrupt Exit bit (EEIEX in FCTL1), when set with GIE = 1, can lead to an interrupt causing an emergency exit during a flash operation.

Workaround:
1) Do not use SMCLK as the source for the flash controller clock if it is sourced from an external crystal.
2) After setting EMEX = 1, wait for a sufficient amount of time before flash is accessed again.
3) No Workaround. Do not use EEIEX bit.

Detailed Bug Description (continued)

FLASH27 FLASH27 - Bug description

Module: Flash, Function: Segment erase is interrupted by FCTL1.EEI

A segment erase operation is interrupted by a pending interrupt when FCTL1.EEI = 1, although interrupts are globally disabled (GIE = 0). As GIE = 0, no ISR is executed and no RETI is generated by the CPU. However, the flash controller cannot proceed with the erase operation without a RETI instruction.

Workaround:
1) Always clear FCTL1.EEI control bit when GIE is cleared.
2) Add a loop after the dummy write, which tests FCTL3.BUSY for HIGH. When the loop is entered, generate a RETI to let the Flash controller state machine continue. The loop is not entered any more when the segment erase has been completed.

Example:

```
          mov R5,0(R5)      ; Dummy write, erase segments
LOOP      bit #BUSY,&FCTL3  ; test busy
          jmp SUB_RETI      ; generate reti
          jnz LOOP          ; loop while busy

SUB_RETI  push SR
          reti
```

TA12 TA12 - Bug description

Module: Timer_A, Function: Interrupt is lost (slow ACLK)

Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.

TA16 TA16 - Bug description

Module: Timer_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

Detailed Bug Description (continued)

TB2 TB2 - Bug description

Module: Timer_B, Interrupt is lost (slow ACLK)

Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if TBR = CCRx + 1). This interrupt is lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TB16 TB16 - Bug description

Module: Timer_B, Function: First increment of TBR erroneous when IDx > 00

The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

Workaround:
None

Detailed Bug Description (continued)

USCI20 USCI20 - Bug description

Module: USCI, Function: I2C Mode Multi-master transmitter issue

When configured for I2C master-transmitter mode, and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following four conditions are true:

1) Two masters are generating SCL.
and
2) The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA.
and
3) The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line is released.
and
4) The transmit buffer has not been loaded before the other master continues communication by driving SCL low.

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI interferes with the current bus activity and may cause unpredictable bus behavior.

Workaround
1) Ensure that slave does not stretch the SCL low phase of an ACK period.
or
2) Ensure that the transmit buffer is loaded in time.
or
3) Do not use the multi-master transmitter mode.

USCI21 USCI21 - Bug description

Module: USCI, Function: UART IrDA Receiver Mode

IrDA reception does not function correctly at certain baud rates. This occurs only when the IrDA receive filter via the UCAxIRRCTL register is enabled and the USCI source clock (BRCLK) is higher than 6 MHz.

Workaround:
1) Set the filter length (UCIRRXFLx in UCAxIRRCTL) to the maximum value 0x3F to achieve proper functionality.
2) Reduce the frequency of the USCI source clock (BRCLK) to the IrDA module to be less than 6 MHz.

XOSC5 XOSC5 - Bug description

Module: LFXT1 Oscillator, Function: LF crystal failures may not be properly detected by the oscillator fault circuitry

The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU, i.e., OFIFG will not be set.

Workaround:
None

Detailed Bug Description (continued)

XOSC6 XOSC6 - Bug description

Module: XT2 Oscillator, Function: XT2 crystal failures may not be properly detected by the oscillator fault circuitry

The XT2OF flag should be set if the XT2 frequency falls below 30 kHz. If there is no oscillation at all, the flag still operates properly. However, 0 kHz to 30 kHz produces an undefined state on XT2OF. When this occurs, OFIFG will not be set.

Workaround:
Do not depend on the fault detection circuitry to accurately detect all failures.

Appendix: Prior Versions

Devices	Rev:	BCL12	BCL13	COMP2	CPU8	FLASH24	FLASH25	FLASH27	PORT11	TA12	TA16	TB2	TB16	USCI20	USCI21	XOSC5	XOSC6
MSP430F233	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F235	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2410	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F247	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2471	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F248	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2481	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F249	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2491	D	✓			✓	✓		✓		✓	✓	✓	✓	✓	✓	✓	✓
	C	✓	✓		✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓
	B	✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Detailed Bug Description

BCL13 BCL13 - Bug description

When subject to very slow V_{cc} rise times, the device may enter into a state where the DCO does not oscillate. No JTAG access or program execution is possible, and the device remains in a reset state until the supply voltage is disconnected.

Workaround:
Apply a V_{cc} power-on ramp ≥10 V/second under all power-on/power-cycle scenarios.

Detailed Bug Description (continued)

COMP2 COMP2 - Bug description

Module: Comparator_A+, Function: Configuring the port disable register (CAPD)

According to the user's guide, each bit in the CAPD register should correspond with its associated port I/O number. For example, when bit 0 of CAPD is set, the port disable function of pin Px.0 is enabled; bit 1 controls Px.1, and so on (where Px is the port that contains the comparator inputs). However, on this device, the bits of the CAPD register correspond with the Comparator_A input number. For example, bit 0 of CAPD controls the CA0 input, bit 1 controls CA1, etc. This difference matters when the port I/O number is not the same as the comparator input number.

If the wrong CAPD bit is set, the port I/O function for the wrong pin will be disabled. Also, the analog signal applied to the comparator input pin being used may cause a parasitic current to flow from V_{cc} to GND (see the Comparator_A+ chapter of the *MSP430x2xx Family User's Guide* for more information on CAPD).

FLASH25 FLASH25 - Bug description

Module: Flash, Function: Marginal Read Mode is not functional

The control bits for marginal read mode contained in the FCTL4 register are automatically cleared by any flash access. This prevents the marginal read mode from being used.

Workarounds:

It is possible to read out memory contents in marginal read mode if the indexed addressing mode X(Ry) is used to access the flash memory. In this case, the FCTL4 control bits are not cleared, and the marginal read mode works as expected. It is recommended to write the code for reading the flash memory contents in assembly, as this allows full control over the addressing mode that is used. Note that certain assemblers may optimize an indexed addressing source operation of 0(Ry) to an indirect register mode @Ry operation, which does not work. The following code is an example of reading the word memory location 0x4000 in marginal read mode, preventing a possible assembler optimization:

```
mov.w #0x4000,R15 ; Pointer to target address
dec.w R15         ; Decrement pointer
mov.w 1(R15),R12  ; Read memory contents at R15+1, store result in R12
```

Detailed Bug Description (continued)

PORT11 PORT11 - Bug description

Module: Port, Function: Pullup for P3.6 controlled by bit 0

According to the user's guide, the internal pullup of an I/O should be enabled when a corresponding bit from PxREN and PxOUT are both set. For example, in the case of P3.6, this should be bit 6. However, P3.6 is currently controlled by bit 0 instead. Bit 0 also controls P3.0, as expected. The pulldown resistors operate properly and are not affected by this errata.

Workarounds:
If bit 6 of PxREN is set, bits 0 and 6 of PxOUT should be set/cleared together. If P3.6 is to be configured for pullup/down, P3.0 must have the same configuration. So the workaround options are:

- Configure both P3.0 and P3.6 with pulldowns (bits 0/6 of PxREN set, bits 0/6 of PxOUT cleared).
- Configure both P3.0 and P3.6 with pullups (bits 0/6 of PxREN set/cleared, bits 0/6 of PxOUT set).
- Do not use the pullup/pulldown feature on these pins (bits 0/6 of PxREN cleared).

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