MSP430F22x2/22x4 Device Erratasheet

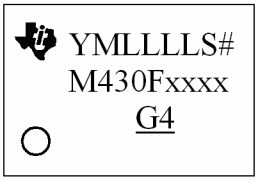
Current Version

Devices	Rev:	BCL12	FLASH24	PORT10	TA12	TA16	TB2	TB16	USCI20	USCI21	XOSC5
MSP430F2232	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

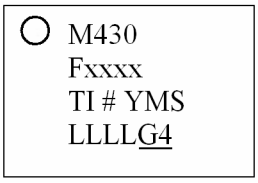
Package Markings

DA38: TSSOP(DA) 38-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RHA40: QFN(RHA) 40-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

Detailed Bug Description

BCL12 BCL12 - Bug description

Module: BasicClock, Function: Switching RSEL can cause DCO dead time

After switching RSELx bits (located in register BCSCTL1) from a value of >13 to a value of <12, the resulting clock delivered by the DCO can stop for a certain time before the new clock frequency gets applied. This dead time is in the range of 20 µs.

Workaround:
Use an intermediate step when switching RSEL from >13 to <12. The intermediate RSEL value should be 13.

CURRENT RSEL	TARGET RSEL	RECOMMENDED TRANSITION SEQUENCE
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

FLASH24 FLASH24 - Bug description

Module: Flash, Function: Write or erase emergency exit can cause failures

When a flash write or erase is abruptly terminated, any further reliable reads by the flash controller are not ensured. The abrupt termination can be the result of one the following events:

1) The flash controller clock is configured to be SMCLK sourced by an external crystal. An oscillator fault occurs thus stopping this clock abruptly.
Or
2) The Emergency Exit bit (EMEX in FCTL3) when set forces a write or an erase operation to be terminated before normal completion.
Or
3) The Enable Emergency Interrupt Exit bit (EEIEX in FCTL1) when set with GIE = 1 can lead to an interrupt causing an emergency exit during a Flash operation.

Workaround:
1) Do not use SMCLK as the source for the flash controller clock if it is sourced from an external crystal.
2) After setting EMEX = 1, wait for a sufficient amount of time before Flash is accessed again.
3) No Workaround. Do not use EEIEX bit.

PORT10 Port10 - Bug description

Module: Digital I/O, Function: Pullup/pulldown resistor selection when module pin function is selected

When the pullup/pulldown resistor for a certain port pin is enabled (PxREN.y = 1) and the module port pin function is selected (PxSEL.y = 1), the pullup/pulldown resistor configuration of this pin is controlled by the respective module output signal (Module X OUT) instead of the port output register (PxOUT.y).

Workaround:
None. Do not set PxSEL.y and PxREN.y at the same time.

Detailed Bug Description (continued)

TA12 TA12 - Bug description

Module: Timer_A, Function: Interrupt is lost (slow ACLK)

Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt is lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description

Module: Timer_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

TB2 TB2 - Bug description

Module: Timer_B, Interrupt is lost (slow ACLK)

Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if TBR = CCRx + 1). This interrupt is lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

Detailed Bug Description (continued)

TB16 TB16 - Bug description

Module: Timer_B, Function: First increment of TBR erroneous when IDx > 00

The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.

Workaround:
None

USCI20 USCI20 - Bug description

Module: USCI, Function: I2C Mode Multi-master transmitter issue

When configured for I2C master-transmitter mode, and used in a multi-master environment, the USCI module can cause unpredictable bus behavior if all of the following four conditions are true:

1 - Two masters are generating SCL
And
2 - The slave is stretching the SCL low phase of an ACK period while outputting NACK on SDA
And
3 - The slave drives ACK on SDA after the USCI has already released SCL, and then the SCL bus line gets released
And
4 - The transmit buffer has not been loaded before the other master continues communication by driving SCL low

The USCI remains in the SCL high phase until the transmit buffer is written. After the transmit buffer has been written, the USCI interferes with the current bus activity and may cause unpredictable bus behavior.

Workaround:
1 - Ensure that slave does not stretch the SCL low phase of an ACK period
Or
2 - Ensure that the transmit buffer is loaded in time
Or
3 - Do not use the multi-master transmitter mode

USCI21 USCI21 - Bug description

Module: USCI, Function: UART IrDA Receiver Mode

IrDA reception does not function correctly at certain baud rates. This occurs only when the IrDA Receive Filter via the UCAxIRRCTL register is enabled and the USCI source clock (BRCLK) is higher than 6 MHz.

Workaround:
1.Set the filter length (UCIRRXFLx in UCAxIRRCTL) to the maximum value 0x3F to achieve proper functionality.
2.Reduce the frequency of the USCI source clock (BRCLK) to the IrDA module to be less than 6 MHz.

Detailed Bug Description (continued)

XOSC5 XOSC5 - Bug description

Module: LFXT1 OSC: LF crystal failures may not be properly detected by the oscillator fault circuitry

The oscillator fault error detection of the LFXT1 oscillator in low-frequency mode (XTS = 0) may not work reliably, causing a failing crystal to go undetected by the CPU, i.e., OFIFG is not set.

Workaround:
None

Appendix: Prior Versions

Devices	Rev:	BCL12	BCL13	CPU14	FLASH21	FLASH22	FLASH24	JTAG13	JTAG14	PORT10	TA12	TA16	TB2	TB16	USCI16	USCI20	USCI21	XOSC5
MSP430F2232	G	✓					✓			✓	✓	✓	✓	✓		✓	✓	✓
	F	✓	✓				✓			✓	✓	✓	✓	✓		✓	✓	✓
	E	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2234	G	✓					✓			✓	✓	✓	✓	✓		✓	✓	✓
	F	✓	✓				✓			✓	✓	✓	✓	✓		✓	✓	✓
	E	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2252	G	✓					✓			✓	✓	✓	✓	✓		✓	✓	✓
	F	✓	✓				✓			✓	✓	✓	✓	✓		✓	✓	✓
	E	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2254	G	✓					✓			✓	✓	✓	✓	✓		✓	✓	✓
	F	✓	✓				✓			✓	✓	✓	✓	✓		✓	✓	✓
	E	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2272	G	✓					✓			✓	✓	✓	✓	✓		✓	✓	✓
	F	✓	✓				✓			✓	✓	✓	✓	✓		✓	✓	✓
	E	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F2274	G	✓					✓			✓	✓	✓	✓	✓		✓	✓	✓
	F	✓	✓				✓			✓	✓	✓	✓	✓		✓	✓	✓
	E	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	D	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Detailed Bug Description

BCL13 BCL13 - Bug description

When subject to very slow V_{cc} rise times, the device may enter into a state in which the DCO does not oscillate. No JTAG access or program execution is possible and the device remains in a reset state until the supply voltage is disconnected.

Workaround:
Apply a V_{cc} power-on ramp ≥10 V/s under all power-on/power-cycle scenarios.

Detailed Bug Description (continued)

CPU14 CPU14 - Bug description

Module: CPU, Function: Erroneous setting of SCG0 after reset

The SCG0 bit in the CPU status register (SR) is set after any reset (PUC or POR) if bit #6 in the reset vector destination address is set. Setting SCG0 turns off the DCO DC generator when DCOCLK is not used for MCLK or SMCLK.

Workarounds:
1) As the error only occurs after PUC or POR, it is sufficient to clear the SCG0 bit at the beginning of the program code. Example:
   bic.w #SCG0, SR
2) Avoid using reset destination addresses where bit #6 is set. Allowed reset vector destination addresses are: xx0xh, xx1xh, xx2xh, xx3xh, xx8xh, xx9xh, xxAxh, xxBxh.

When any of the above reset destination addresses are used, SCG0 is valid.

FLASH21 FLASH21 - Bug description

Module: Flash, Function: Info memory read data corrupted

Flash addresses between 0x1080 and 0x10ff (information memory) might not be read correctly. Supply voltages and addressing mode affect the read value.

Workaround:
None

FLASH22 FLASH22 - Bug description

Module: Flash, Function: Flash controller may prevent correct LPM entry

When ACLK (or SMCLK) is used as the flash controller clock source, and this clock source is deactivated due to a low-power mode entry while a flash erase or write operating is pending, the flash controller keeps ACLK (or SMCLK) active even after the flash operation has been completed. This results in an incorrect LPM entry and increased current consumption. Note that this issue can occur only when the flash operation and the low-power mode entry are initiated from code located in RAM.

Workaround:
Do not enter low-power modes while flash erase or write operations are active. Wait for the operation to be completed before entering a low-power mode.

JTAG13 JTAG13 - Bug description

Module: JTAG, PSA Checksum generation fails

PSA checksum generation gives a wrong result when data_psa is executed during test clock low phase and the last address of flash info memory addresses 0x107E or 0x10FE are part of the calculation

Workaround:
Calculate psa sum when test clock is at high level.

Detailed Bug Description (continued)

JTAG14 JTAG14 - Bug description

Module EEM: Releasing JTAG control can corrupt CPU registers during debug

During a debug session, on rare occasions, the CPU register contents can get corrupted when JTAG control is released by the debugger. This behavior is exhibited during, but not limited to, the use of the “Use Virtual Breakpoints” and “Force Single Stepping” features in the IAR Embedded Workbench software. This bug does not affect normal device and application operation, such as starting a device out of POR and executing application code.

In order for the bug to occur, both of the following two conditions must be true:

1) The CPU (MCLK) is sourced by the DCO
And
2) The “External Resistor (Rosc)” feature of the DCO is not used

Workaround:
Use an external crystal or a digital high-speed clock source connected to the LFXT1 oscillator to source the CPU (MCLK) during a debug session. Alternatively, use the on-chip DCO in the “External Resistor (Rosc)” configuration. Note that in this case an external resistor connected to the device’s Rosc pin is mandatory, and that the factory-programmed DCO calibration constants cannot be applied directly.

USCI16 USCI16 - Bug description

Module: USCI, Function: UART/IrDA Mode Lost Characters

When configured for UART/IrDA mode, the USCI baud rate generator may halt operation under the following conditions:
1) IrDA mode: repeated invalid start bits on the receive line
Or
2) UART/IrDA modes: positive pulse on the receive line during break character reception inside the stop bit time slot (the second stop bit time slot in case of UCSPB = 1) with a pulse width that passes the deglitch filter but is shorter than half a bit time.

After halting, additional characters are ignored. Transmit functionality is not affected.

Workaround:
Check the UCBUSY flag status periodically in software. If the flag is set and no character has been received in the expected time, reset the USCI module in software. To reset the USCI module, toggle UCSWRST and reenable the USCI interrupts.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265