MSP430FE42x Device Erratasheet

Current Version

Device	Revision	CPU4	ESP1	ESP2	ESP3	FLL3	SD1	SD2	TA12	TA16	US15	WDG2
MSP430FE425	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FE426	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FE427	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

Package Markings

PM64: LQFP(PM) 64-pin

YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

Detailed Bug Description

CPU4 CPU4 - Bug description

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, –1) can be used. The number of clock cycles is different:
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.
No fix planned.

ESP1 ESP1 - Bug description

Module: ESP430CE1, Function: Suspending the ESP430CE1

Suspending the ESP430 may create an invalid interrupt, which can lead to a reset-like behavior of the module.

Workaround:
Set the bit 0x08 together with the ESPSUSP bit:

```
bis.w    #08h+ESPSUSP, &ESPCTL
```

This bit needs to be cleared when the suspend mode is exited, too.

```
bic.w    #08h+ESPSUSP, &ESPCTL
```

NOTE:

- After suspending the ESP430CE1 it can take up to 9 MCLK clock cycles before the CPU can access the SD16 registers.
- An interrupt service routine for the SD16 is required.

```
// Shut down ESP (set Embedded Signal Processing into
// "Suspend" mode)
// ensure that it is not in measurement or calibration mode,
      ESPCTL |= 0x08 + ESPSUSP;
         // Set ESP into Suspend Mode
         // incl.  Bug Fix for Suspend Mode
// wait 9 clocks until proper access to the SD16 is possible
      _NOP();_NOP();_NOP();_NOP();_NOP();
      _NOP();_NOP();_NOP();_NOP();

      MBCTL &= ~(IN0IFG + IN0IE);
         // Clear any Pending MB interrupt and disable
         // ESP interrupt
      SD16CTL &= ~SD16REFON; // Switch Reference off
```

Detailed Bug Description (continued)

ESP2 ESP2 - Bug description

Module: ESP430CE1, Function: Negative energy flag operation

The NEGENFG negative energy flag treatment inside the ESP430 module is executed after each mains cycle and is set according to the energy accumulated during this period. Therefore, the flag is set under two conditions:

- If during at least one mains cycle period over the last second the accumulated energy in the ACTENSPER register was negative
- If the accumulated energy in the ACTENERGY register is negative

Workaround:
If the indication of the negative energy status is required by the application it can be done with following sequence in CPU software.

1) Set negative energy bits: NE0 = 0, NE1 = 1 (negative energy is summed)
2) Perform the required steps manually in software after new energy samples are available from the ESP430CE1:
   - Check if the energy is negative and set the negative energy flag
   - Correct the energy to positive values, if required

```
if ((msg_data & ENRDYFG))
    {
       if ((ACTENERGY1_HI & 0x8000) > 0 ) {// Negative Energy measured ?
        negenfg = 1;        // set global neg. Energy Flag
       }else {
         negenfg = 0;       // clear global neg. Energy Flag
       }

      if (negenfg == 1) // Negative Energy measured ?
         total_energy -= (float)energy.l;
      else
         total_energy += (float)energy.l;

    } // End of if ((msg_data & ENRDY)
```

Detailed Bug Description (continued)

ESP3 ESP3 - Bug description

Module: ESP430CE1, Function: Temperature measurement in Tamper mode could modify SD16 settings.

Unintended modification of the SD16 registers by the ESP can occur during temperature measurement when operating in Tamper mode. The following simultaneous events can trigger this:

1. Meter is running in Tamper mode (measuring on both I1 and I2 current channels).
2. Temperature measurement is requested.
3. I2GTI1FG in register ESP430_STAT0 changes state from logic 0 to 1 or logic 1 to 0 during the temperature measurement.

Workaround:
Synchronize the request for temperature measurement with the ENRDYFG or ENRDYME. Request for temperature measurement after the flag ENRDYFG = 1, or when ENRDYME is set to 1. This ensures enough time for the temperature measurement before I2GTI1FG changes state.

FLL3 FLL3 - Bug description

Module: FLL+, Function: FLLDx = 11 for /8 may generate an unstable MCLK frequency

When setting the FLL to higher frequencies using FLLDx = 11 (/8), the output frequency of the FLL may have a larger frequency variation (e.g,. averaged over 2 seconds), as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround:
None

SD1 SD1 - Bug description

Module: SD16, Function: Reduced SINAD performance if SD16 clock source is greater than 6 MHz

If the frequency of the SD16 input clock source is greater than 6 MHz, the performance of the SD16 may be degraded due to noise influencing the analog measurements under reduced SINAD.

Workaround:
Writing 0x48 to memory location 0xBF configures the SD16 for optimized performance at input clock frequencies greater than 6 MHz.

Include the following code

```
*(unsigned char*) 0xBF=0x48;  // Write value 0x48 to memory address 0xBF
```

Detailed Bug Description (continued)

SD2 SD2 - Bug description

Module: SD16, Function: Internal short measurement can be influenced by external Ax.0 analog voltages

Applying a common-mode voltage other than VSS or a differential voltage to the analog inputs of the SD16 may influence the measurement accuracy when converting the internal short channel (A7). The error under these conditions is proportional to the common mode or differential voltage and is typically 150+ LSBs.

Workaround:
Avoid applying common mode voltages other than VSS, or a differential input voltage during the measurement of the internal short channel.

TA12 TA12 - Bug description

Module: Timer_A, Function: Interrupt is lost (slow ACLK)

Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).
Due to the fast MCLK, the CCRx register increment (CCRx = CCRx + 1) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description

Module: Timer_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

US15 US15 - Bug description

Module: USART0, USART1, Function: UART receive with two stop bits

USART hardware does not detect a missing second stop bit when SPB = 1. The Framing Error flag (FE) will not be set under this condition, and erroneous data reception may occur.

Workaround:
None (Configure USART for a single stop bit, SPB = 0)

Detailed Bug Description (continued)

WDG2 WDG2 - Bug description

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:
None

Appendix: Prior Versions

Device	Revision	CPU4	ESP1	ESP2	ESP3	FLL3	SD1	SD2	TA12	TA16	US15	WDG2
MSP430FE425	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FE426	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FE427	G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

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