MSP430FG42x0 Device Erratasheet

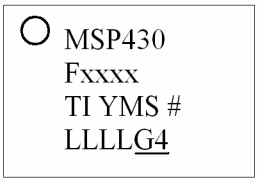
Current Version

Devices	Rev:	CPU4	DAC2	DAC3	FLL3	LCDA1	LCDA2	LCDA3	PORT6	SDA1	SDA3	TA12	TA16	WDG2
MSP430FG4250	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4260	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FG4270	A	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

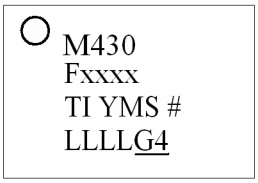
Note: See Appendix for prior revisions

Package Markings

RGZ48: QFN(RGZ) 48-pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
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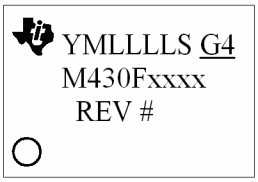
o = PIN 1

DL48: SOP(DL) 48-pin



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LLLL = LOT Trace Code
S = Assembly Site Code
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o = PIN 1

Detailed Bug Description

CPU4 CPU4 - Bug description:

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The Assembler version 1.08 and higher produces correct code. The number of clock cycles is different:
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.
No fix planned.

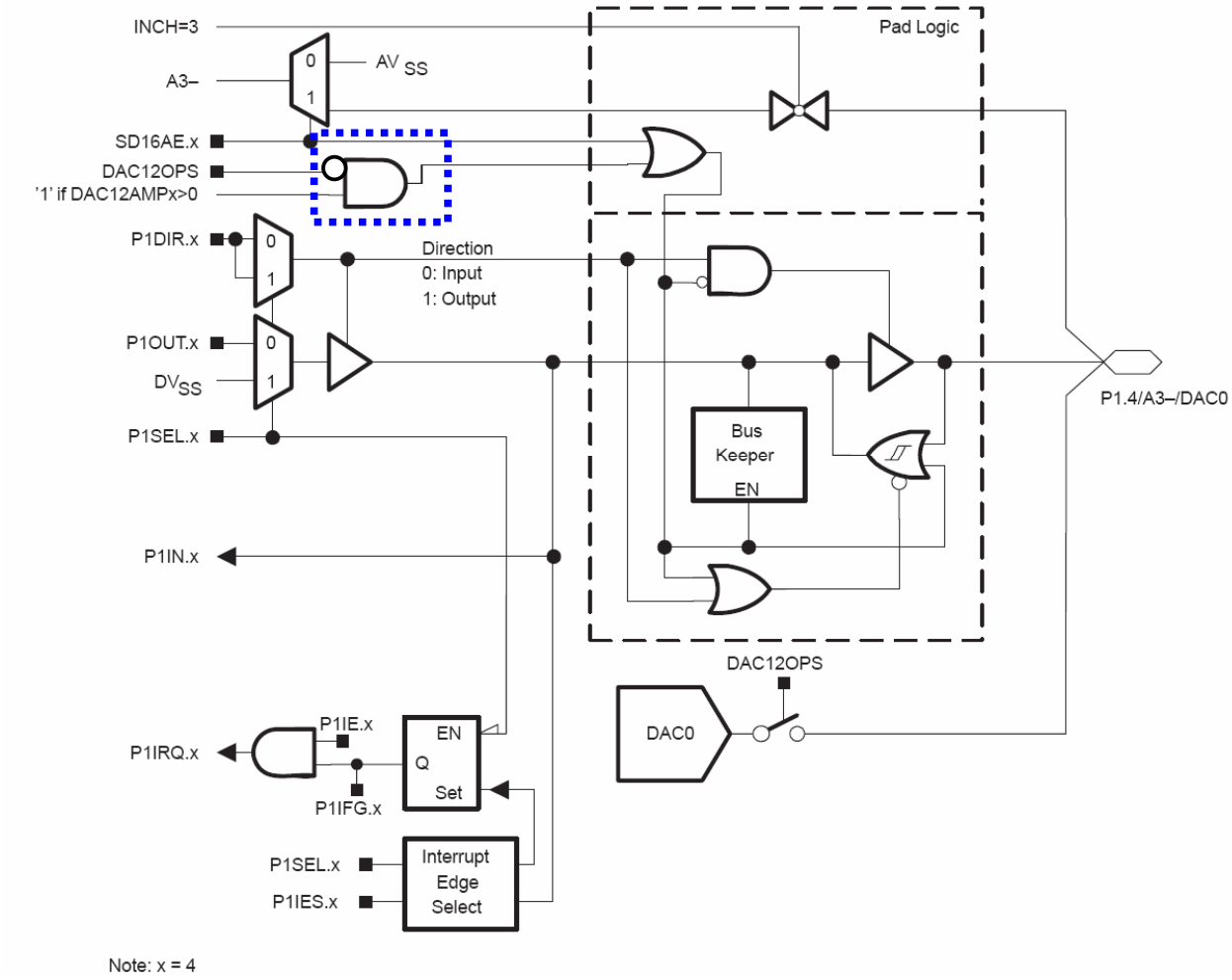
Detailed Bug Description (continued)

DAC2 DAC2 - Bug description:

Module: DAC12, Function: P1.4 GPIO function is not disabled when P1.4 = DAC0 output

The DAC12OPS control bit used to automatically disable the P1.4 I/O logic is inverted as shown in the figure below. When DAC12 is enabled (DAC12AMPx > 0) and DAC12OPS=0, the port I/O for P1.4 will be disabled. Setting DAC12OPS = 1 to connect the DAC12 output to P1.4 will erroneously enable the port GPIO logic.

Port P1 pin schematic: P1.4, input/output with Schmitt–trigger and analog functions



Note: x = 4

Workaround:
The P1.4 I/O logic should be disabled when the DAC12 is enabled using the SD16AE.4 analog enable bit. SD16AE.4=1 will disable the P1.4 I/O logic. The A3 SD16_A analog input cannot be used under this condition.

Detailed Bug Description (continued)

DAC3 DAC3 - Bug description:

Module: DAC12, Function: Port P1.4 can not be used if DAC12 is internally enabled.

When DAC12 is enabled (DAC12AMPx > 0) and internal use is selected (DAC12OPS=0), the P1.4 digital I/O functionality is disabled.
See also: DAC2 bug description.

Workaround:
None

FLL3 FLL3 – Bug description:

Module: FLL+, Function: FLLDx = 11 for /8 may generate an unstable MCLK frequency

When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g. averaged over 2sec) as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround:
None

LCDA1 LCDA1 - Bug description:

Module: LCD_A, Function High voltage on LCD_A pins.

When static LCD mode is selected, the charge pump does not work correctly. The feedback loop within the charge pump is switched off. This can result in high voltages on LCD_A segment and common pins.

WARNING: Using the charge pump when static mode is selected may cause permanent damage to the MSP430 device and/or the LCD.

Workaround:
None

LCDA2 LCDA2 - Bug description:

Module: LCD_A, Floating segment S5

Dedicated LCD segment S5 is floating when LCD_A is disabled: LCDON = 0.
In this case S5 should be connected to ground.

Workaround:
None

Detailed Bug Description (continued)

LCDA3 LCDA3 - Bug description:

Module: LCD_A, Charge pump voltage

The charge pump output voltage has an offset of approximately -200 mV. This reduces the LCD voltage levels specified in the datasheet for LCD_A by the same amount and should be accounted for when selecting a charge pump voltage. See actual values below:

LCD_A

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$V_{CC(LCD)}$	Supply Voltage Range	Charge pump enabled (LCDCPEN = 1; VLCDx > 0000)		2.2		3.6	V
C_{LCD}	Capacitor on LCDCAP (see Note 1)	Charge pump enabled (LCDCPEN = 1; VLCDx > 0000)		4.7			µF
$I_{CC(LCD)}$	Supply Current	$V_{LCD(typ)}$=3V; LCDCPEN = 1; VLCDx= 1000, all segments on f_{LCD}= f_{ACLK}/32 no LCD connected (see Note 2) T_A = 25°C	2.2 V		3.8		µA
f_{LCD}	LCD frequency					1.1	kHz
V_{LCD}	LCD voltage	VLCDx = 0000			VCC		V
V_{LCD}	LCD voltage	VLCDx = 0001			2.50		V
V_{LCD}	LCD voltage	VLCDx = 0010			2.56		V
V_{LCD}	LCD voltage	VLCDx = 0011			2.61		V
V_{LCD}	LCD voltage	VLCDx = 0100			2.67		V
V_{LCD}	LCD voltage	VLCDx = 0101			2.72		V
V_{LCD}	LCD voltage	VLCDx = 0110			2.78		V
V_{LCD}	LCD voltage	VLCDx = 0111			2.83		V
V_{LCD}	LCD voltage	VLCDx = 1000			2.89		V
V_{LCD}	LCD voltage	VLCDx = 1001			2.94		V
V_{LCD}	LCD voltage	VLCDx = 1010			3.00		V
V_{LCD}	LCD voltage	VLCDx = 1011			3.05		V
V_{LCD}	LCD voltage	VLCDx = 1100			3.11		V
V_{LCD}	LCD voltage	VLCDx = 1101			3.16		V
V_{LCD}	LCD voltage	VLCDx = 1110			3.22		V
V_{LCD}	LCD voltage	VLCDx = 1111		3.12	3.27	3.42	V
R_{LCD}	LCD Driver Output impedance	V_{LCD} = 3V; LCDCPEN = 1; VLCDx = 1000, I_{LOAD} = ±10µA	2.2 V			10	kΩ

NOTES: 1. Enabling the internal charge pump with an external capacitor smaller than the minimum specified might damage the device.
2. Connecting an actual display will increase the current consumption depending on the size of the LCD.

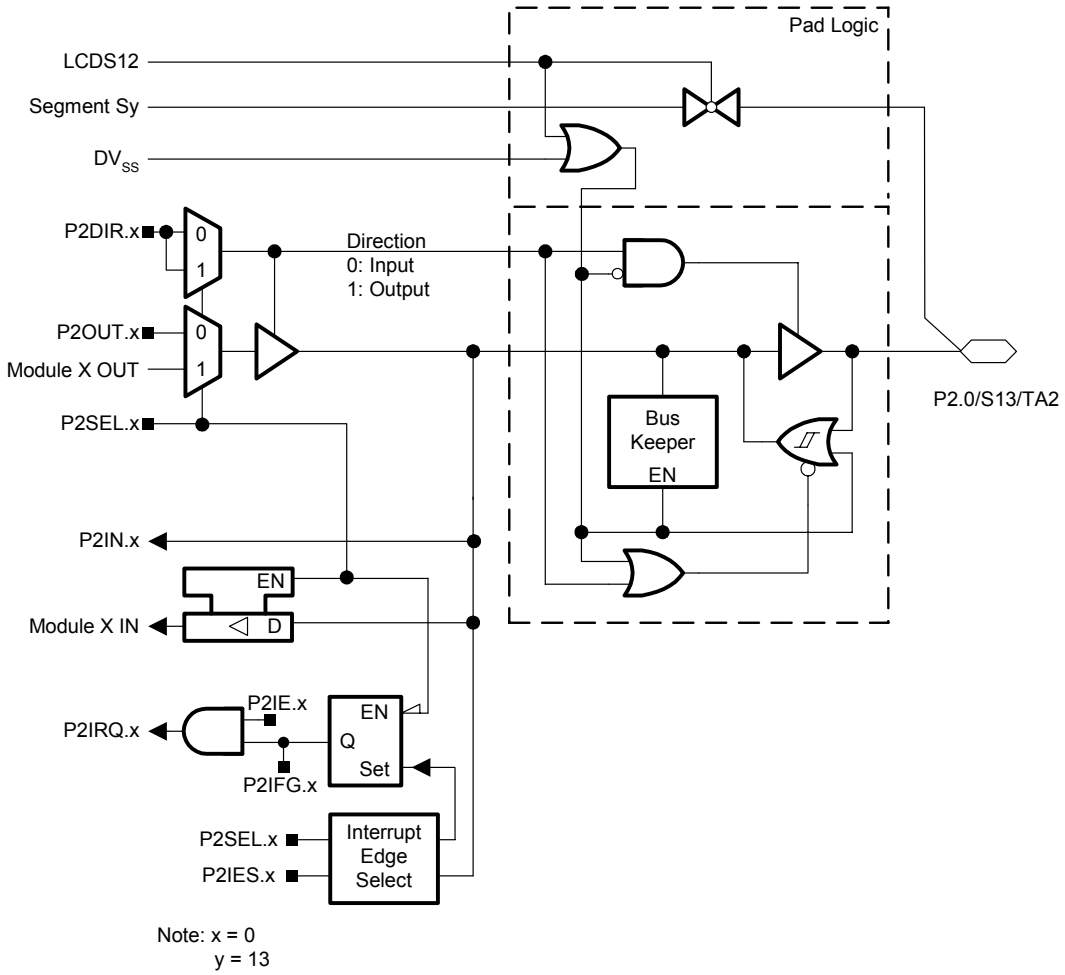
Workaround:
None

Detailed Bug Description (continued)

PORT6 PORT6 - Bug description:

Module: Port 2, P2.0 module function

In addition to GPIO and LCD functionality, P2.0 also has Timer_A3 module output capability. When P2SEL.0 = 1 and P2DIR.0 = 1, P2.0 becomes a TA2 output.



Note: x = 0
y = 13

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS12
P2.0/S13/TA2	0	P2.0 Input/Output	0/1	0	0
		N/A	0	1	0
		Timer_A3.TA2	1	1	0
		S13	X	X	1

Workaround:
N/A

Detailed Bug Description (continued)

SDA1 SDA1 - Bug description:

Module: SD16_A, Buffer always on

Input buffer continues to consume current after being disabled.
The corresponding specification is shown below:

SD16_A, power supply and recommended operating conditions

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$			2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 00; GAIN: 1,2	3 V		850	1200	µA
			SD16BUFx = 00; GAIN: 4,8,16	3 V		900	1250	
			SD16BUFx = 00; GAIN: 32	3 V		1300	1800	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	SD16BUFx = 00; GAIN: 1	3 V		800	1050	
			SD16BUFx = 00; GAIN: 32	3 V		850	1200	
		SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 01; GAIN: 1	3 V		850		
			SD16BUFx = 10; GAIN: 1	3 V		1130		
			SD16BUFx = 11; GAIN: 1	3 V		1130		
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)		3 V	0.03	0.5		

Workaround:
None

SDA3 SDA3 - Bug description:

Module: SD16_A, the interrupt delay function can result in incorrect conversion data

The interrupt delay operation can result in incorrect conversion data when SD16INTDLYx = 01, 10 or 11.

Workaround:
Use SD16INTDLYx = 00 setting (Interrupt generated after 4th conversion). This will apply to the first conversion in Continuous mode and to each conversion in Single mode.

Detailed Bug Description (continued)

TA12 TA12 - Bug description:

Module: TimerA, Function: Interrupt is lost (slow ACLK)

TimerA counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).
Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the TimerA counter has incremented again. Therefore the next compare interrupt should happen at once with the next TimerA counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:
Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description:

Module: TimerA, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:
None

WDG2 WDG2 - Bug description:

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:
None

Appendix: Prior Versions

None

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