ANALOG DEVICES

AN-588
APPLICATION NOTE

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AD7416/AD7417/AD7418 Power-On Reset Circuit

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In many applications a large number of decoupling capacitors are used on the V_{DD} line to prevent any power supply noise being coupled into ICs. As a consequence of using these noise protection capacitors, the V_{DD} line takes longer to discharge to 0 V when power is switched off. If the time between power-off and power-on is short enough, it is conceivable that the V_{DD} line would have only discharged to a value as high as 0.5 V. The effect this has on the AD7416/AD7417/AD7418 is that not all of the internal circuitry will have fully switched off. Therefore, applying power before V_{DD} has reached 0 V can cause the AD7416/AD7417/AD7418 to reset into an unknown state. Figure 1 is a recommended setup in applications where the user expects the supply voltage discharge time to be too short for a proper power-on reset of the AD7416/AD7417/AD7418.

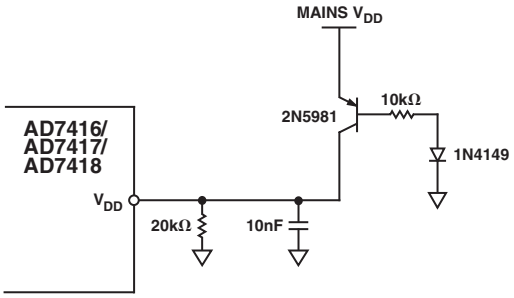

Figure 1. Power-On Reset Circuit

The PNP transistor in Figure 1 will start switching off when the main V_{DD} line connected to its emitter falls below approximately 1 V. At 0.5 V, the voltage on the AD7416/AD7417/AD7418 V_{DD} pin is virtually 0 V. This circuit will ensure that proper power-on reset is achieved when power-off, power-on time is relatively short.

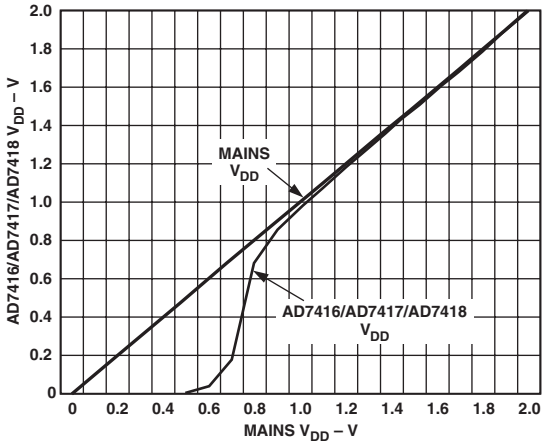

Figure 2. Voltages on Emitter and Collector of PNP Transistor in Figure 1

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