

## MSP430FW42x Device Erratasheet

### Current Version

Devices	Rev	CPU4	FLL3	SIF1	SIF2	TA12	TA16	WDG2
MSP430FW423	E	✓	✓	✓	✓	✓	✓	✓
MSP430FW425	E	✓	✓	✓	✓	✓	✓	✓
MSP430FW427	E	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

## Package Markings

**PM64: LQFP(PM) 64-pin**



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

## Detailed Bug Description

**CPU4** CPU4 - Bug description:

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:  
PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction  
PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround implemented in assembler.  
No fix planned.

**FLL3** FLL3 - Bug description:

Module: FLL+, Function: FLLDx = 11 for /8 may generate an unstable MCLK frequency

When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g., averaged over 2 seconds) as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround:  
None

**SIF1** SIF1 - Bug description:

Module: Scan Interface Module, Function: SIFCLK and MCLK dependency

When the CPU clock source MCLK is faster than the SIF clock source SIFCLK, the PSM processing state-machine output register can become corrupted and result in incorrect SIFCNT operation.

Workaround:  
None: Ensure that the MCLK frequency is slower than or equal to the frequency of SIFCLK.

**SIF2** SIF2 - Bug description:

Module: Scan Interface Module, Function: SIFACLK and TSM0 dependency

When the SIFACLK bit for the TSM0 state is set, the behavior of the TSM state machine can be unpredictable.

Workaround:  
Do not set SIFACLK in TSM0. This will shorten the duration of the TSM0 state only. If the duration of TSM0 is of concern for an application, insert a dummy state at TSM0 with a cleared SIFACLK bit and use TSM1 as the first valid user state.

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## Detailed Bug Description (continued)

**TA12** TA12 - Bug description:

Module: Timer\_A, Function: Interrupt is lost (slow ACLK)

Timer\_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK, the CCRx register increment (CCRx = CCRx+1) happens before the Timer\_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer\_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

**TA16** TA16 - Bug description:

Module: Timer\_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLK) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:

None

**WDG2** WDG2 - Bug description:

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:

None

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## Appendix: Prior Versions

Devices	Rev	CPU4	FLL3	PORT4	PORT5	PORT7	SIF1	SIF2	TA12	TA16	WDG2
MSP430FW423	E	✓	✓				✓	✓	✓	✓	✓
	D	✓	✓				✓	✓	✓	✓	✓
	C	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FW425	E	✓	✓				✓	✓	✓	✓	✓
	D	✓	✓				✓	✓	✓	✓	✓
	C	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
MSP430FW427	E	✓	✓				✓	✓	✓	✓	✓
	D	✓	✓				✓	✓	✓	✓	✓
	C	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

## Detailed Bug Description

### PORT4 Port4 - Bug description:

Module: PORT1/2, SIF - clock output depends on P2.7 AND P3.0

The SIF - clock output is not available at port P2.7 when setting P2.7 as secondary function and output as described in data sheet.

Workaround:

Set P3.0 also to alternate function and output. The SIF – clock signal is then available at P2.7.

### PORT5 Port5 - Bug description:

Module: PORT5/6, SIF - comparator output not available at P3.6

The SIF - comparator output is not available at port P6.3 when setting P6.3 as secondary function and output as described in data sheet.

Workaround:

No workaround

### PORT7 Port7 - Bug description:

Module: PORT5/6, SIFDAC output function not available at P6.6

The SIFDAC output is not available at port P6.6 when setting P6.6 as secondary function and output as described in data sheet.

Workaround:

No workaround

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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