

MSP430F42x Device Erratasheet

Current Version

Devices	Rev:	CPU4	FLL3	SD1	SD2	TA12	TA16	US15	WDG2
MSP430F425	G	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F426	G	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F427	G	✓	✓	✓	✓	✓	✓	✓	✓

Note: See Appendix for prior revisions

Package Markings

PM64: LQFP(PM) 64-pin



YM = Year and Month Date Code
 LLLL = LOT Trace Code
 S = Assembly Site Code
 # = DIE Revision
 o = PIN 1

Detailed Bug Description

CPU4 CPU4 - Bug description

Module: CPU, Function: PUSH #4, PUSH #8

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction.

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction.

Workaround implemented in assembler.

No fix planned.

FLL3 FLL3 - Bug description

Module: FLL + , Function: FLLDx = 11 for /8 may generate an unstable MCLK frequency

When setting the FLL to higher frequencies using FLLDx = 11 (/8) the output frequency of the FLL may have a larger frequency variation (e.g., averaged over 2 seconds) as well as a lower average output frequency than expected when compared to the other FLLDx bit settings.

Workaround:

None

SD1 SD1 - Bug description

Module: SD16, Function: Reduced SINAD performance if SD16 clock source is greater than 6 MHz

If the frequency of the SD16 input clock source is greater than 6 MHz, the performance of the SD16 may be degraded due to noise influencing the analog measurements under reduced SINAD.

Workaround:

Writing 0x48 to memory location 0xBF configures the SD16 for optimized performance at input clock frequencies greater than 6 MHz.

Include the following code:

```
*(unsigned char*) 0xBF = 0x48; // Write value 0x48 to memory address 0xBF
```

SD2 SD2 - Bug description

Module: SD16, Function: Internal short measurement can be influenced by external Ax.0 analog voltages

Applying a common-mode voltage other than VSS or a differential voltage to the analog inputs of the SD16 may influence the measurement accuracy when converting the internal short channel (A7). The error under these conditions is proportional to the common-mode or differential voltage and is typically 150 + LSBs.

Workaround:

Avoid applying common-mode voltages other than VSS, or a differential input voltage during the measurement of the internal short channel.

Detailed Bug Description (continued)

TA12 TA12 - Bug description

Module: Timer_A, Function: Interrupt is lost (slow ACLK)

Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TAR = CCRx).

Due to the fast MCLK, the CCRx register increment ($CCRx = CCRx + 1$) happens before the Timer_A counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

Workaround:

Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 TA16 - Bug description

Module: Timer_A, Function: First increment of TAR erroneous when IDx > 00

The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

Workaround:

None

US15 US15 - Bug description

Module: USART0, USART1, Function: UART receive with two stop bits

USART hardware does not detect a missing second stop bit when SPB = 1. The Framing Error flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround:

None (configure USART for a single stop bit, SPB = 0)

WDG2 WDG2 - Bug description

If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to a correctly generated PUC.

Workaround:

None

Appendix: Prior Versions

Devices	Rev:	CPU4	FLL3	SD1	SD2	TA12	TA16	US15	WDG2
MSP430F425	G	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F426	G	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓
MSP430F427	G	✓	✓	✓	✓	✓	✓	✓	✓
	E	✓	✓	✓	✓	✓	✓	✓	✓

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