



# CMOS Static RAM 1 Meg (128K x 8-Bit) Revolutionary Pinout

IDT71124

## Features

- ◆ 128K x 8 advanced high-speed CMOS static RAM
- ◆ JEDEC revolutionary pinout (center power/GND) for reduced noise.
- ◆ Equal access and cycle times
  - *Commercial and Industrial: 12/15/20ns*
- ◆ One Chip Select plus one Output Enable pin
- ◆ Bidirectional inputs and outputs directly TTL-compatible
- ◆ Low power consumption via chip deselect
- ◆ Available in a 32-pin 400 mil Plastic SOJ.

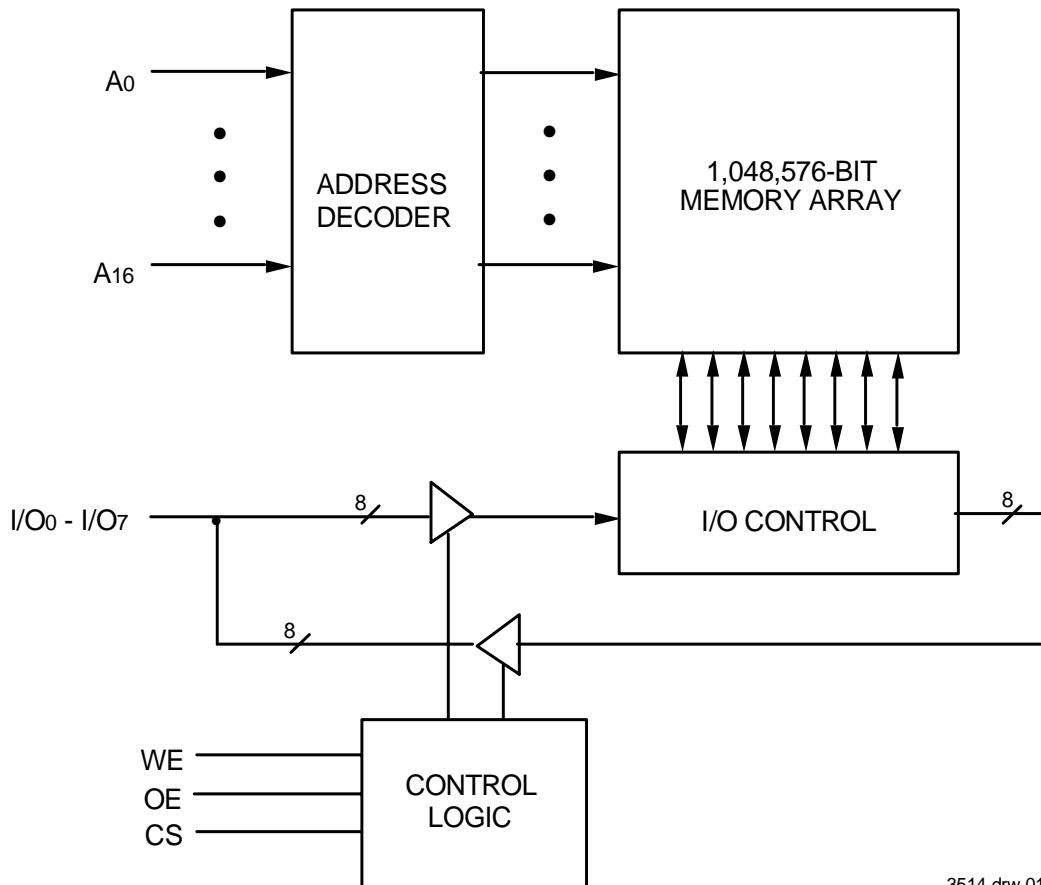
## Description

The IDT71124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC centerpower/GND pinout reduces noise generation and improves system performance.

The IDT71124 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71124 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71124 is packaged in a 32-pin 400 mil Plastic SOJ.

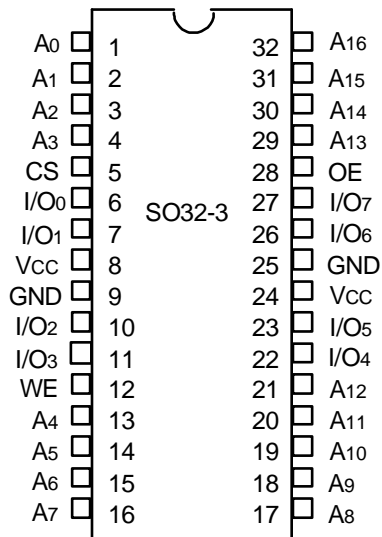
## Functional Block Diagram



3514 drw 01

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## Pin Configuration



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## SOJ Top View

## Truth Table<sup>(1,2)</sup>

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAIN	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (1sB)
VHC <sup>(3)</sup>	X	X	High-Z	Deselected - Standby (1sB1)

NOTES:

- H = V<sub>IH</sub>, L = V<sub>IL</sub>, x = Don't care.
- VLC = 0.2V, VHC = VCC - 0.2V.
- Other inputs ≥ VHC or ≤ VLC.

3514 tbl 01

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Value	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0 <sup>(2)</sup>	V
T <sub>A</sub>	Operating Temperature	0 to +70	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	°C
P <sub>T</sub>	Power Dissipation	1.25	W
I <sub>OUT</sub>	DC Output Current	50	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>CC</sub> + 0.5V.

## Capacitance (T<sub>A</sub> = +25°C, f = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 3dV	8	pF

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NOTE:

- This parameter is guaranteed by device characterization, but is not production tested.

## Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	V <sub>CC</sub>
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3514 tbl 04

## Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	---	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	---	0.8	V

3514 tbl 05

## DC Electrical Characteristics

(V<sub>CC</sub> = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	—	5	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS} = V_{IH}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8mA, V <sub>CC</sub> = Min.	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = Min.	2.4	—	V

3514 tbl 06

## DC Electrical Characteristics<sup>(1)</sup>

(V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

Symbol	Parameter	71124S12		71124S15		71124S20		Unit
		Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I <sub>CC</sub>	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>	160	160	155	155	140	140	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(2)</sup>	40	40	40	40	40	40	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$ , Outputs Open, V <sub>CC</sub> = Max., f = 0 <sup>(2)</sup> V <sub>IN</sub> ≤ V <sub>LC</sub> or V <sub>IN</sub> ≥ V <sub>HC</sub>	10	10	10	10	10	10	mA

3514 tbl 07

### NOTES:

- All values are maximum guaranteed values.
- f<sub>MAX</sub> = 1/trc (all address inputs are cycling at f<sub>MAX</sub>): f = 0 means no address input lines are changing.

## AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1 and 2

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## AC Test Loads

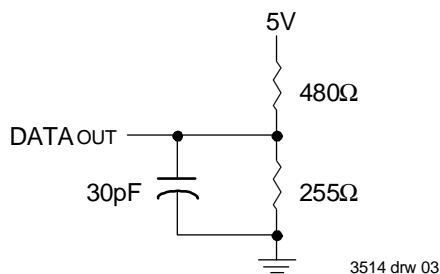
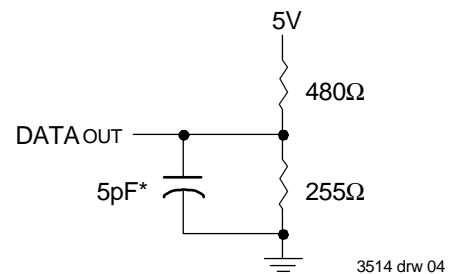


Figure 1. AC Test Load



\*Including jig and scope capacitance.

Figure 2. AC Test Load  
(for t<sub>CLZ</sub>, t<sub>OLZ</sub>, t<sub>CHZ</sub>, t<sub>OHZ</sub>, t<sub>ow</sub>, and t<sub>whz</sub>)

## AC Electrical Characteristics (Vcc = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

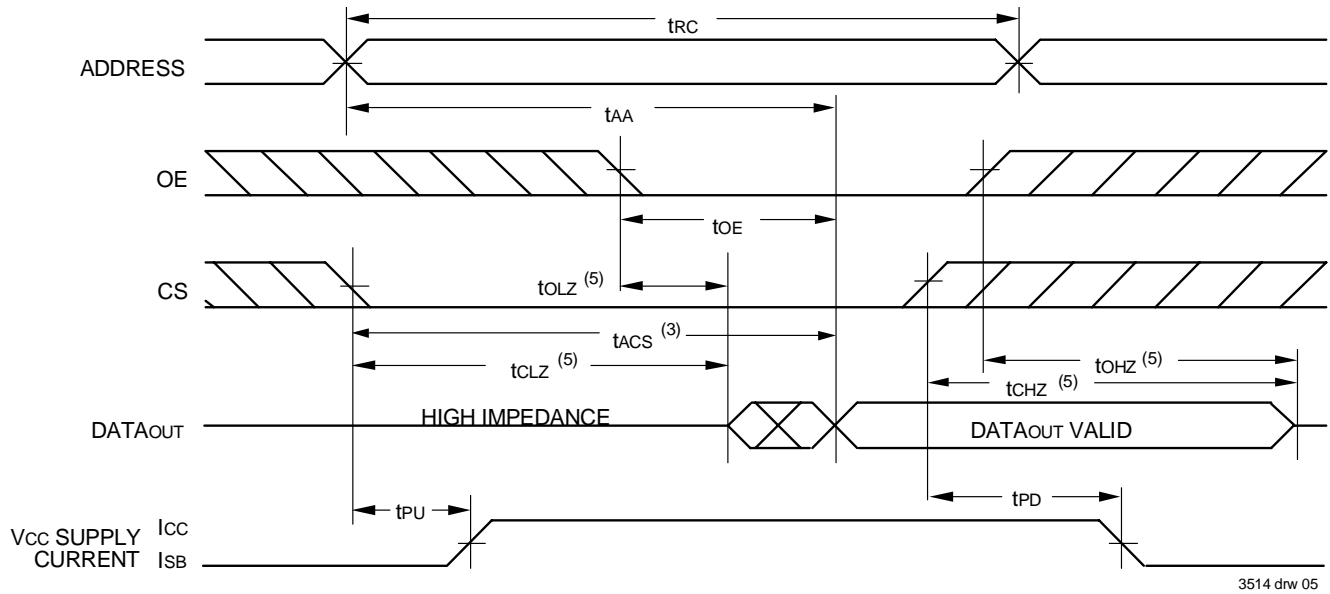
Symbol	Parameter	71124S12		71124S15		71124S20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>								
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	20	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	20	ns
t <sub>ACS</sub>	Chip Select Access Time	—	12	—	15	—	20	ns
t <sub>CLZ</sub> <sup>(1)</sup>	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t <sub>CHZ</sub> <sup>(1)</sup>	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	6	—	7	—	8	ns
t <sub>OLZ</sub> <sup>(1)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(1)</sup>	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t <sub>OH</sub>	Output Hold from Address Change	4	—	4	—	4	—	ns
t <sub>PU</sub> <sup>(1)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(1)</sup>	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
<b>WRITE CYCLE</b>								
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	20	—	ns
t <sub>AW</sub>	Address Valid to End of Write	8	—	12	—	15	—	ns
t <sub>CW</sub>	Chip Select to End of Write	8	—	12	—	15	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	8	—	12	—	15	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	6	—	8	—	9	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(1)</sup>	Output active from End-of-Write	3	—	3	—	4	—	ns
t <sub>WHZ</sub> <sup>(1)</sup>	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

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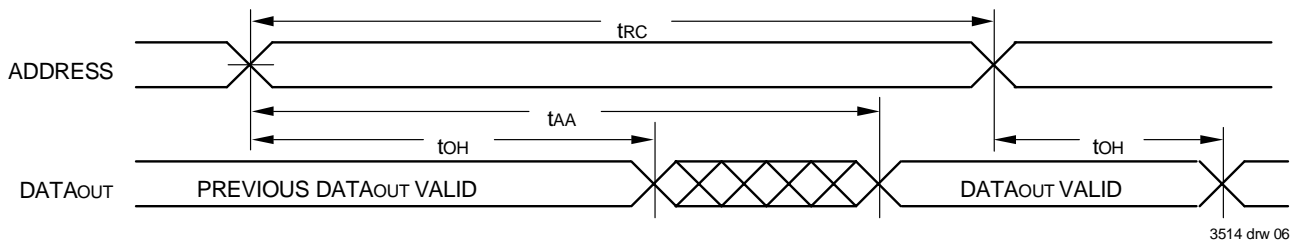
**NOTE:**

1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

## Timing Waveform of Read Cycle No. 1<sup>(1)</sup>



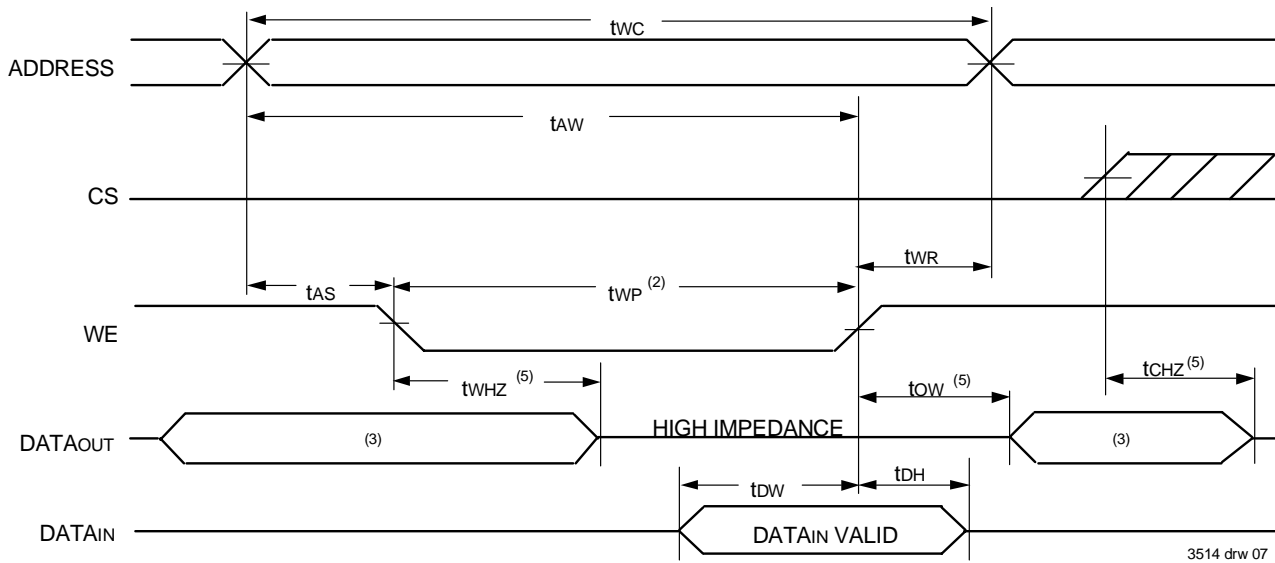
## Timing Waveform of Read Cycle No. 2<sup>(1,2,4)</sup>



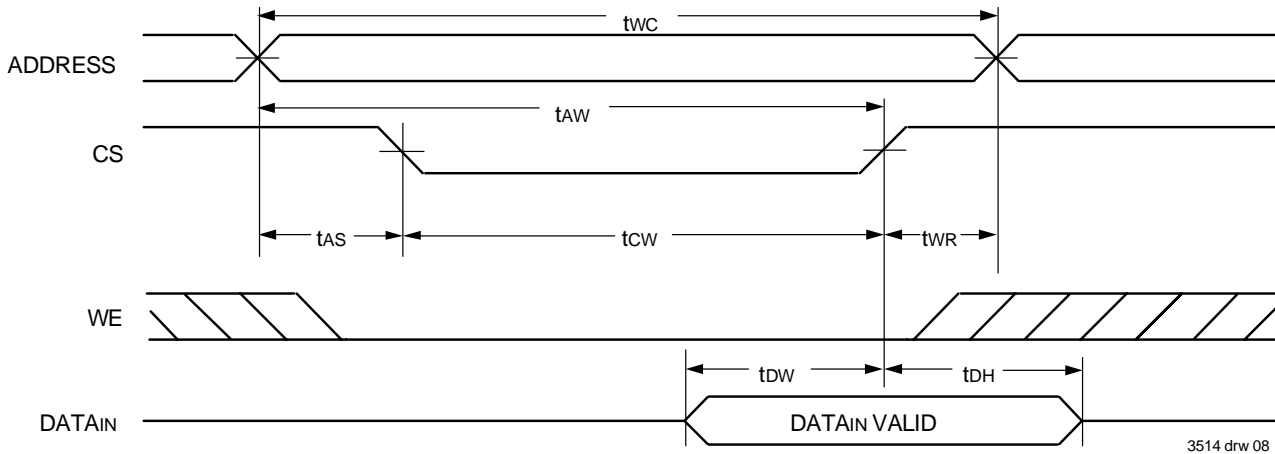
### NOTES:

1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS}$  is LOW.
3. Address must be valid prior to or coincident with the later of  $\overline{CS}$  transition LOW; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is LOW.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

### Timing Waveform of Write Cycle No. 1 ( $\overline{WE}$ Controlled Timing)<sup>(1,2,4)</sup>



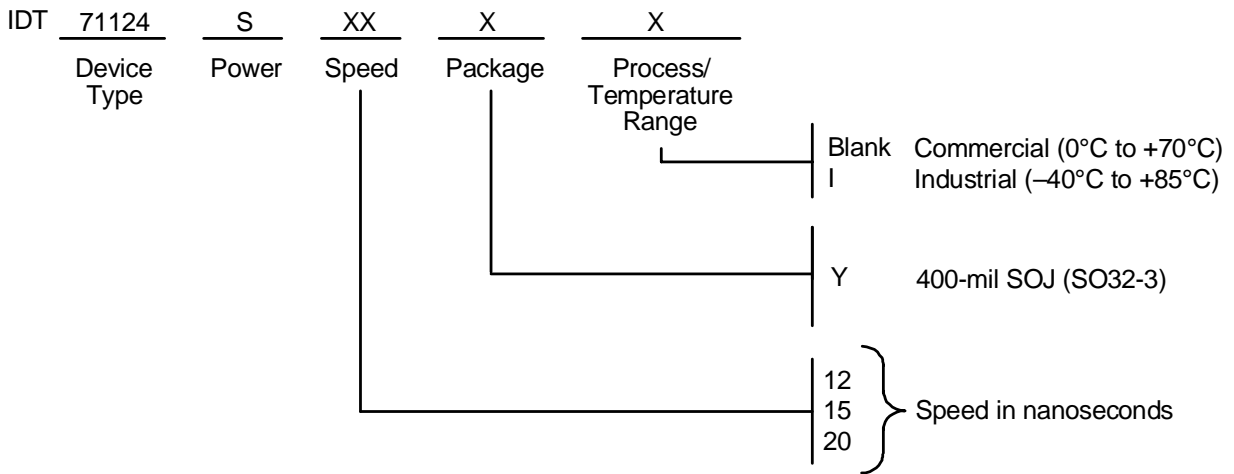
### Timing Waveform of Write Cycle No. 2 ( $\overline{CS}$ Controlled Timing)<sup>(1,4)</sup>



**NOTES:**

1. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
2.  $\overline{OE}$  is continuously HIGH. During a  $\overline{WE}$  controlled write cycle with  $\overline{OE}$  LOW,  $t_{WP}$  must be greater than or equal to  $t_{WHZ} + t_{OW}$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{DW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is the specified  $t_{WP}$ .
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.  $\overline{CS}$  must be active during the  $t_{CW}$  write period.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

## Ordering Information



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## Datasheet Document History

8/5/99		Updated to new format
	Pg. 3	Removed military entries on DC table
	Pg. 4	Removed Note 1 and renumbered footnotes
	Pg. 6	Revised footnotes on Write Cycle No. 1 diagram
8/13/99	Pg. 8	Added Datasheet Document History
9/30/99	Pg. 1, 3, 4, 7	Added 12ns, 15ns, and 20ns industrial temperature speed grade offerings
2/18/00	Pg. 3	Revise LSB for Industrial Temperature offerings to meet commercial specifications
3/14/00	Pg. 3	Revised LSB to accommodate speed functionality
4/01/00	Pg.4	Tightened tAW, tCW, tWP and tDW within the AC Electrical Characteristics
8/09/00		Not recommended for new designs
02/01/01		Removed "Not recommended for new designs"



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