



128K X 8 BIT SUPER LOW POWER CMOS SRAM

FEATURES

- Fast access time : 35/55ns
- Low power consumption:
Operating current : 12/10/7mA (TYP.)
Standby current : 1 μ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 1.5V (MIN.)
- **Lead free and green package available**
- Package : 32-pin 450 mil SOP
32-pin 600 mil P-DIP
32-pin 8mm x 20mm TSOP-I
32-pin 8mm x 13.4mm STSOP
36-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

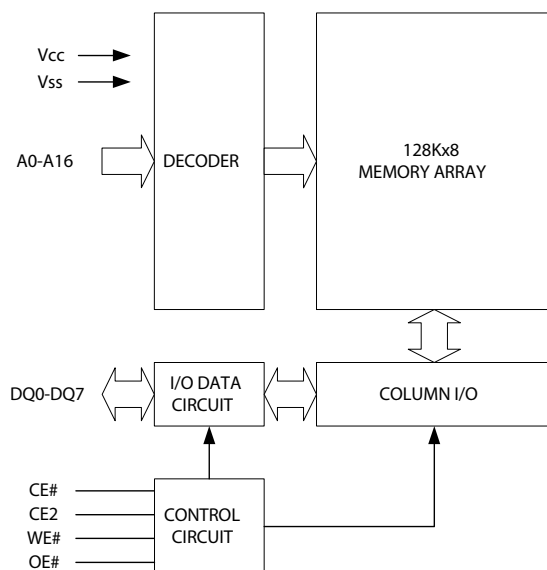
The AS6C1008 is a 1,048,576-bit low power CMOS static random access memory organized as 131,072 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C1008 is well designed for very low power system applications, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C1008-55 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed
AS6C1008	-40 ~ 85°C	2.7 ~ 5.5V	35/55ns

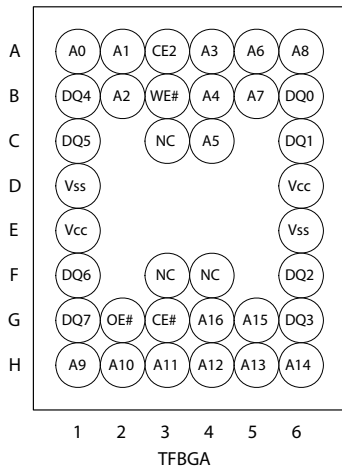
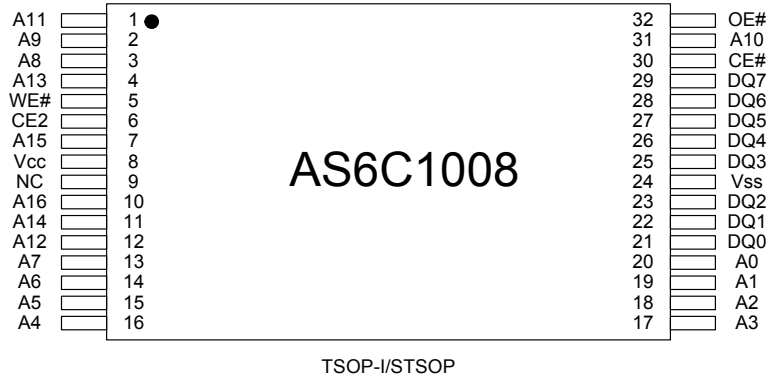
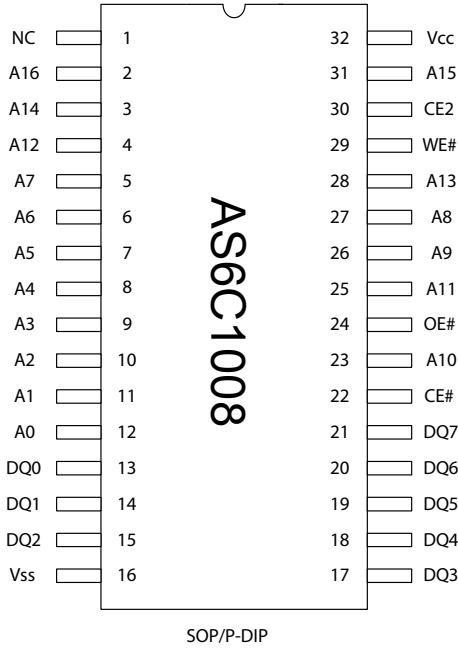
FUNCTIONAL BLOCK DIAGRAM**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V _{TERM}	-0.5 to 7.0	V
Operating Temperature	T _A	-40 to 85(I grade)	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{SOLDER}	260	°C



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*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC} , I _{CC1}
Read	L	H	L	H	D _{OUT}	I _{CC} , I _{CC1}
Write	L	H	X	L	D _{IN}	I _{CC} , I _{CC1}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT
Supply Voltage	V _{CC}		2.7	3.0	5.5	V
Input High Voltage	V _{IH} ¹		0.7*V _{CC}	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ²		-0.2	-	0.6	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA	-35	12	80	mA
			-55	10	60	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	1	10	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V	-SL	1	10	μA
		or CE2 ≤ 0.2V	-SLE/-SLI	1	10	μA
		Other pins at 0.2V	-LL	1	20	μA
		or V _{CC} -0.2V	-LLE/-LLI	1	50	μA

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C



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CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 50\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -1\text{mA}/2\text{mA}$

AC ELECTRICAL CHARACTERISTICS**(1) READ CYCLE**

PARAMETER	SYM.	AS6C1008		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	ns
Address Access Time	t_{AA}	-	35	ns
Chip Enable Access Time	t_{ACE}	-	35	ns
Output Enable Access Time	t_{OE}	-	25	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	10	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	5	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	15	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	15	ns
Output Hold from Address Change	t_{OH}	10	-	ns

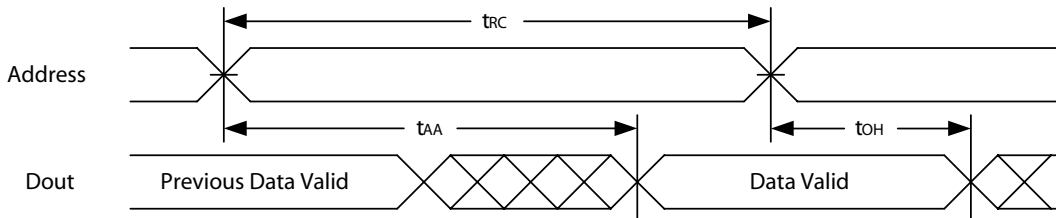
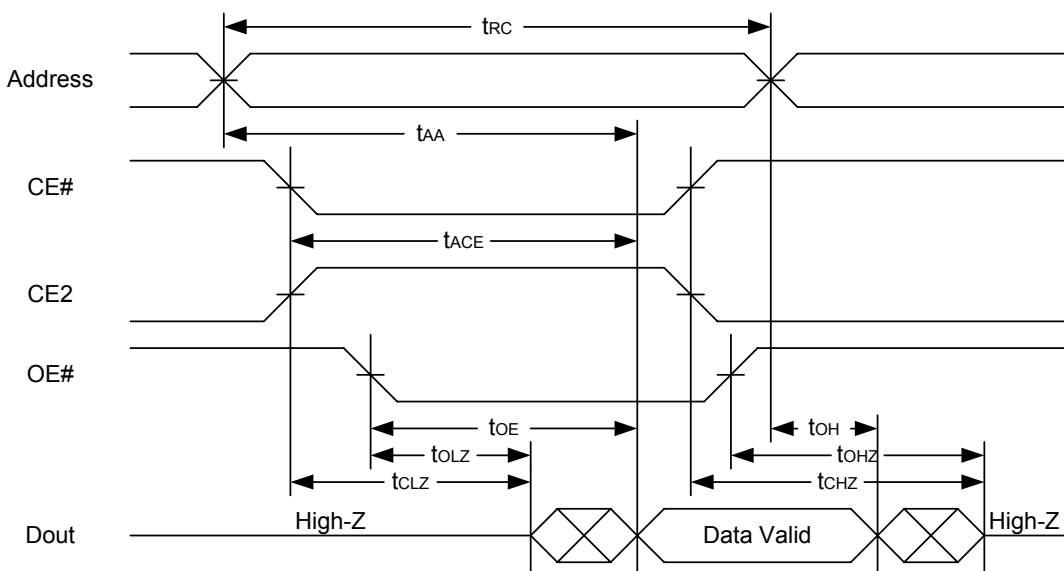
(2) WRITE CYCLE

PARAMETER	SYM.	AS6C1008		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	ns
Address Valid to End of Write	t_{AW}	30	-	ns
Chip Enable to End of Write	t_{CW}	30	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	25	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	5	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	15	ns

*These parameters are guaranteed by device characterization, but not production tested.



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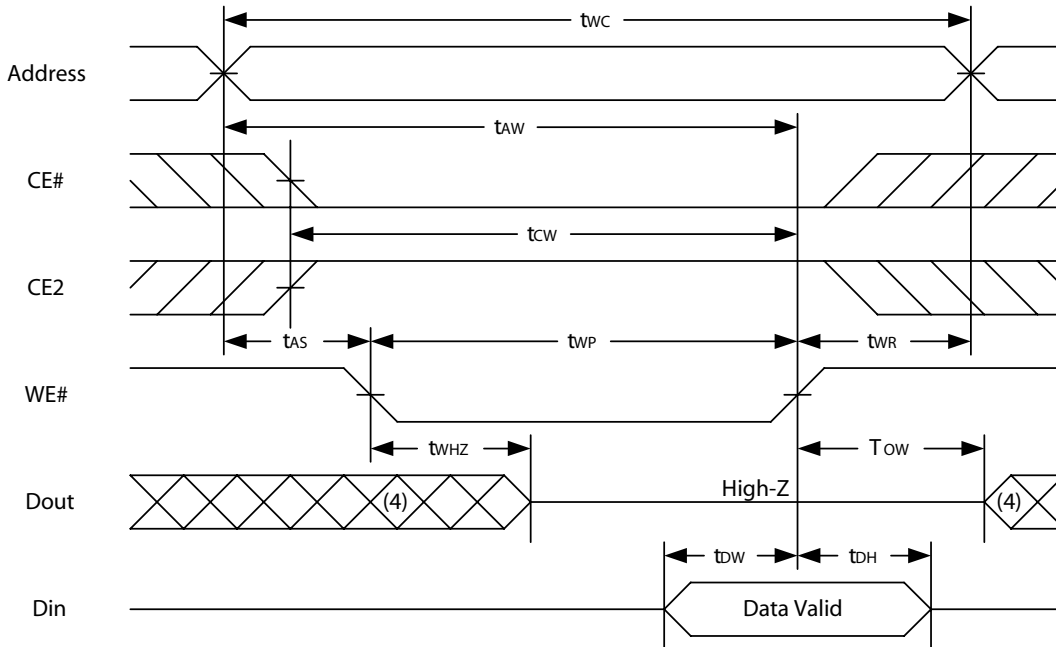
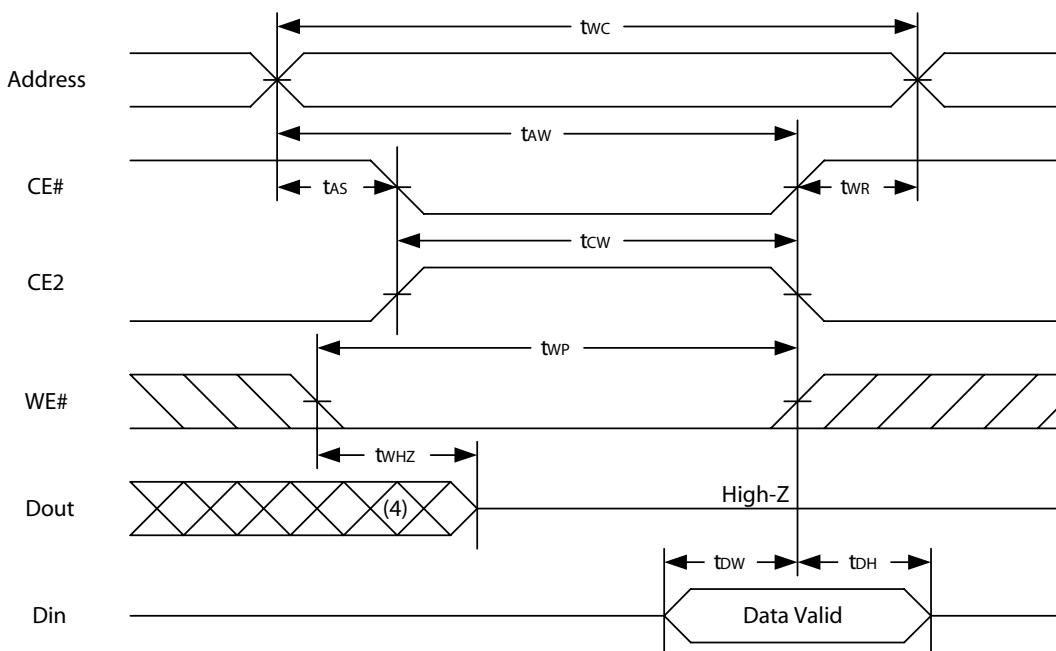
TIMING WAVEFORMS**READ CYCLE 1 (Address Controlled) (1,2)****READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)**

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.



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WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)****Notes :**

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



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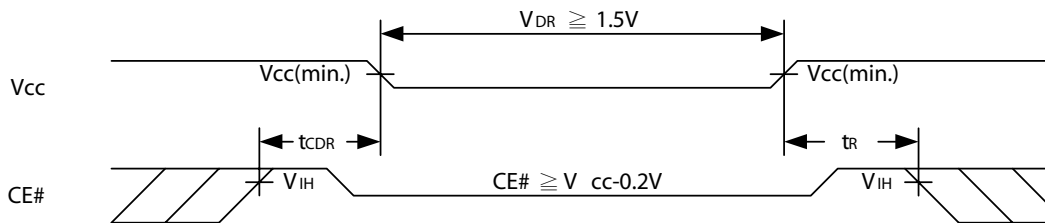
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V _{DR}	CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V	1.5	-	5.5	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V others at 0.2V or V _{CC} -0.2V	-SL	-	0.5	8	μA
			-SLE/-SLI	-	0.5	8	μA
			-LLI	-	0.5	30	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _r		t _{RC*}	-	-	ns	

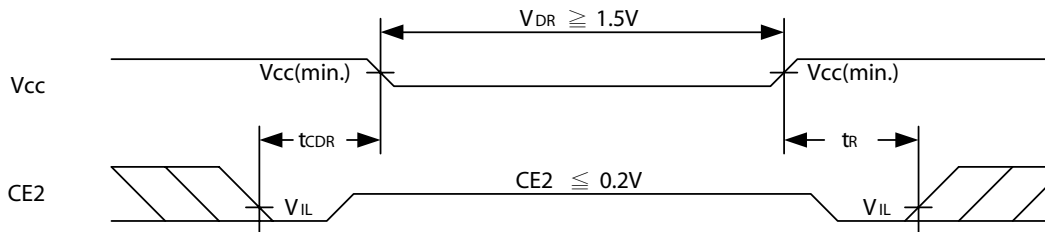
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)



Low Vcc Data Retention Waveform (2) (CE2 controlled)

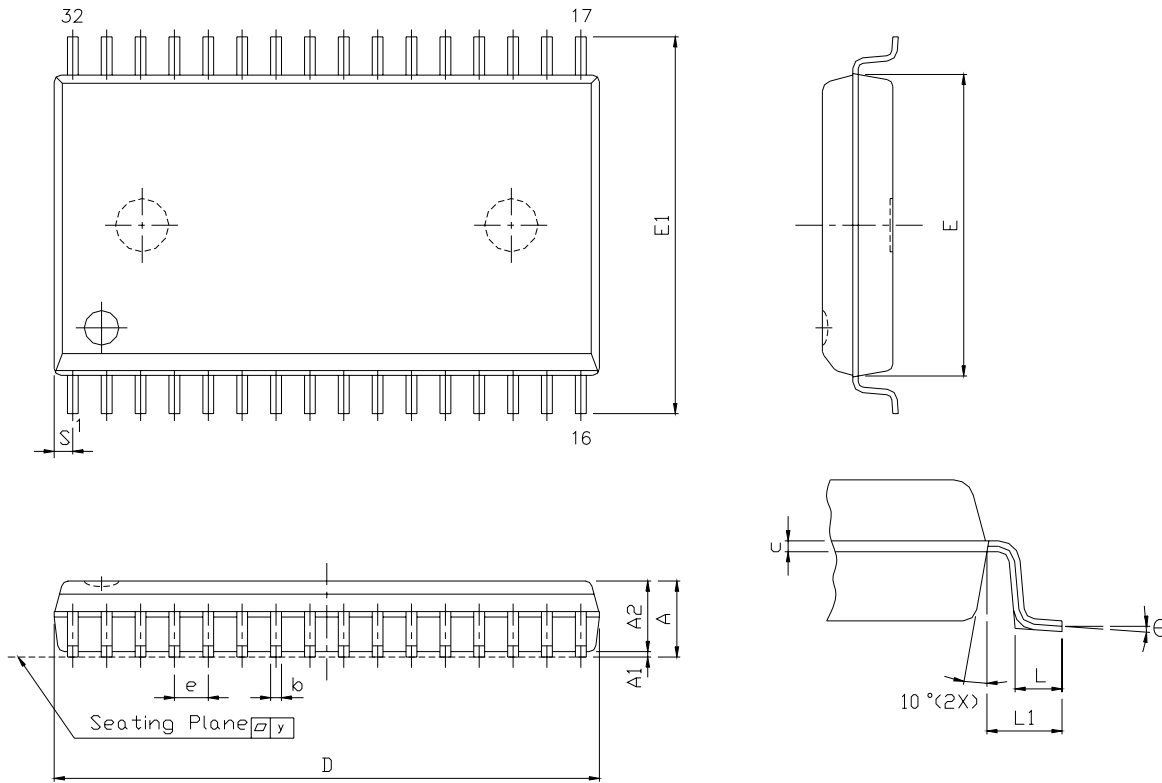




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PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension

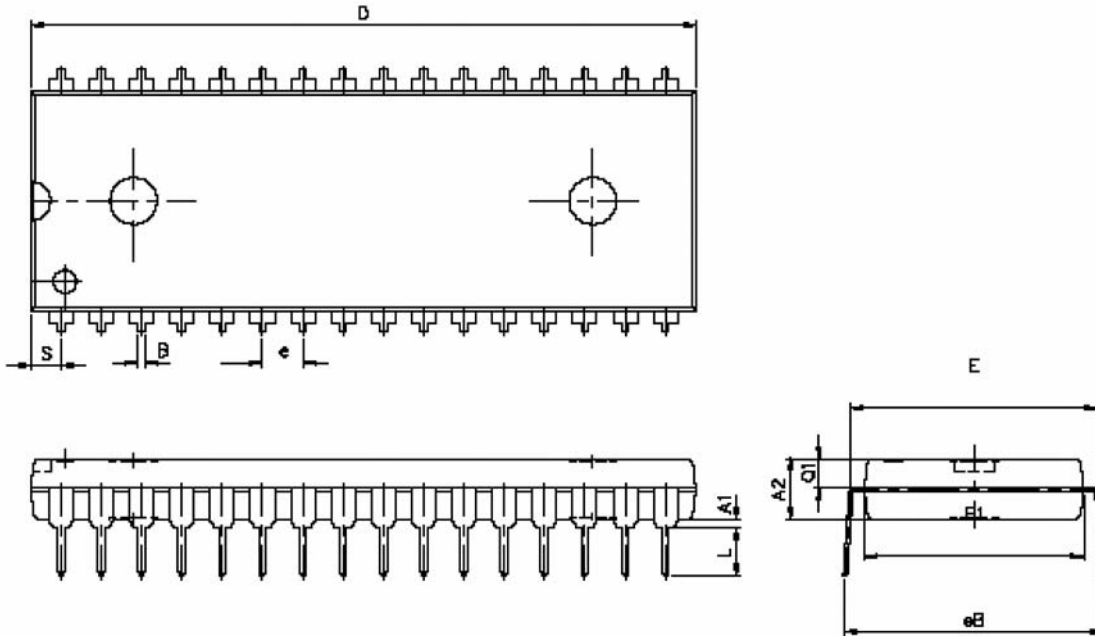


SYM.	UNIT	INCH.(BASE)	MM(REF)
A		0.118 (MAX)	2.997 (MAX)
A1		0.004(MIN)	0.102(MIN)
A2		0.111(MAX)	2.82(MAX)
b		0.016(TYP)	0.406(TYP)
c		0.008(TYP)	0.203(TYP)
D		0.817(MAX)	20.75(MAX)
E		0.445 ±0.005	11.303 ±0.127
E1		0.555 ±0.012	14.097 ±0.305
e		0.050(TYP)	1.270(TYP)
L		0.0347 ±0.008	0.881 ±0.203
L1		0.055 ±0.008	1.397 ±0.203
S		0.026(MAX)	0.660 (MAX)
y		0.004(MAX)	0.101(MAX)
?		0° -10°	0° -10°



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32 pin 600 mil P-DIP Package Outline Dimension



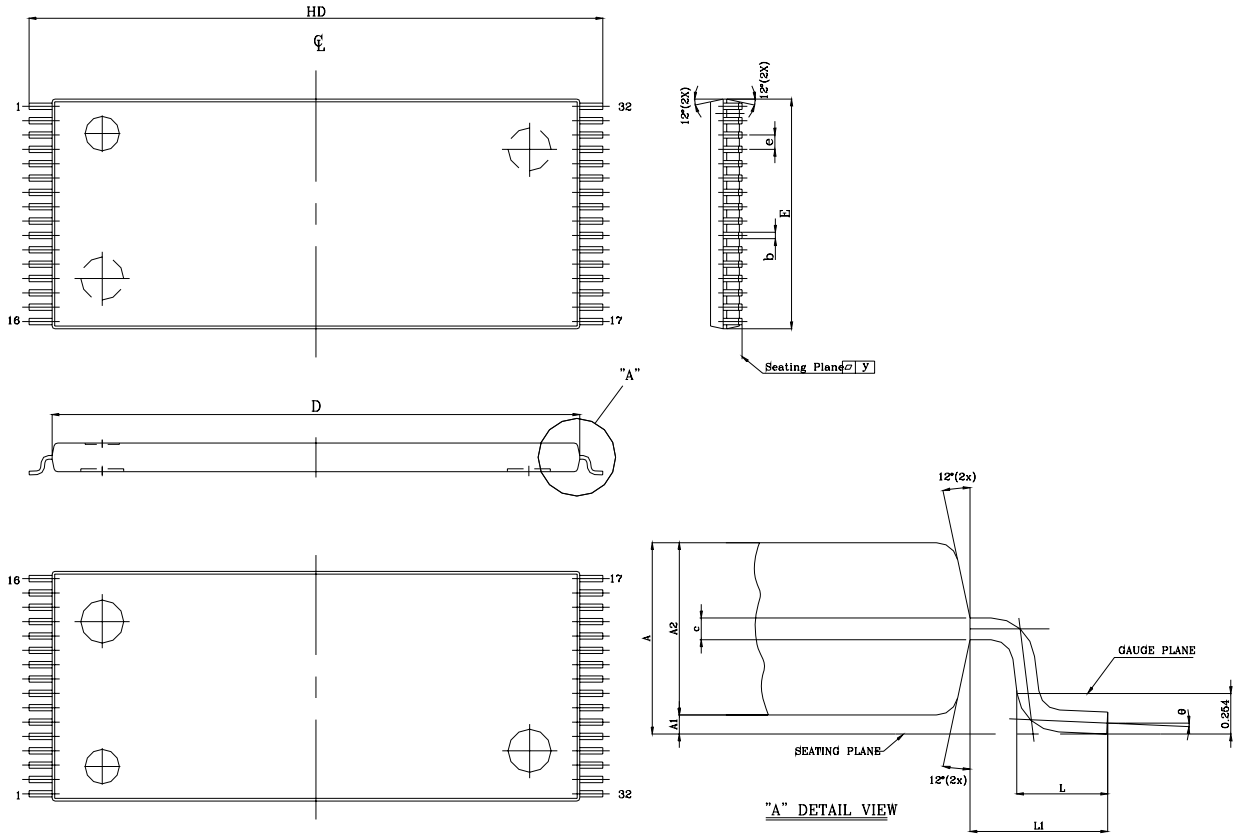
SYM.	UNIT	INCH(BASE)	MM(REF)
A1		0.001 (MIN)	0.254 (MIN)
A2		0.150 ± 0.005	3.810 ± 0.127
B		0.018 ± 0.005	0.457 ± 0.127
D		1.650 ± 0.005	41.910 ± 0.127
E		0.600 ± 0.010	15.240 ± 0.254
E1		0.544 ± 0.004	13.818 ± 0.102
e		0.100 (TYP)	2.540 (TYP)
eB		0.640 ± 0.020	16.256 ± 0.508.
L		0.130 ± 0.010	3.302 ± 0.254
S		0.075 ± 0.010	1.905 ± 0.254
Q1		0.070 ± 0.005	1.778 ± 0.127

Note : D/E1/S dimension do not include mold flash.



128K X 8 BIT SUPER LOW POWER CMOS SRAM

32 pin 8mm x 20mm TSOP-I Package Outline Dimension

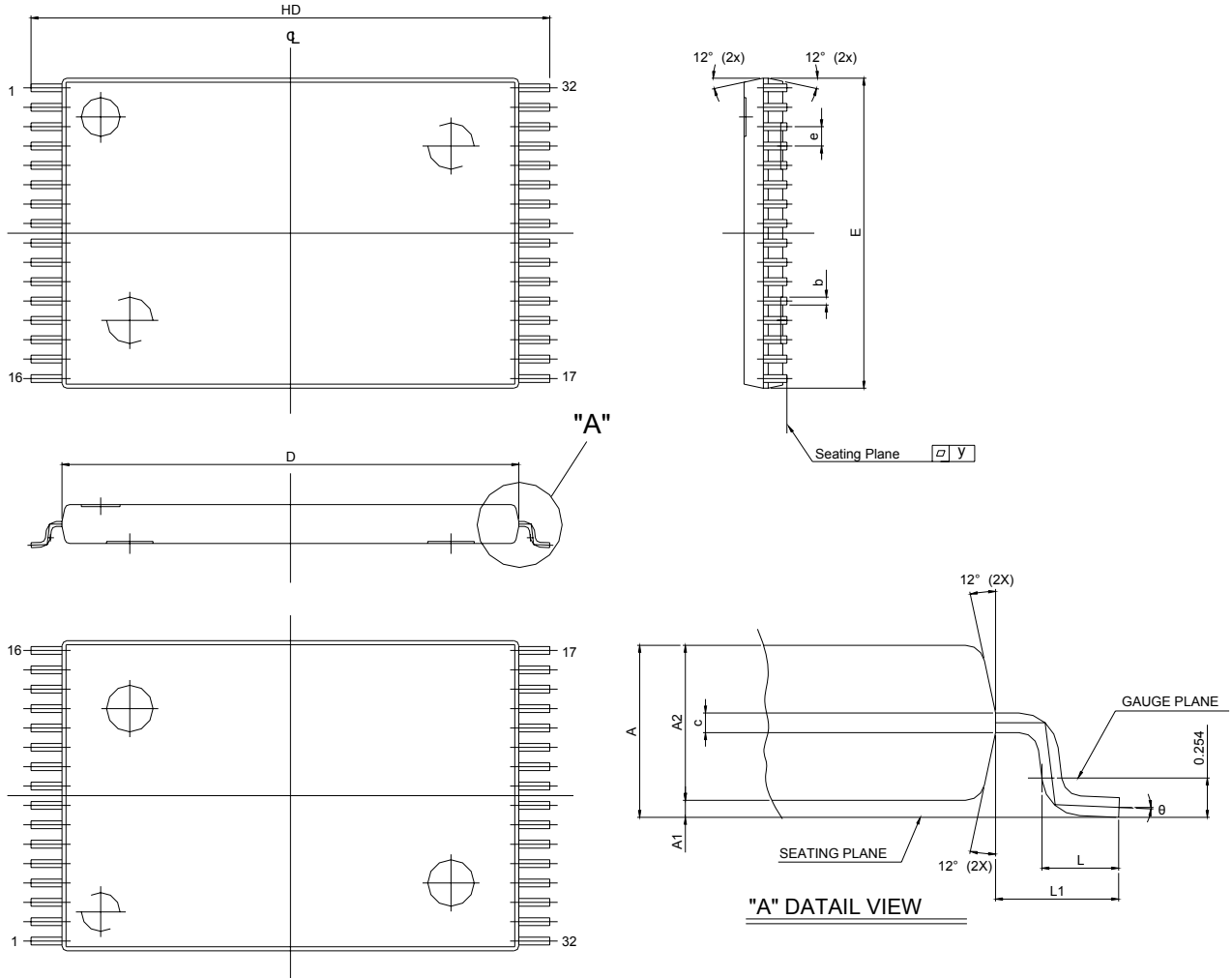


SYM. \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 - 0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.08 ±0.10
y	0.003 (MAX)	0.076 (MAX)
∅	0° ~ 5°	0° ~ 5°



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32 pin 8mm x 13.4mm STSOP Package Outline Dimension

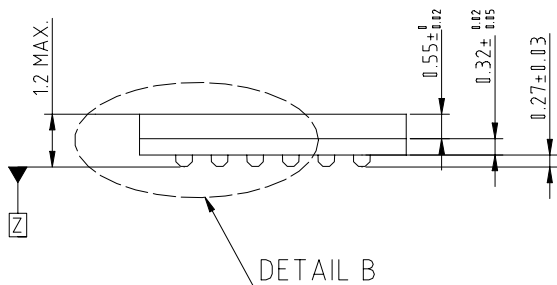
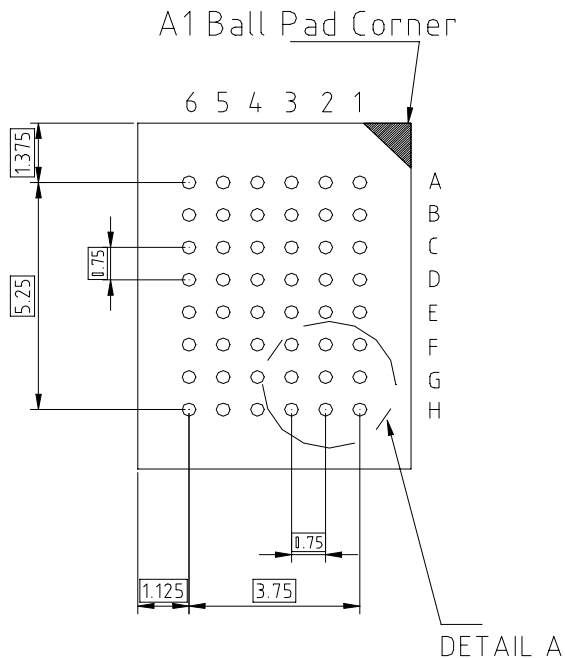
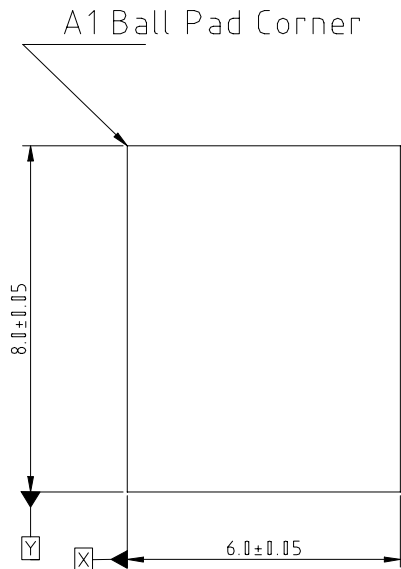


SYM.	UNIT	INCH(BASE)	MM(REF)
A		0.049 (MAX)	1.25 (MAX)
A1		0.005 ±0.002	0.130 ±0.05
A2		0.039 ±0.002	1.00 ±0.05
b		0.008 ±0.01	0.20±0.025
c		0.005 (TYP)	0.127 (TYP)
D		0.465 ±0.004	11.80 ±0.10
E		0.315 ±0.004	8.00 ±0.10
e		0.020 (TYP)	0.50 (TYP)
HD		0.528±0.008	13.40 ±0.20.
L		0.0197 ±0.004	0.50 ±0.10
L1		0.0315 ±0.004	0.8 ±0.10
y		0.003 (MAX)	0.076 (MAX)
θ		0°~5°	0°~5°

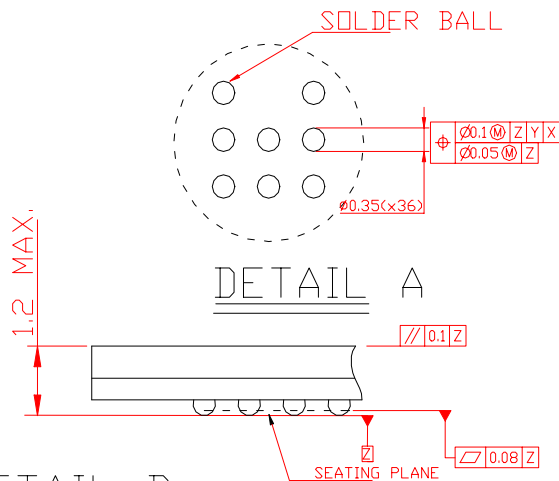


128K X 8 BIT SUPER LOW POWER CMOS SRAM

36 ball 6mm x 8mm TFBGA Package Outline Dimension



SIDE VIEW



DETAIL B



128K X 8 BIT SUPER LOW POWER CMOS SRAM

ORDERING INFORMATION

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C1008-55SIN	128K x 8	2.7 - 5.5V	32 pin 450mil SOP	Industrial ~ -40 F - 85 F	55
AS6C1008-55TIN	128K x 8	2.7 - 5.5V	32 pin TSOP-1(8x20mm)	Industrial ~ -40 F - 85 F	55
AS6C1008-55STIN	128K x 8	2.7 - 5.5V	32 pin stSOP (8x13.3mm)	Industrial ~ -40 F - 85 F	55

PART NUMBERING SYSTEM

AS6C	1008	-55	X	X	N	L
SRAM prefix	Device Number 10 = 1M 08 = x8	Access Time	Package Option 32 pin 450mil SOP 32 pin TSOP-1(8x20mm) 32 pin stSOP (8x13.3mm)	Temperature Range I = Industrial (-40 to + 85 C)	N = Lead Free RoHS compliant part	super low power



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