



## 64K X 16 BIT LOW POWER CMOS SRAM

**FEATURES**

- Fast access time : 55ns
- Low power consumption:  
Operating current : 20/18mA (TYP.)  
Standby current : 2 $\mu$ A (TYP.)
- Single 2.7V ~ 5.5V power supply
- All outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)  
UB# (DQ8 ~ DQ15)
- Data retention voltage : 2.0V (MIN.)
- **Lead free and green package available**
- Package : 44-pin 400 mil TSOP-II  
48-ball 6mm x 8mm TFBGA

**PRODUCT FAMILY****GENERAL DESCRIPTION**

The AS6C1016 is a 1,048,576-bit low power CMOS static random access memory organized as 65,536 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C1016 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

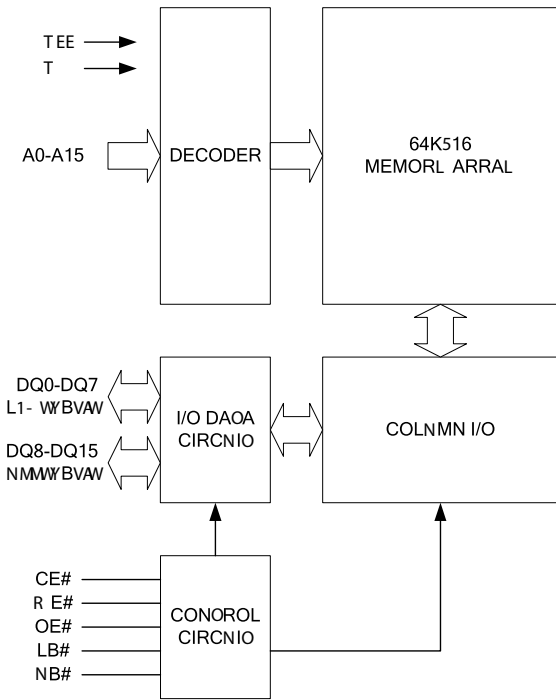
The AS6C1016 operates from a single power supply of 2.7V ~ 5.5V and all inputs and outputs are fully TTL compatible

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby( $I_{SB1}$ , TYP.)	Operating( $I_{CC}$ , TYP.)
AS6C1016(I)	-40 ~ 85°C	2.7 ~ 5.5V	55ns	2 $\mu$ A	20/18mA



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**FUNCTIONAL BLOCK DIAGRAM**



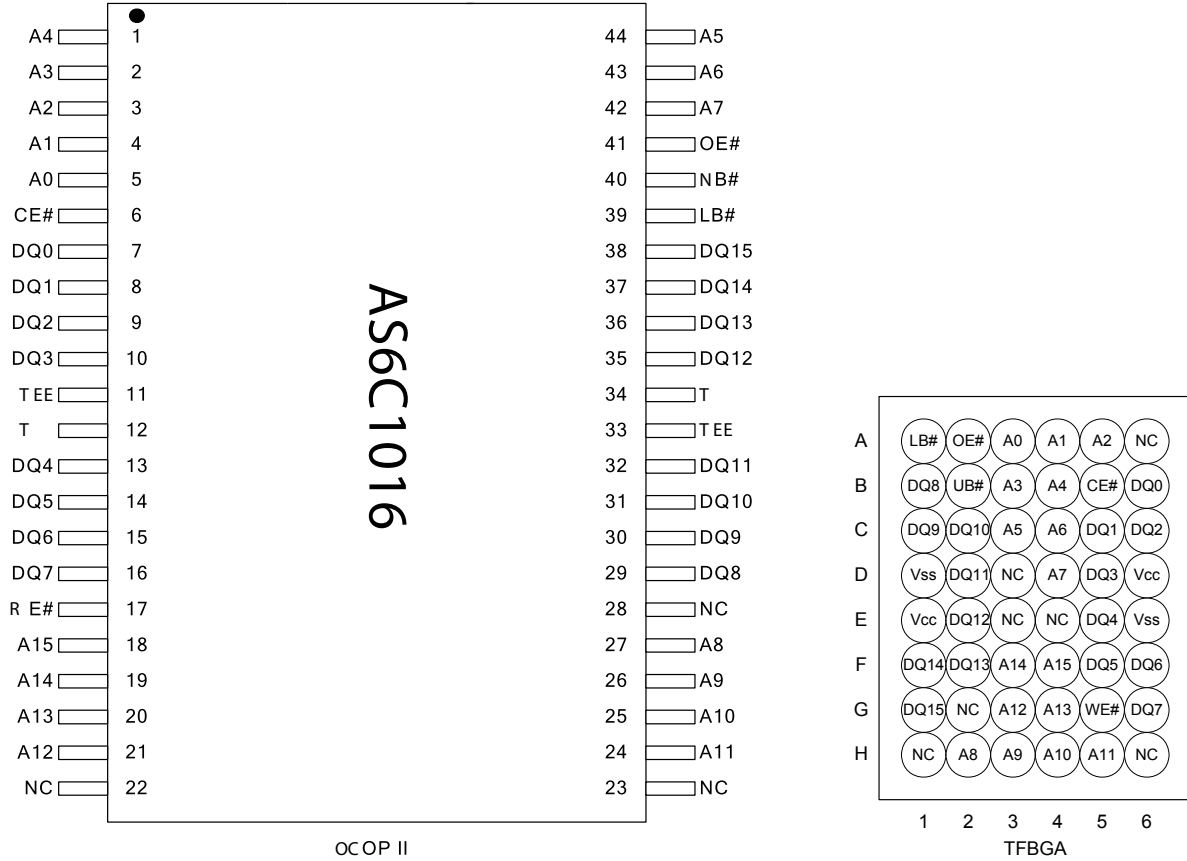
**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground



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**PIN CONFIGURATION**



**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V <sub>T1</sub>	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V <sub>T2</sub>	-0.5 to Vcc+0.5	V
Operating Temperature	T <sub>A</sub>	-40 to 85(I grade)	°C
Storage Temperature	T <sub>STG</sub>	-65 to 150	°C
Power Dissipation	P <sub>D</sub>	1	W
DC Output Current	I <sub>OUT</sub>	50	mA
Soldering Temperature (under 10 sec)	T <sub>SOLDER</sub>	260	°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.



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**TRUTH TABLE**

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High - Z	High - Z	I <sub>SB1</sub>
	X	X	X	H	H	High - Z	High - Z	
Output Disable	L	H	H	L	X	High - Z	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	H	H	X	L	High - Z	High - Z	
Read	L	L	H	L	H	D <sub>OUT</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	L	H	H	L	High - Z	D <sub>OUT</sub>	
	L	L	H	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	
Write	L	X	L	L	H	D <sub>IN</sub>	High - Z	I <sub>CC</sub> , I <sub>CC1</sub>
	L	X	L	H	L	High - Z	D <sub>IN</sub>	
	L	X	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	

Note: H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't care.

**DC ELECTRICAL CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. <sup>4</sup>	MAX.	UNIT	
Supply Voltage	V <sub>CC</sub>		2.7	3.0	5.5	V	
Input High Voltage	V <sub>IH</sub> <sup>1</sup>		0.7*V <sub>CC</sub>	-	V <sub>CC</sub> +0.3	V	
Input Low Voltage	V <sub>IL</sub> <sup>2</sup>		-0.2	-	0.6	V	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> ≥ V <sub>IN</sub> ≥ V <sub>SS</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	V <sub>CC</sub> ≥ V <sub>OUT</sub> ≥ V <sub>SS</sub> , Output Disabled	-1	-	1	μA	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1mA	2.4	2.7	-	V	
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I <sub>CC</sub>	Cycle time = Min., I <sub>I/O</sub> = 0mA	-55	-	20	60	mA
		CE# = 0.2V, Others at 0.2V or V <sub>CC</sub> -0.2V	-70	-	18	50	mA
	I <sub>CC1</sub>	Cycle time = 1μs CE# = 0.2V, I <sub>I/O</sub> = 0mA Other pins at 0.2V or V <sub>CC</sub> - 0.2V	-	-	4	10	mA
Standby Power Supply Current	I <sub>SB1</sub>	CE# ≥ V <sub>CC</sub> - 0.2V Others at 0.2V or V <sub>CC</sub> - 0.2V	-	-	2	50	μA

Notes:

- V<sub>IH</sub>(max) = V<sub>CC</sub> + 3.0V for pulse width less than 10ns.
- V<sub>IL</sub>(min) = V<sub>SS</sub> - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.  
Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(TYP.) and T<sub>A</sub> = 25°C

**CAPACITANCE (T<sub>A</sub> = 25°C, f = 1.0MHz)**

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.



## 64K X 16 BIT LOW POWER CMOS SRAM

**AC TEST CONDITIONS**

Input Pulse Levels	0.2V to $V_{CC} - 0.2V$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30pF + 1TTL, I_{OH}/I_{OL} = -2mA/4mA$

**AC ELECTRICAL CHARACTERISTICS****(1) READ CYCLE**

PARAMETER	SYM.	AS6C1016-55		UNIT
		MIN.	MAX.	
Read Cycle Time	$t_{RC}$	55	-	ns
Address Access Time	$t_{AA}$	-	55	ns
Chip Enable Access Time	$t_{ACE}$	-	55	ns
Output Enable Access Time	$t_{OE}$	-	30	ns
Chip Enable to Output in Low-Z	$t_{CLZ}^*$	10	-	ns
Output Enable to Output in Low-Z	$t_{OLZ}^*$	5	-	ns
Chip Disable to Output in High-Z	$t_{CHZ}^*$	-	20	ns
Output Disable to Output in High-Z	$t_{OHZ}^*$	-	20	ns
Output Hold from Address Change	$t_{OH}$	10	-	ns
LB#, UB# Access Time	$t_{BA}$	-	55	ns
LB#, UB# to High-Z Output	$t_{BHZ}^*$	-	25	ns
LB#, UB# to Low-Z Output	$t_{BLZ}^*$	10	-	ns

**(2) WRITE CYCLE**

PARAMETER	SYM.	AS6C1016-55		UNIT
		MIN.	MAX.	
Write Cycle Time	$t_{WC}$	55	-	ns
Address Valid to End of Write	$t_{AW}$	50	-	ns
Chip Enable to End of Write	$t_{CW}$	50	-	ns
Address Set-up Time	$t_{AS}$	0	-	ns
Write Pulse Width	$t_{WP}$	45	-	ns
Write Recovery Time	$t_{WR}$	0	-	ns
Data to Write Time Overlap	$t_{DW}$	25	-	ns
Data Hold from End of Write Time	$t_{DH}$	0	-	ns
Output Active from End of Write	$t_{OW}^*$	5	-	ns
Write to Output in High-Z	$t_{WHZ}^*$	-	20	ns
LB#, UB# Valid to End of Write	$t_{BW}$	50	-	ns

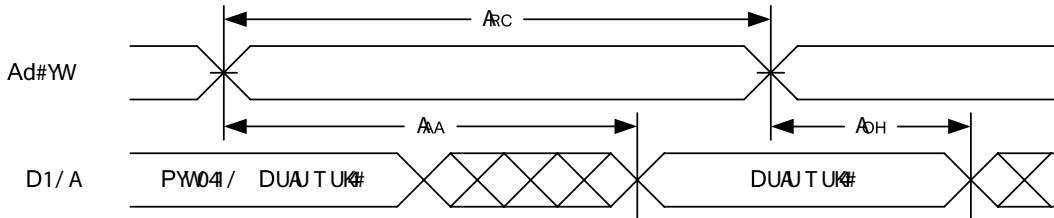
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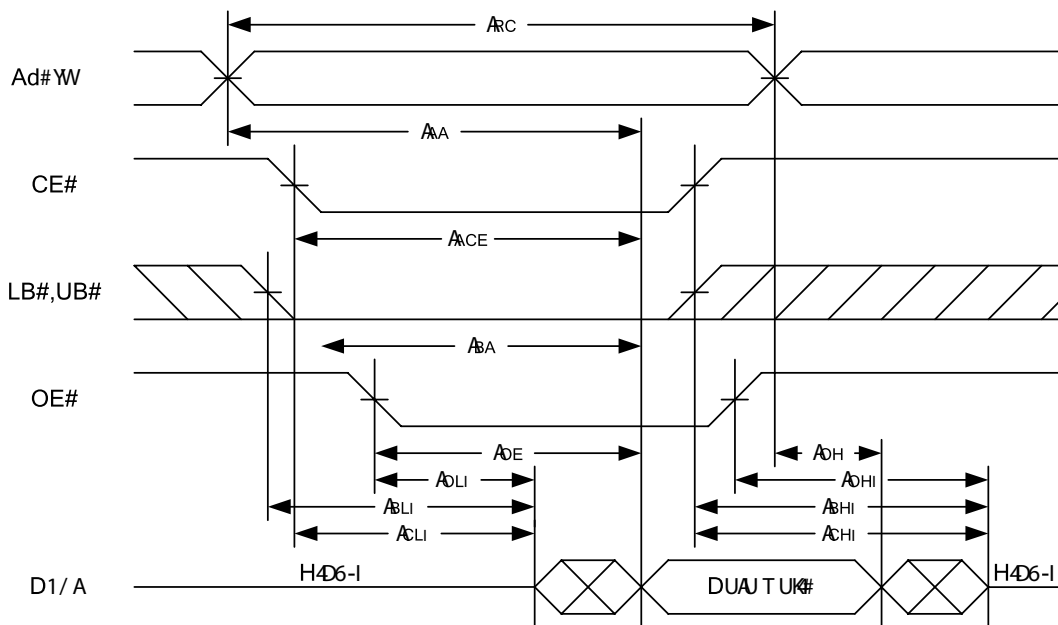
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**TIMING WAVEFORMS**

**READ CYCLE 1 (Address Controlled) (1,2)**



**READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)**



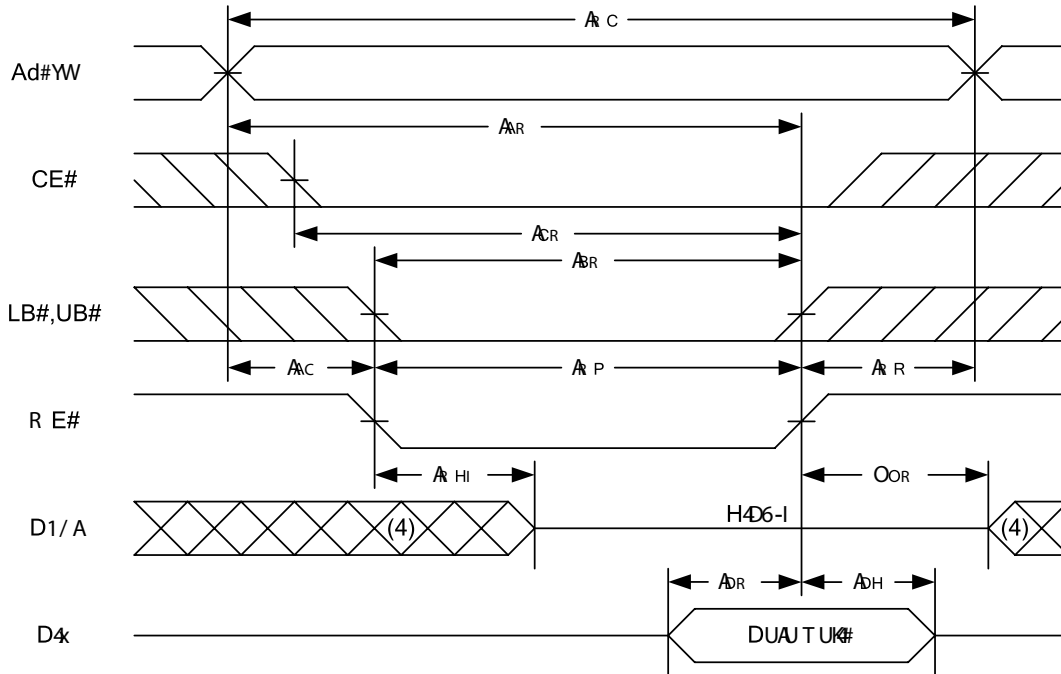
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, LB# or UB# = low transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $t_{CLZ}$ ,  $t_{BLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$ ,  $t_{BHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
5. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{BHZ}$  is less than  $t_{BLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .

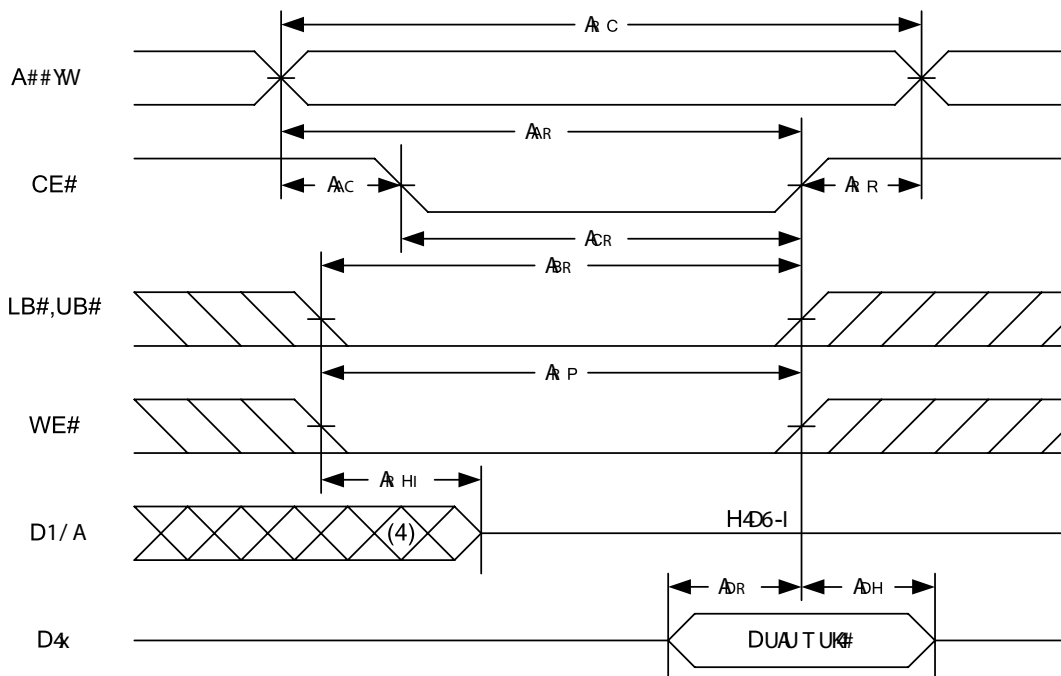


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**WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)**



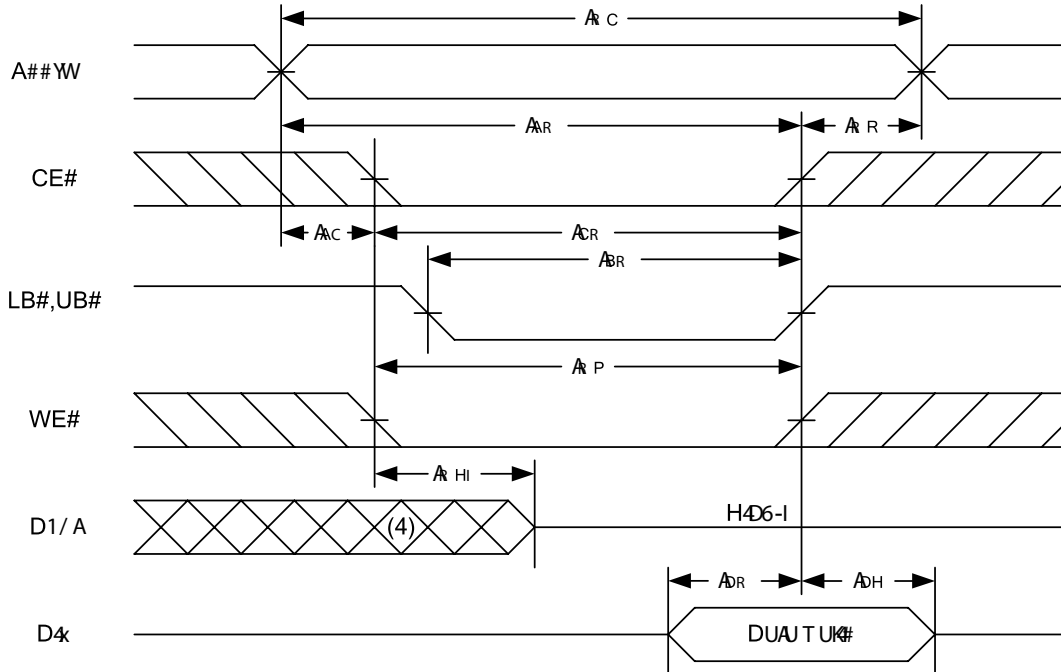
**WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)**





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**WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)**



Notes :

1. WE#, CE#, LB#, UB# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low,  $t_{WP}$  must be greater than  $t_{WHZ} + t_{DW}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6.  $t_{OW}$  and  $t_{WHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.

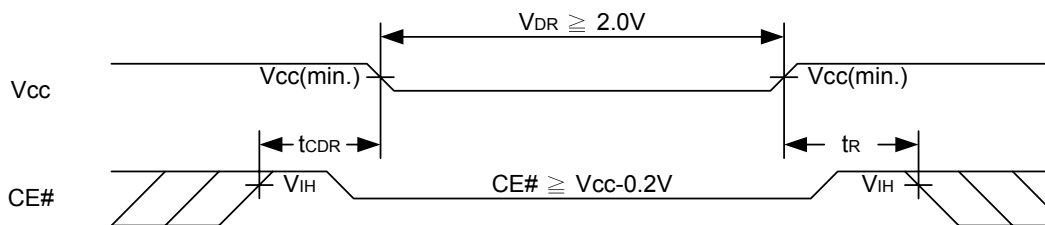
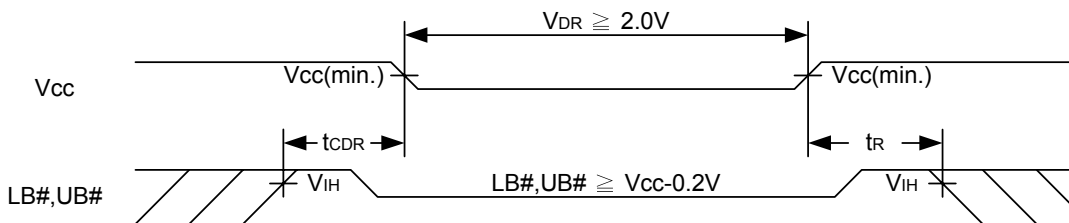




## 64K X 16 BIT LOW POWER CMOS SRAM

**DATA RETENTION CHARACTERISTICS**

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub> for Data Retention	V <sub>DR</sub>	CE# ≥ V <sub>CC</sub> - 0.2V	2.0	-	5.5	V
Data Retention Current	I <sub>DR</sub>	V <sub>CC</sub> = 2.0V CE# ≥ V <sub>CC</sub> - 0.2V Other pins at 0.2V or V <sub>CC</sub> -0.2V	-	0.5	20	μA
Chip Disable to Data Retention Time	t <sub>CDR</sub>	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t <sub>r</sub>		t <sub>RC</sub> *	-	-	ns

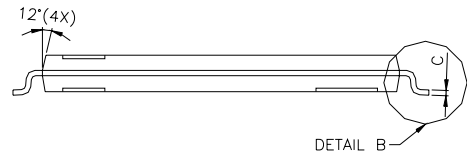
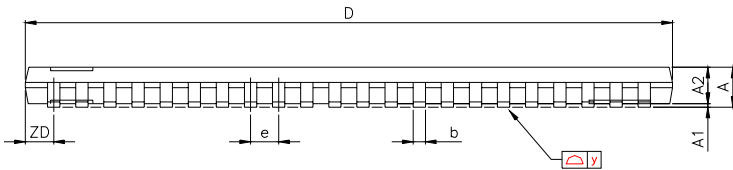
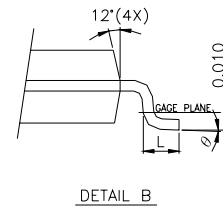
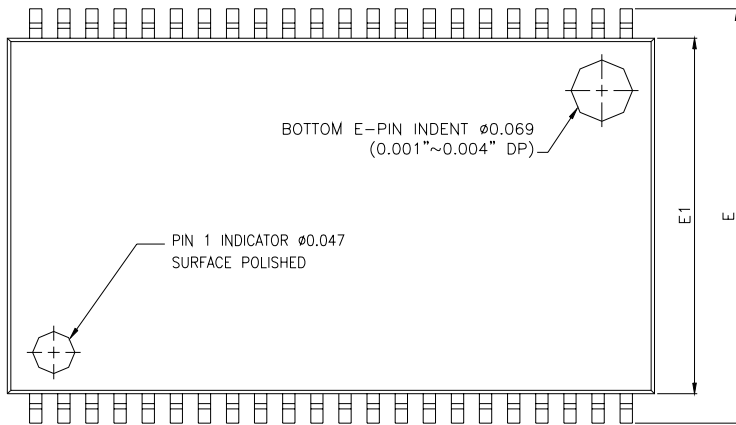
t<sub>RC</sub>\* = Read Cycle Time**DATA RETENTION WAVEFORM****Low V<sub>CC</sub> Data Retention Waveform (1)** (CE# controlled)**Low V<sub>CC</sub> Data Retention Waveform (2)** (LB#, UB# controlled)



64K X 16 BIT LOW POWER CMOS SRAM

**PACKAGE OUTLINE DIMENSION**

**44-pin 400mil TSOP-II Package Outline Dimension**

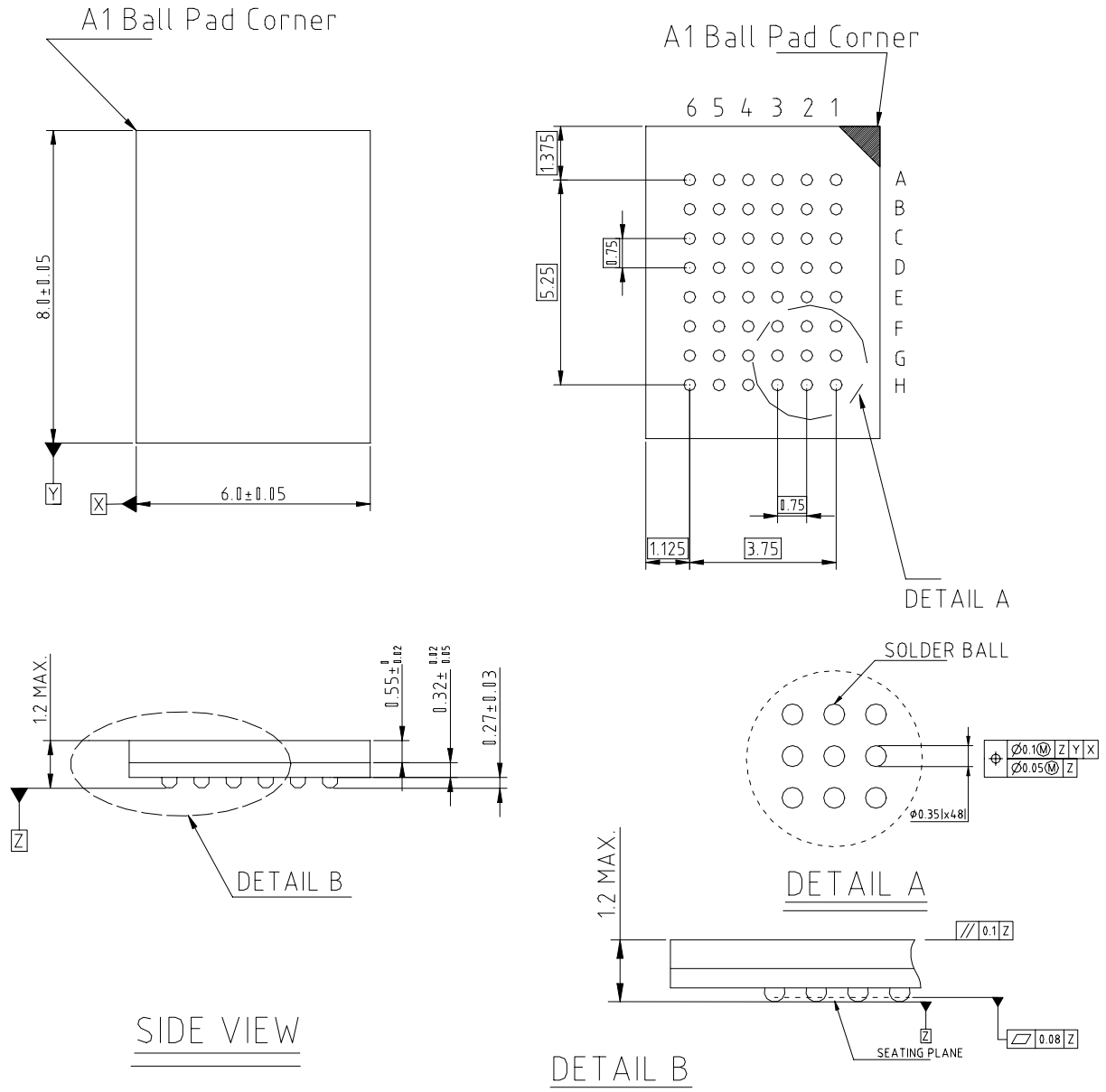


SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
$\theta$	$0^\circ$	$3^\circ$	$6^\circ$	$0^\circ$	$3^\circ$	$6^\circ$



64K X 16 BIT LOW POWER CMOS SRAM

48-ball 6mm x 8mm TFBGA Package Outline Dimension





## 64K X 16 BIT LOW POWER CMOS SRAM

**ORDERING INFORMATION**

Alliance	Organization	VCC Range	Package	Operating Temp	Speed ns
AS6C1016-55ZIN	64K x 16	2.7 - 5.5V	44pin TSOP II	Industrial ~ -40 F - 85 F	55
AS6C1016-55BIN	64K x 16	2.7 - 5.5V	48ball TFBGA	Industrial ~ -40 F - 85 F	55

**PART NUMBERING SYSTEM**

AS6C	1016	-55	X	X	N
low power SRAM prefix	Device Number 10 = 1M 16 =x16	Access Time	Package Option 44pin TSOP II 48ball TFBGA	Temperature Range I = Industrial (-40 to + 85 C)	N = Lead Free RoHS compliant part



## 64K X 16 BIT LOW POWER CMOS SRAM



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