



8-Mbit (1024K x 8) MoBL[®] Static RAM

Features

- **Very high speed: 45 ns, 55 ns and 70 ns**
 - **Wide voltage range: 2.20V – 3.60V**
- **Ultra-low active power**
 - **Typical active current: 1.5 mA @ f = 1 MHz**
 - **Typical active current: 12 mA @ f = f_{max}**
- **Ultra-low standby power**
- **Easy memory expansion with \overline{CE}_1 , \overline{CE}_2 , and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball BGA, 48-pin TSOP1, and 44-pin TSOP1I**

Functional Description^[1]

The CY62158DV30 is a high-performance CMOS static RAMs organized as 1024K words by 8 bits. This device features advanced circuit design to provide ultra-low active current.

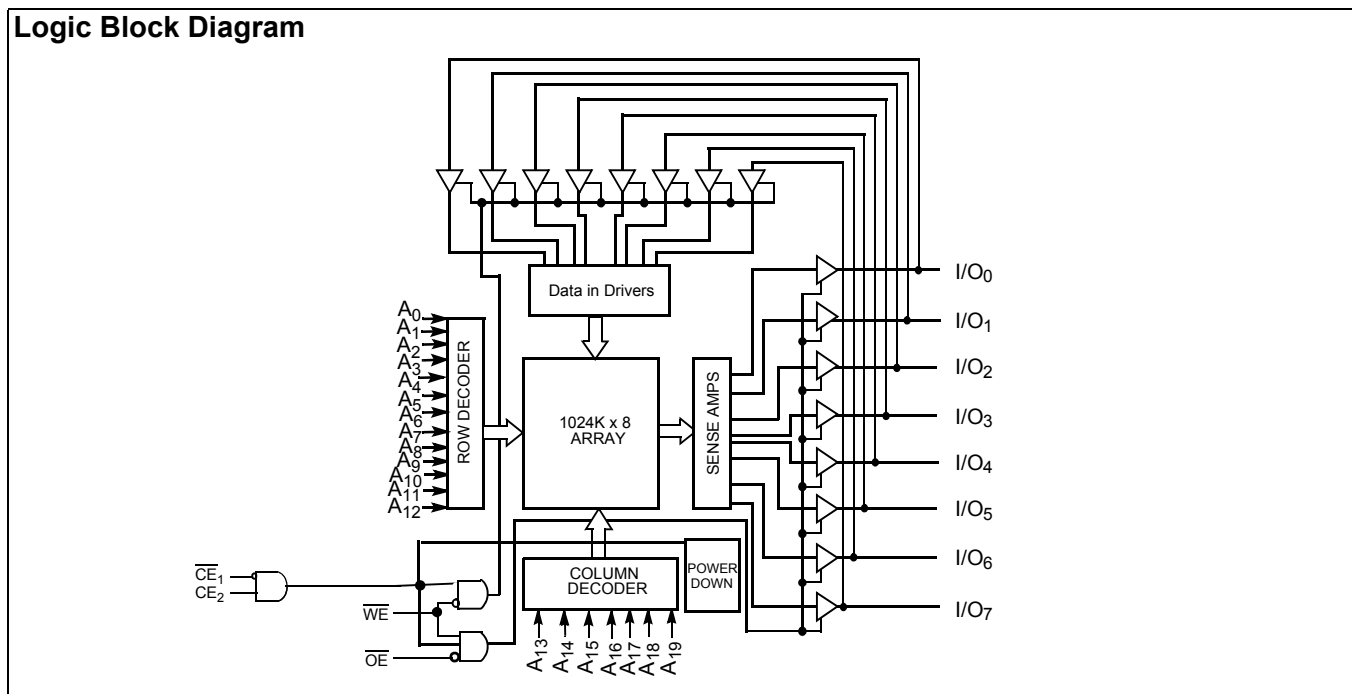
This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption by 85% when deselected (\overline{CE}_1 HIGH or \overline{CE}_2 LOW).

Writing to the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and Chip Enable 2 (\overline{CE}_2) HIGH. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₉).

Reading from the device is accomplished by taking Chip Enable 1 (\overline{CE}_1) and Output Enable (\overline{OE}) LOW and Chip Enable 2 (\overline{CE}_2) HIGH while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

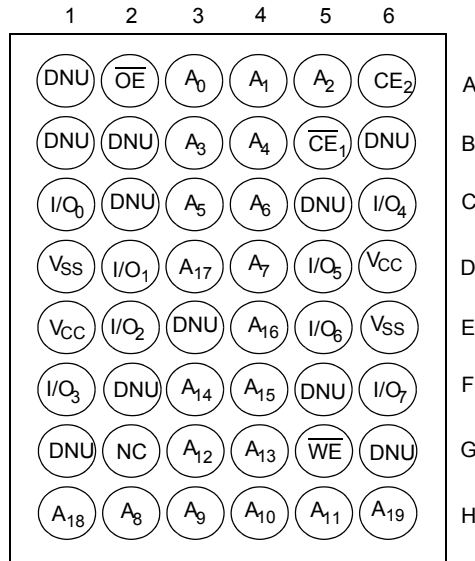
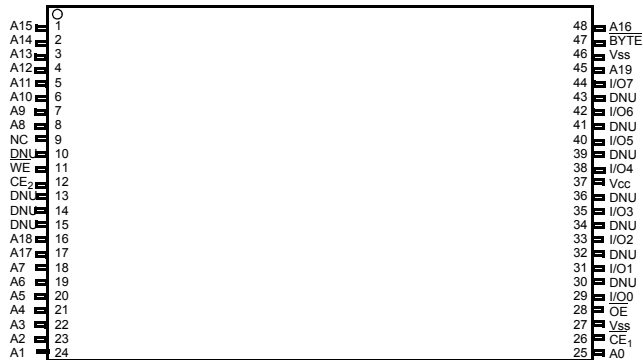
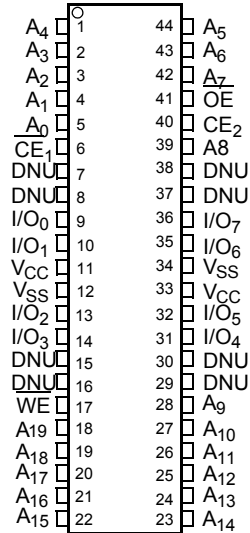
The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 LOW and \overline{CE}_2 HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW and \overline{CE}_2 HIGH and \overline{WE} LOW). See the truth table for a complete description of read and write modes.

Logic Block Diagram



Note:

1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, available at <http://www.cypress.com>.

Pin Configuration^[2, 3, 4]
FBGA
Top View

48TSOPI⁺
Top View

44 TSOPII
Top View

Notes:

- NC pins are not internally connected to the die.
- DNU pins have to be left floating.
- The BYTE pin in the TSOPI package has to be tied LOW to use the device as 1M x 8 SRAM. The 48-TSOPI package can also be used as a 512K x 16 SRAM by tying the BYTE signal HIGH. For 512K x 16 functionality, please refer to the CY62157DV30 data sheet.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	55°C to +125°C
Supply Voltage to Ground Potential .-	0.3V to $V_{CC(max)}$ + 0.3V
DC Voltage Applied to Outputs in High-Z State ^[5, 6]	-0.3V to $V_{CC(max)}$ + 0.3V
DC Input Voltage ^[5, 6]	-0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)
Latch-up Current.....	>200 mA

Operating Range

Product	Range	Ambient Temperature (T _A)	V _{CC} ^[7]
CY62158DV30L	Industrial	-40°C to +85°C	2.2V – 3.6V
CY62158DV30LL			

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μ A)	
	f = 1 MHz		f = f _{max}		Typ. ^[8]	Max.				
	Min.	Typ. ^[8]	Max.				Typ. ^[8]	Max.	Typ. ^[8]	Max.
CY62158DV30L	2.2	3.0	3.6	45,55,70	1.5	3	12	20	2	20
CY62158DV30LL	2.2	3.0	3.6	45,55,70	1.5	3	12	15	2	8

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62158DV30			Unit
				Min.	Typ. ^[8]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = 2.20V	2.0			V
		I _{OH} = -1.0 mA	V _{CC} = 2.70V	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = 2.20V			0.4	V
		I _{OL} = 2.1mA	V _{CC} = 2.70V			0.4	V
V _{IH}	Input HIGH Voltage	V _{CC} = 2.2V to 2.7V		1.8		V _{CC} + 0.3V	V
		V _{CC} = 2.7V to 3.6V		2.2		V _{CC} + 0.3V	V
V _{IIL}	Input LOW Voltage	V _{CC} = 2.2V to 2.7V		-0.3		0.6	V
		V _{CC} = 2.7V to 3.6V		-0.3		0.8	V
I _{IX}	Input Leakage Current	GND \leq V _I \leq V _{CC}		-1		+1	μ A
I _{OZ}	Output Leakage Current	GND \leq V _O \leq V _{CC} , Output Disabled		-1		+1	μ A
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}	V _{CC} = V _{CCmax} I _{OUT} = 0 mA CMOS levels	L	12	20	mA
				LL			
		f = 1 MHz		L	1.5	3	mA
				LL			
I _{SB1}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ \geq V _{CC} - 0.2V, CE ₂ \leq 0.2V V _{IN} \geq V _{CC} - 0.2V, V _{IN} \leq 0.2V f = f _{MAX} (Address and Data Only), f = 0 (OE, and WE), V _{CC} = 3.60V		L	2	20	μ A
				LL			
I _{SB2}	Automatic CE Power-down Current — CMOS Inputs	CE ₁ \geq V _{CC} - 0.2V or CE ₂ \leq 0.2V, V _{IN} \geq V _{CC} - 0.2V or V _{IN} \leq 0.2V, f = 0, V _{CC} = 3.60V		L	2	20	μ A
				LL			

Notes:

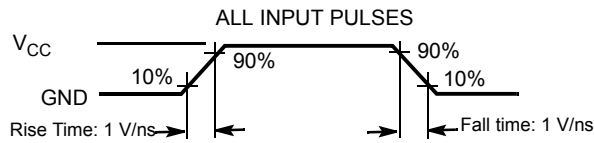
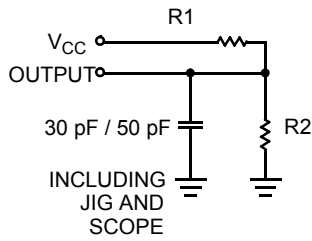
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- V_{IH(max.)} = V_{CC} + 0.75V for pulse duration less than 20ns.
- Full device AC operation assumes a 100 μ s ramp time from 0 to V_{cc(min)} and 200 μ s wait time after V_{cc} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Capacitance^[9, 10.]

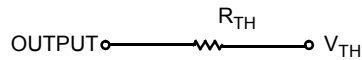
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)}	10	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	TSOP II	TSOP I	Unit
Θ _{JA}	Thermal Resistance ^[9] (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	72	75.13	74.88	°C/W
Θ _{JC}	Thermal Resistance ^[9] (Junction to Case)		8.86	8.95	8.6	°C/W

AC Test Loads and Waveforms^[11]


Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R _{TH}	8000	645	Ω
V _{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[8]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5			V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ₁ ≥ V _{CC} - 0.2V or CE ₂ ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	L		10	μA
			LL		4	μA
t _{CDR} ^[9]	Chip Deselect to Data Retention Time		0			ns
t _R ^[12]	Operation Recovery Time		t _{RC}			ns

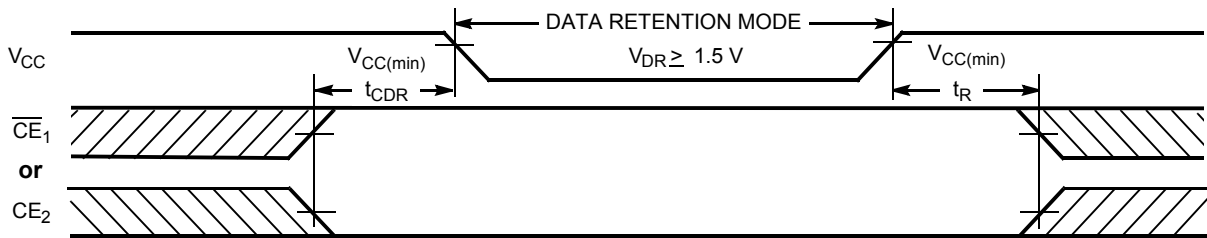
Notes:

9. Tested initially and after any design or process changes that may affect these parameters.

 10. The input capacitance on the CE₂ pin is 15 pF.

11. Test condition for the 45 ns part is a load capacitance of 30 pF.

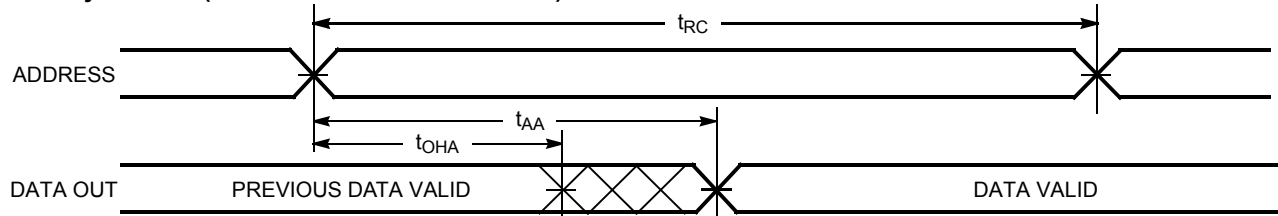
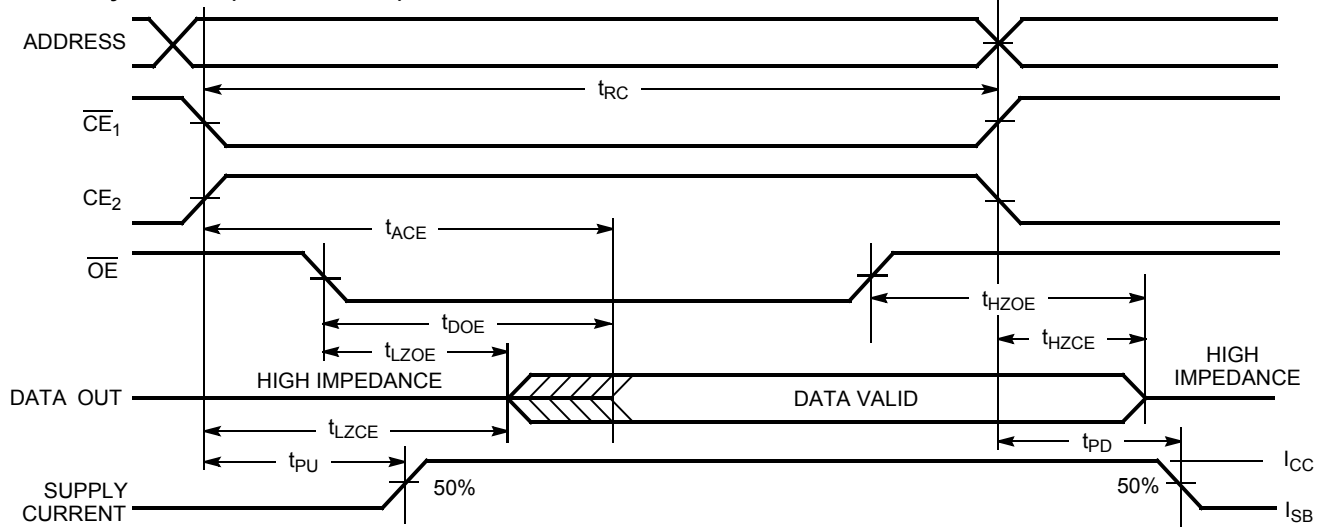
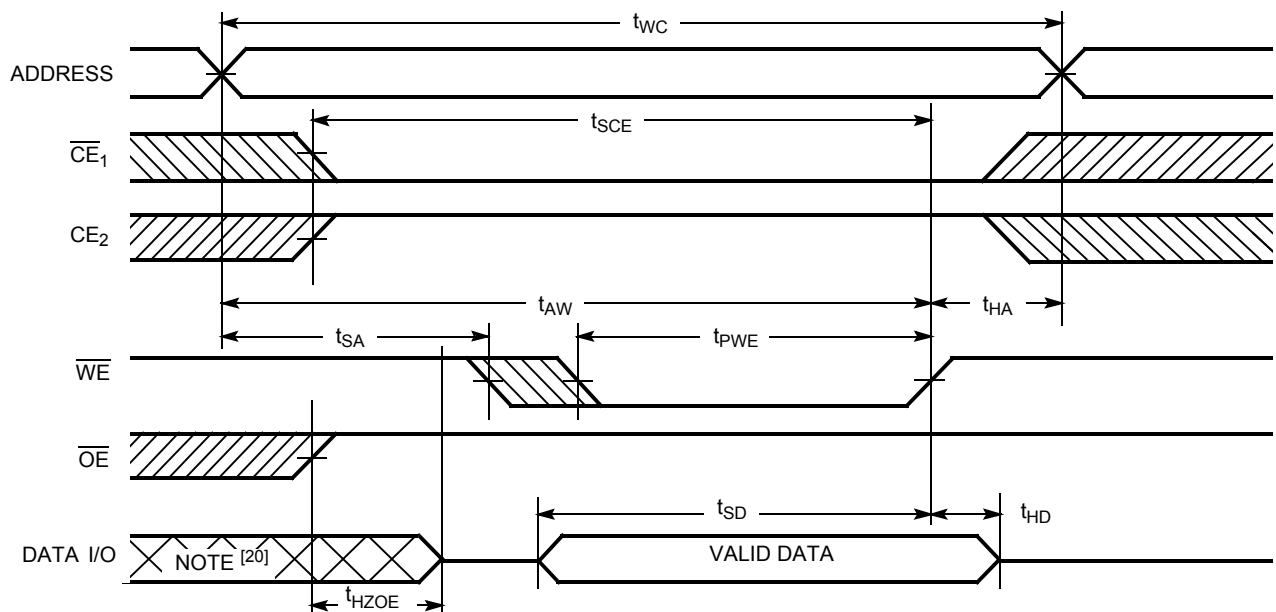
 12. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} ≥ 100 μs or stable at V_{CC(min.)} ≥ 100 μs.

Data Retention Waveform

Switching Characteristics Over the Operating Range ^[13]

Parameter	Description	45 ns ^[11]		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to Data Valid		45		55		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		25		25		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[14]	5		5		5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[14, 15]		15		20		25	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[14]	10		10		10		ns
t_{HZCE}	\overline{CE}_1 HIGH or CE_2 LOW to High Z ^[14, 15]		20		20		25	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to Power-Up	0		0		10		ns
t_{PD}	\overline{CE}_1 HIGH or CE_2 LOW to Power-Down		45		55		25	ns
Write Cycle^[16]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to Write End	40		40		60		ns
t_{AW}	Address Set-Up to Write End	40		40		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	35		40		45		ns
t_{SD}	Data Set-Up to Write End	25		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[14, 15]		15		20		25	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[14]	10		10		10		ns

Notes:

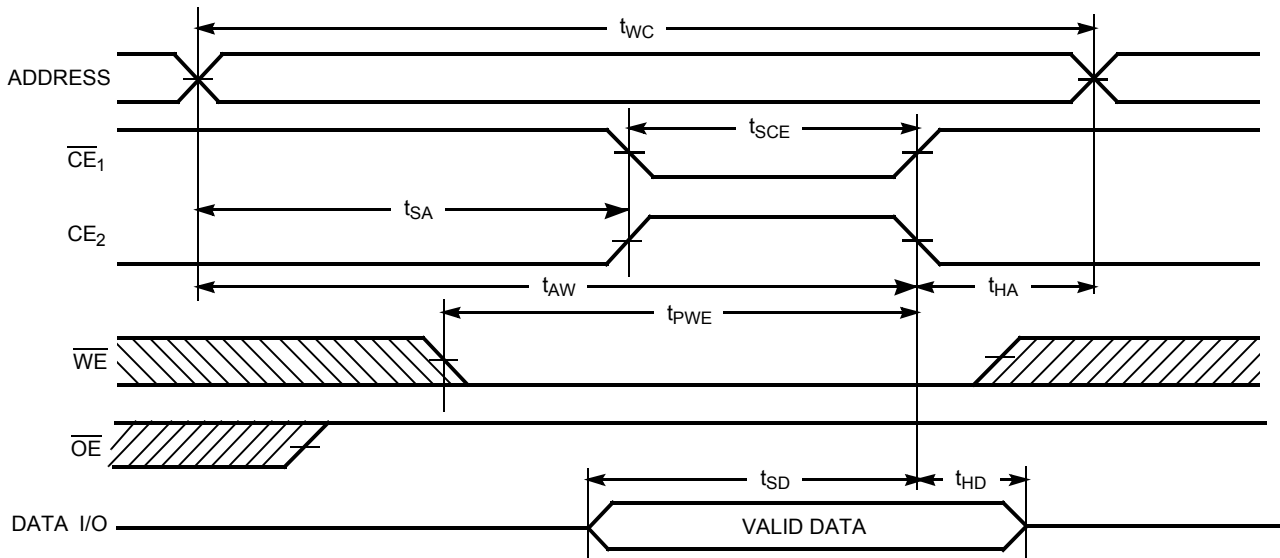
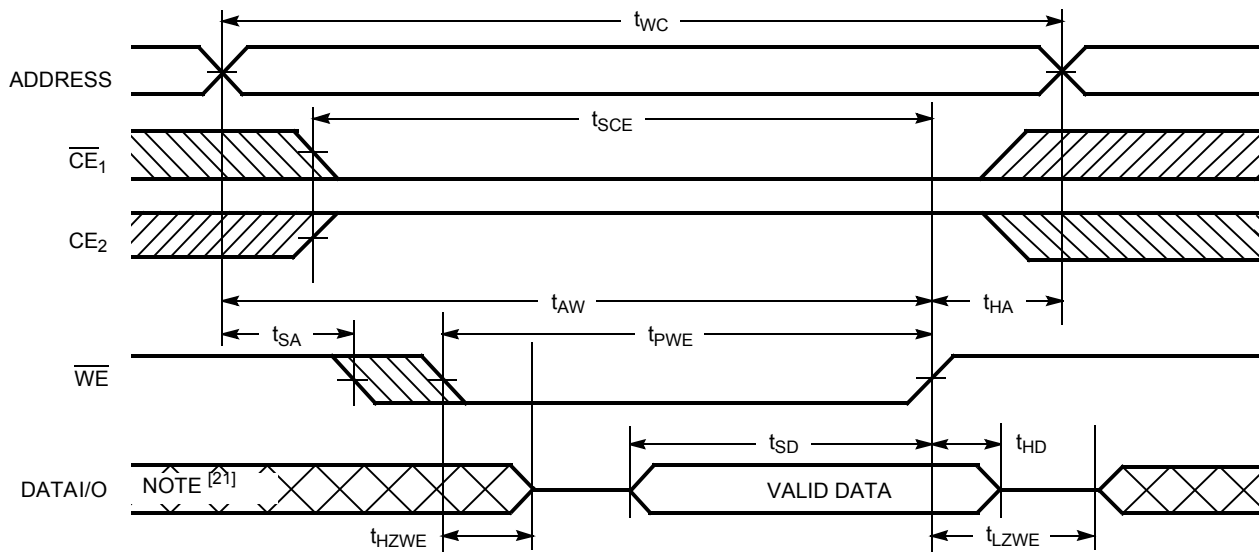
13. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3ns or less (1V/ns), timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
14. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
15. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled) [17, 18]

Read Cycle No. 2 (\overline{OE} Controlled) [18, 19]

Write Cycle No. 1 (\overline{WE} Controlled) [16, 20, 22]

Notes:

17. Device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.

18. \overline{WE} is HIGH for read cycle.

19. Address valid prior to or coincident with \overline{CE}_1 transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 2 (CE₁ or CE₂ Controlled) ^[16, 20, 22]

Write Cycle No. 3 (WE Controlled, OE LOW) ^[22]

Truth Table

CE ₁	CE ₂	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I _{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I _{SB})
L	H	H	L	Data Out (I/O ₀ -I/O ₇)	Read	Active (I _{CC})
L	H	H	H	High Z	Output Disabled	Active (I _{CC})
L	H	L	X	Data in (I/O ₀ -I/O ₇)	Write	Active (I _{CC})

Notes:

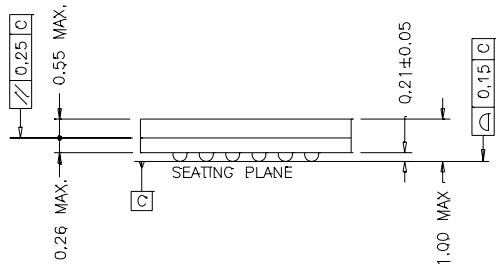
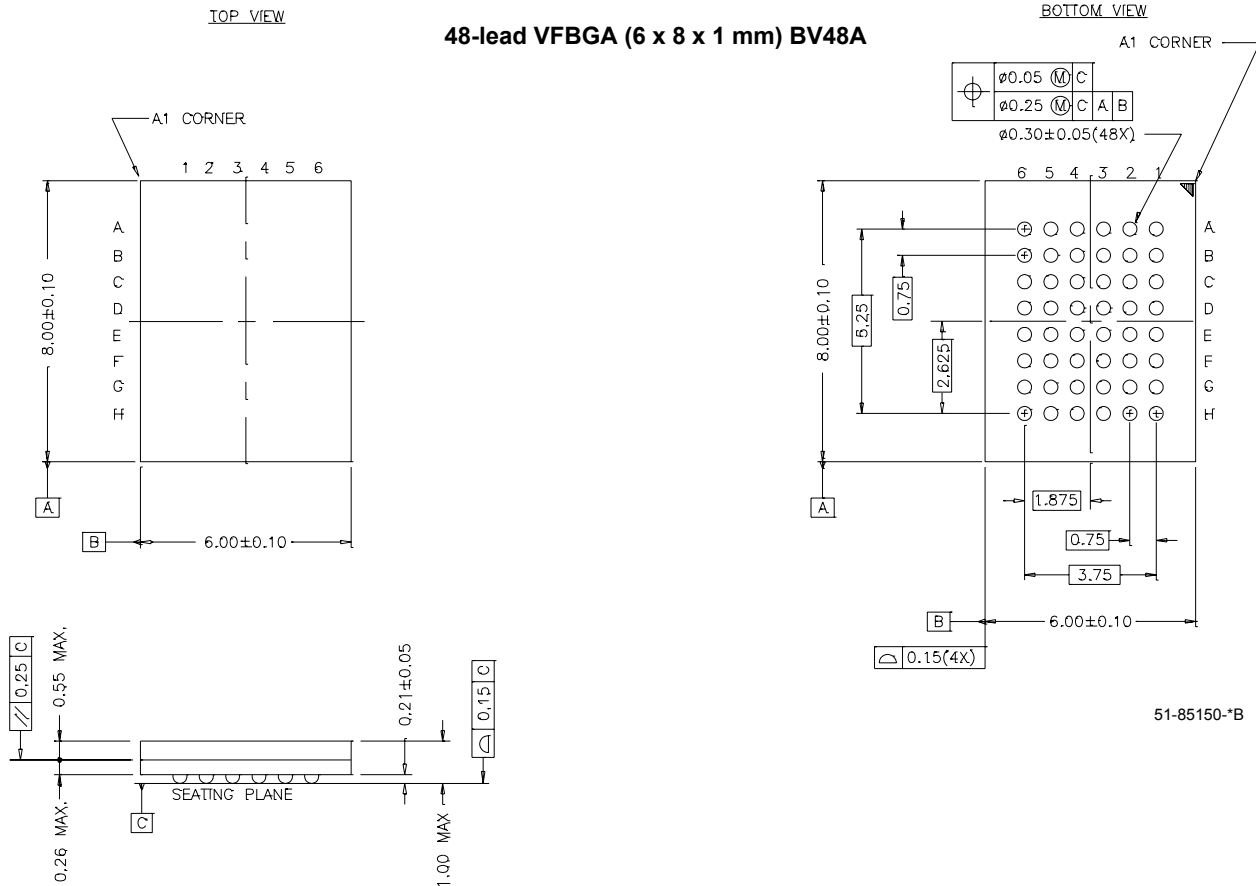
20. Data I/O is high impedance if OE = V_{IH}.

21. During this period, the I/Os are in output state and input signals should not be applied.

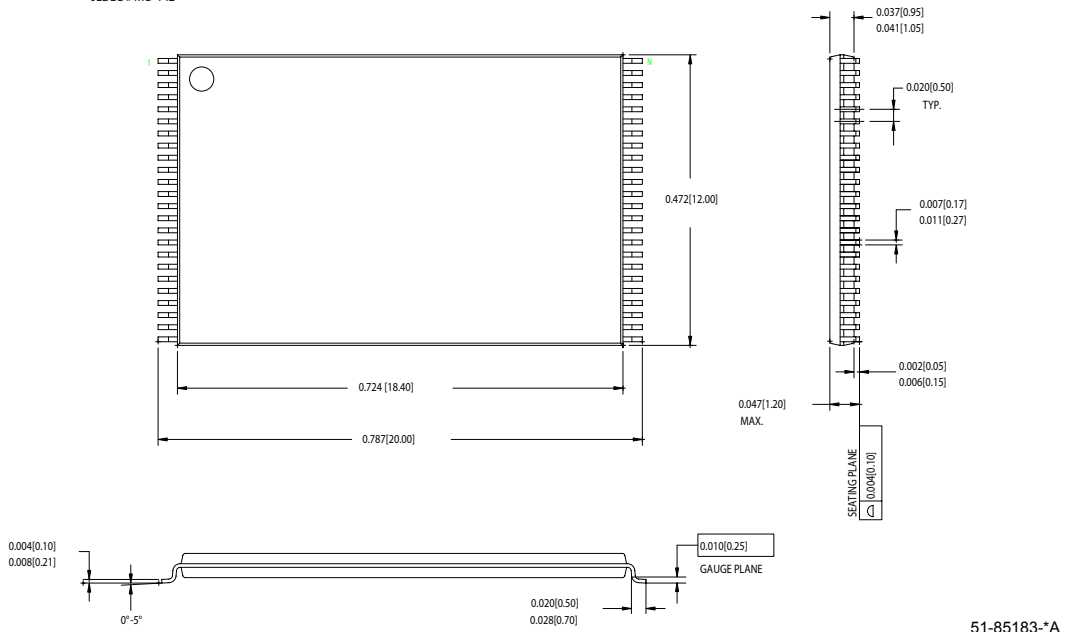
22. If CE₁ goes HIGH or CE₂ goes LOW simultaneously with WE HIGH, the output remains in high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
45	CY62158DV30L-45BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62158DV30LL-45BVI			
45	CY62158DV30L-45ZXI	Z-48	48 Pin TSOP I (Pb-free)	Industrial
	CY62158DV30LL-45ZXI			
45	CY62158DV30L-45ZSXI	ZS-44	44 Pin TSOP II (Pb-free)	Industrial
	CY62158DV30LL-45ZSXI			
55	CY62158DV30L-55BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62158DV30LL-55BVI			
55	CY62158DV30L-55ZXI	Z-48	48 Pin TSOP I (Pb-free)	Industrial
	CY62158DV30LL-55ZXI			
55	CY62158DV30L-55ZSXI	ZS-44	44 Pin TSOP II (Pb-free)	Industrial
	CY62158DV30LL-55ZSXI			
70	CY62158DV30L-70BVI	BV48A	48-ball Fine Pitch BGA (6 mm × 8mm × 1 mm)	Industrial
	CY62158DV30LL-70BVI			
70	CY62158DV30L-70ZXI	Z-48	48 Pin TSOP I (Pb-free)	Industrial
	CY62158DV30LL-70ZXI			
70	CY62158DV30L-70ZSXI	ZS-44	44 Pin TSOP II (Pb-free)	Industrial
	CY62158DV30LL-70ZSXI			

Package Diagrams

48-Lead TSOP I (12 mm x 18.4 mm x 1.0 mm) Z48A

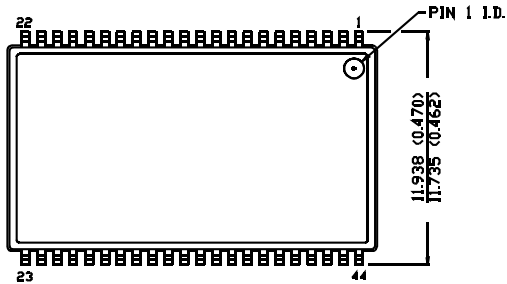
DIMENSIONS IN INCHES[MM] MIN. MAX.
 JEDEC # MO-142



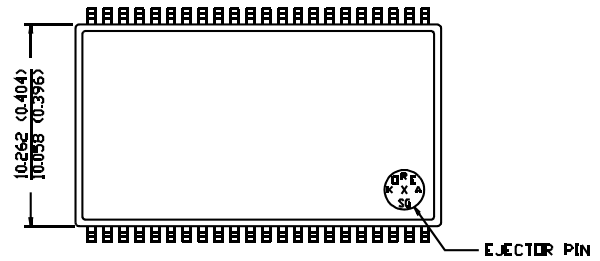
Package Diagrams (continued)

44-pin TSOP II ZS44

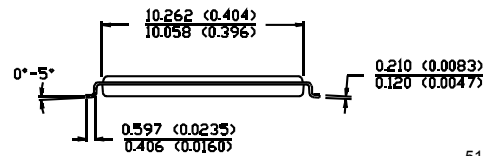
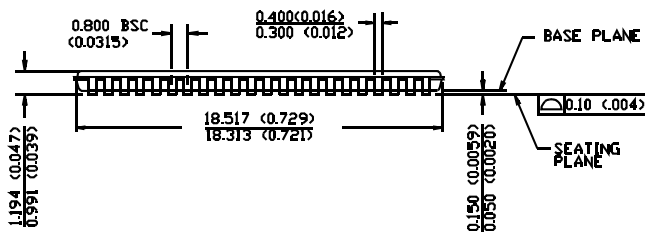
DIMENSION IN MM (INCH)
MAX
MIN



TOP VIEW



BOTTOM VIEW



51-85087-A

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Document History Page

Document Title: CY62158DV30 MoBL [®] 8-Mbit (1024K x 8) MoBL [®] Static RAM				
Document Number: 38-05391				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	126293	05/22/03	HRT	New Data Sheet
*A	131014	11/25/03	CBD	Change from Advance to Preliminary
*B	133114	01/24/04	CBD	Minor Change: MPN change and upload
*C	211602	See ECN	AJU	Change from Preliminary to Final Changed Marketing part # from CY62158DV to CY62158DV30 in the "Title" and in the "Ordering Information" table Added footnote 4 and 10 Modified footnote 7 to include ramp time and wait time Removed MAX value for V _{DR} on "Data Retention Characteristics" table Changed ordering code for Pb-free parts Modified voltage limits in Maximum Ratings section
*D	239450	See ECN	SYT/AJU	Added footnote #11 Added 45 ns and 70 ns Speed Bins