



32K × 8 CMOS STATIC RAM

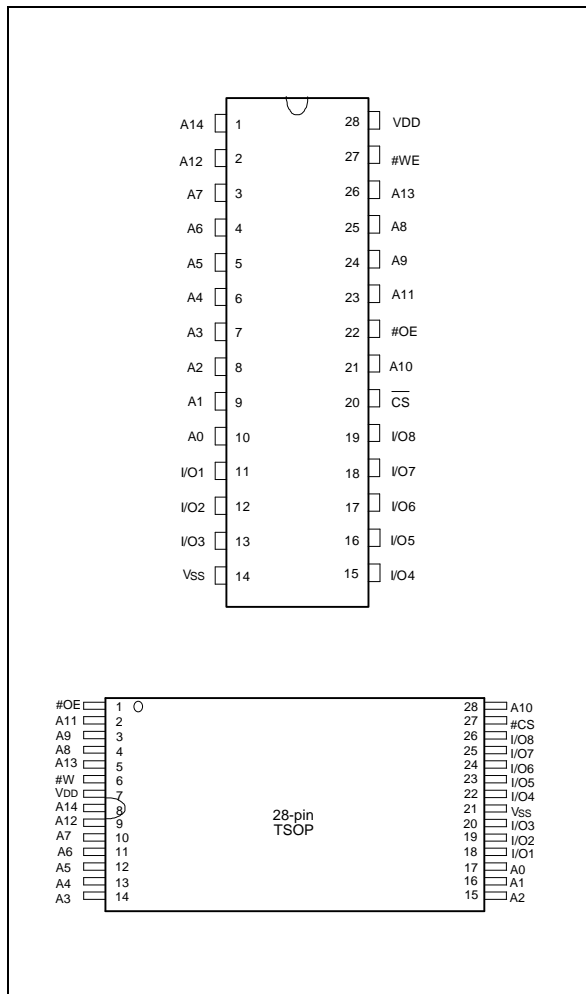
GENERAL DESCRIPTION

The W24L257 is a normal-speed, very low-power CMOS static RAM organized as 32768 × 8 bits that operates on a wide voltage range from 3V to 5.5V power supply. This device is manufactured using Winbond's high performance CMOS technology.

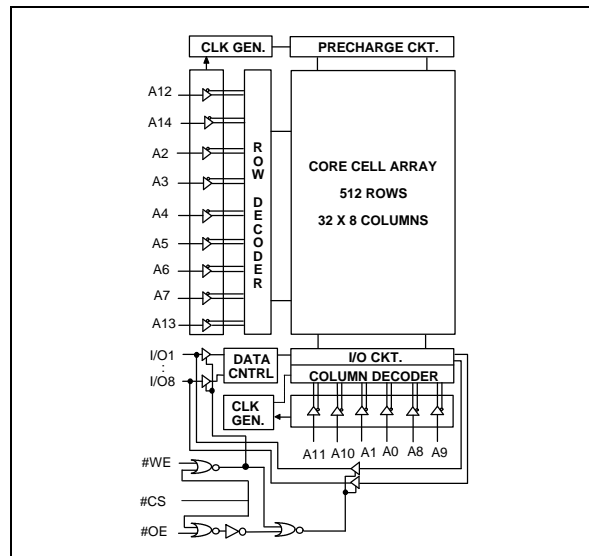
FEATURES

- Low power consumption:
- Access time: 70 nS
- 3.3V/5V power supply
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Battery back-up operation capability
- Data retention voltage: 2V (min.)
- Packaged in 330 mil SOP, and standard type one STSOP (8 mm × 13.4 mm)

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 – A14	Address Inputs
I/O1 – I/O8	Data Inputs/Outputs
#CS	Chip Select Input
#WE	Write Enable Input
#OE	Output Enable Input
VDD	Power Supply
VSS	Ground
NC	No Connection

TRUTH TABLE

#CS	#OE	#WE	MODE	I/O1 - I/O8	V _{DD} CURRENT
H	X	X	Not Selected	High Z	ISB, ISB1
L	H	H	Output Disable	High Z	I _{DD}
L	L	H	Read	Data Out	I _{DD}
L	X	L	Write	Data In	I _{DD}

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER		RATING		UNIT
		3.3V	5V	
Supply Voltage to V _{SS} Potential		-0.5 to +4.6	-0.5 to +7.0	V
Input/Output to V _{SS} Potential		-0.5 to V _{DD} +0.5		V
Allowable Power Dissipation		1.0		W
Storage Temperature		-65 to +150		°C
Operating Temperature	L/LL	0 to 70		°C
	LE	-20 to 85		
	LI	-40 to 85		

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5V ±10%; V_{DD} = 3.3V ±5%; V_{SS} = 0V; T_A (°C) = 0 to 70 for L/LL, -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	3.3V		5V		UNIT
			MIN.	MAX.	MIN.	MAX.	
Input Low Voltage	V _{IL}	-	-0.5	+0.6	-0.5	+0.8	V
Input High Voltage	V _{IH}	-	+2.0	V _{DD} +0.5	+2.2	V _{DD} +0.5	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-1	+1	-2	+2	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} , #CS = V _{IH} (Min.) or #OE = V _{IH} (Min.) or #CS = V _{IL} (Max.)	-1	+1	-2	+2	μA
Output Low Voltage	V _{OL}	I _{OL} = +2.1 mA	-	0.4	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -1.0 mA	2.2	-	2.4	-	V
Operating Power Supply Current	I _{DD}	#CS = V _{IL} (Max.) and I/O = 0 mA, Cycle = Min. Duty = 100%	-	35	-	70	mA



Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	3.3V		5V		UNIT	
			MIN.	MAX.	MIN.	MAX.		
Standby Power Supply Current	ISB	#CS = V _{IH} (min.) or Cycle = min. Duty = 100%	-	1	-	3	mA	
	ISB1	#CS ≥ V _{DD} - 0.2V	LL/LE/LI	-	15	-	15	μA
		L		-	30	-	30	

Note: Typical parameter is measured under ambient temperature T_A = 25° C and V_{DD} = 3.3V/5V

CAPACITANCE

(V_{DD} = 5V ±10%; V_{DD} = 3V ±5%, T_A = 25° C, f = 1 MHz)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C _{IN}	V _{IN} = 0V	6	pF
Input/Output Capacitance	C _{I/O}	V _{OUT} = 0V	8	pF

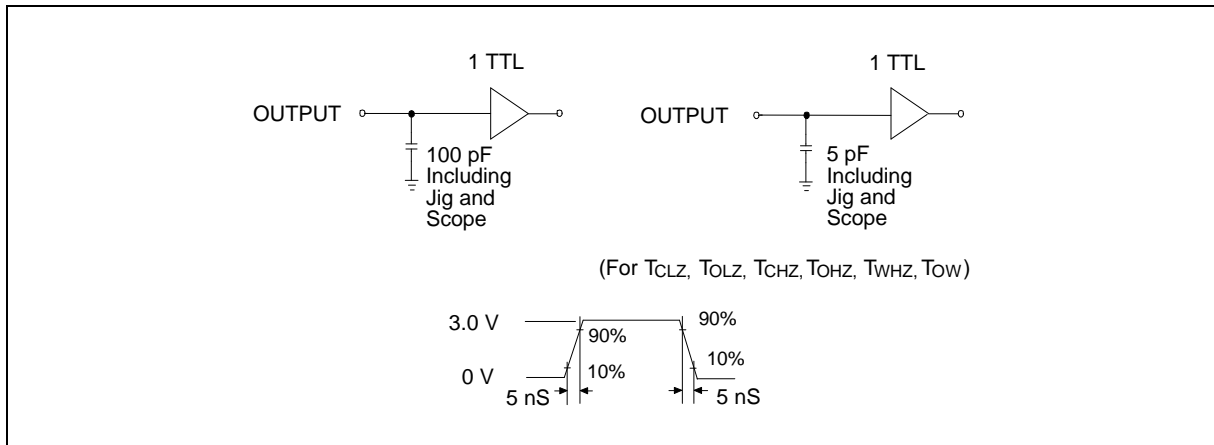
Note: These parameters are sampled but not 100% tested.

AC Characteristics

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5 nS
Input and Output Timing Reference Level	1.5V
Output Load	See the drawing below

AC Test Loads and Waveform





AC Characteristics, continued

Read Cycle(V_{DD} = 5V ±10%; V_{DD} = 3V ±5%; V_{SS} = 0V; T_A (°C) = 0 to 70 for L/LL, -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYMBOL	3.3V/5V		UNIT
		MIN.	MAX.	
Read Cycle Time	TRC	70	-	nS
Address Access Time	TAA	-	70	nS
Chip Select Access Time	TACS	-	70	nS
Output Enable to Output Valid	TAOE	-	35	nS
Chip Selection to Output in Low Z	TCLZ*	10	-	nS
Output Enable to Output in Low Z	TOLZ*	5	-	nS
Chip Deselection to Output in High Z	TCHZ*	-	30	nS
Output Disable to Output in High Z	TOHZ*	-	30	nS
Output Hold from Address Change	TOH	10	-	nS

* These parameters are sampled but not 100% tested

Write Cycle

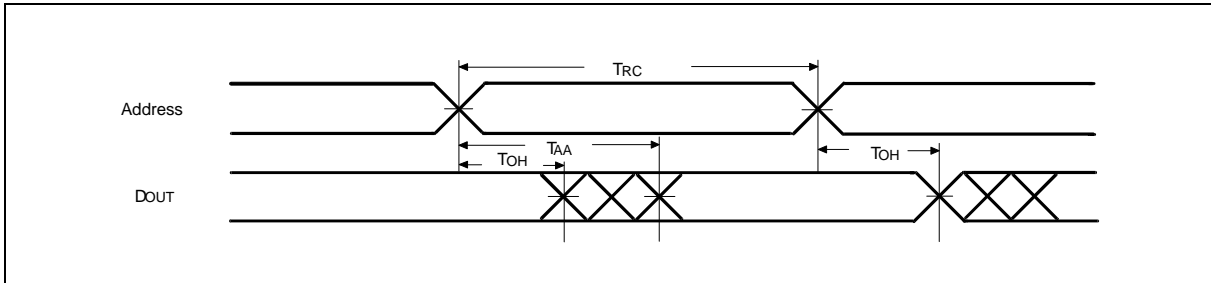
PARAMETER	SYMBOL	3.3V/5V		UNIT	
		MIN.	MAX.		
Write Cycle Time	TWC	70	-	nS	
Chip Selection to End of Write	TCW	55	-	nS	
Address Valid to End of Write	TAW	55	-	nS	
Address Setup Time	TAS	0	-	nS	
Write Pulse Width	TWP	40	-	nS	
Write Recovery Time	#CS, #WE	TWR	0	-	nS
Data Valid to End of Write	TDW	35	-	nS	
Data Hold from End of Write	TDH	0	-	nS	
Write to Output in High Z	TWHZ*	-	25	nS	
Output Disable to Output in High Z	TOHZ*	-	25	nS	
Output Active from End of Write	TOW	5	-	nS	

* These parameters are sampled but not 100% tested

TIMING WAVEFORMS

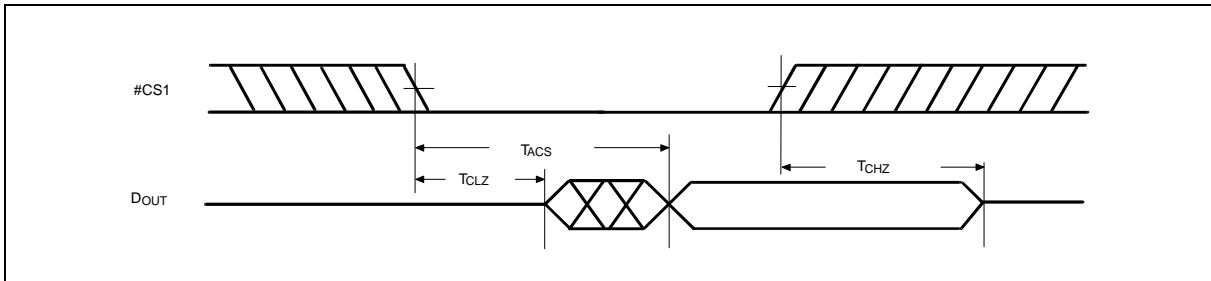
Read Cycle 1

(Address Controlled)



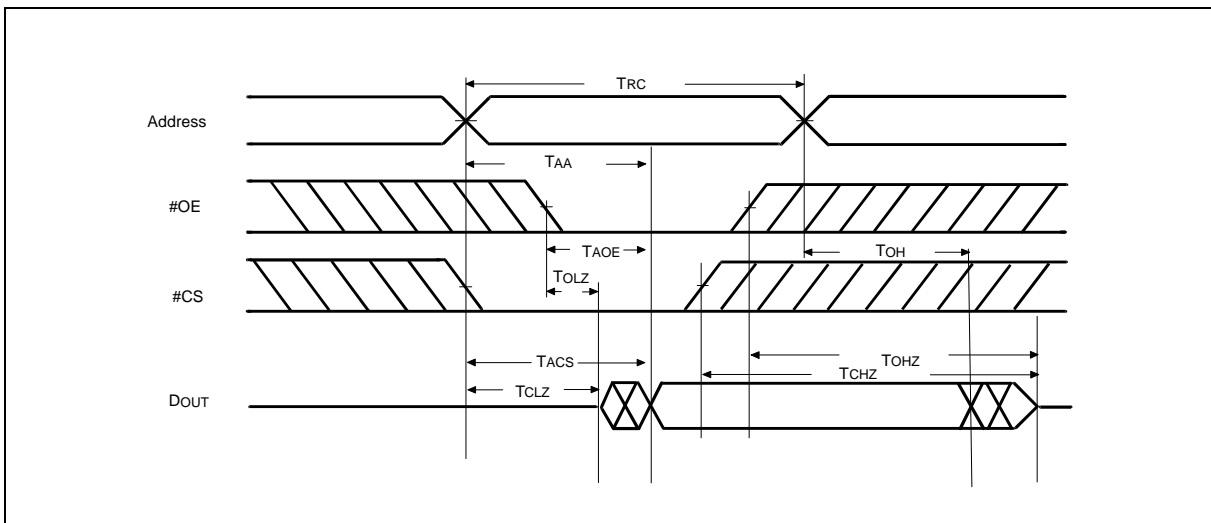
Read Cycle 2

(Chip Select Controlled)



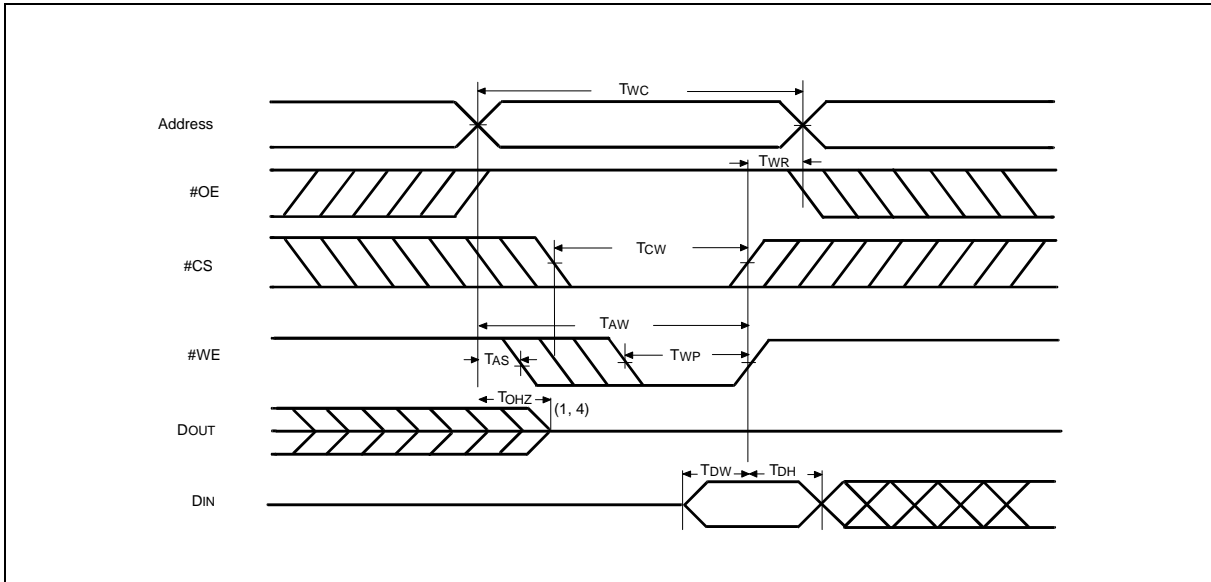
Read Cycle 3

(Output Enable Controlled)



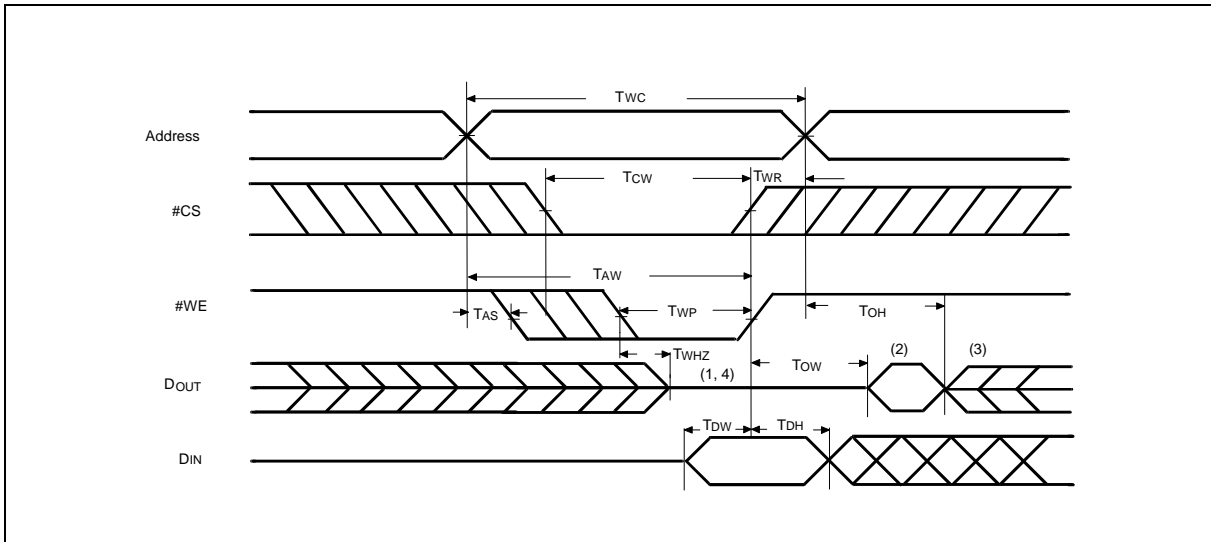
Timing Waveforms, continued

Write Cycle 1



Write Cycle 2

(#OE = VIL Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

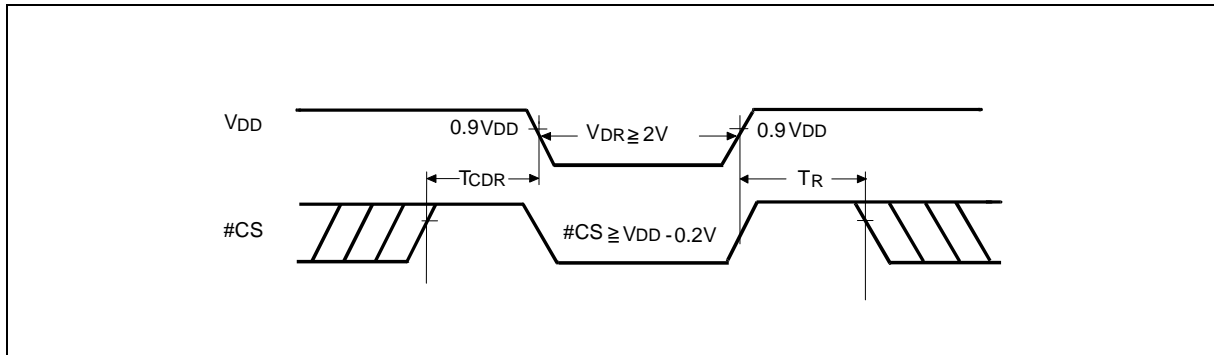
DATA RETENTION CHARACTERISTICS

(TA (°C) = 0 to 70 for L/LL, -20 to 85 for LE, -40 to 85 for LI)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
VDD for Data Retention	VDR	#CS ≥ VDD - 0.2V	2.0	-	-	V
Data Retention Current	IDDDR	#CS ≥ VDD - 0.2V, LL/LE/LI	-	-	15	μA
		VDD = 3V L	-	-	30	μA
Chip Deselect to Data Retention Time	TCDR	See data retention waveform	0	-	-	nS
Operation Recovery Time	TR		TRC*	-	-	nS

* Read Cycle Time

DATA RETENTION WAVEFORM





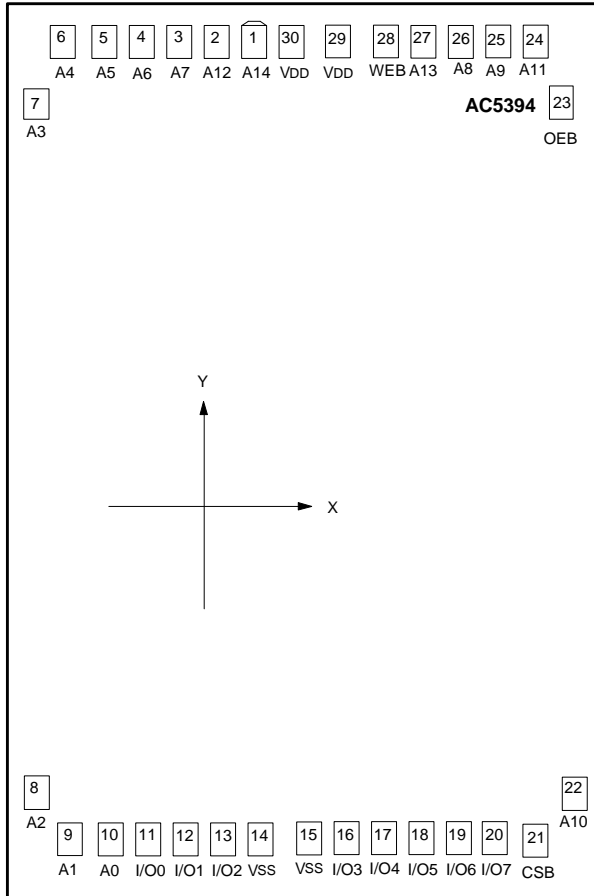
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING VOLTAGE (V)	OPERATING TEMPERATURE (°C)	STANDBY CURRENT MAX. (mA)	PACKAGE
W24L257S70L	70	3.3V/5V	0 to 70	30	330 mil SOP
W24L257S70LL	70	3.3V/5V	0 to 70	15	330 mil SOP
W24L257S70LE	70	3.3V/5V	-20 to 85	15	330 mil SOP
W24L257S70LI	70	3.3V/5V	-40 to 85	15	330 mil SOP
W24L257Q70L	70	3.3V/5V	0 to 70	30	Small TSOP
W24L257Q70LL	70	3.3V/5V	0 to 70	15	Small TSOP
W24L257Q70LE	70	3.3V/5V	-20 to 85	15	Small TSOP
W24L257Q70LI	70	3.3V/5V	-40 to 85	15	Small TSOP

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

BONDING PAD DIAGRAM

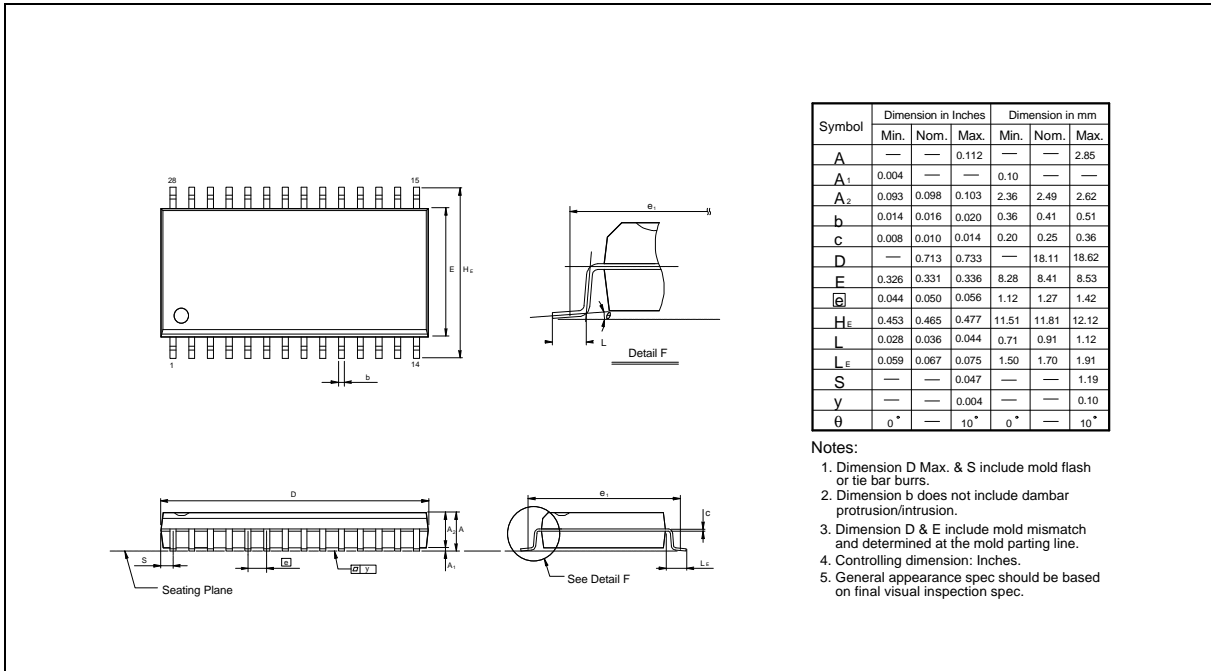


PAD NO.	X	Y
1	-232.25	1445.22
2	-351.70	1445.22
3	-471.15	1445.22
4	-590.60	1445.22
5	-710.05	1445.22
6	-829.50	1445.22
7	-992.79	1362.24
8	-992.79	-1306.11
9	-857.86	-1452.79
10	-738.41	-1452.79
11	-594.84	-1414.13
12	-451.06	-1414.13
13	-310.67	-1414.13
14	-171.78	-1405.28
15	24.45	-1405.28
16	151.80	-1414.13
17	298.07	-1414.13
18	443.28	-1414.13
19	588.20	-1414.13
20	732.84	-1414.13
21	871.11	-1452.79
22	992.75	-1312.15
23	992.75	1373.67
24	810.09	1445.22
25	690.64	1445.22
26	571.19	1445.22
27	451.74	1445.22
28	332.29	1445.22
29	120.25	1444.65
30	-93.23	1444.65

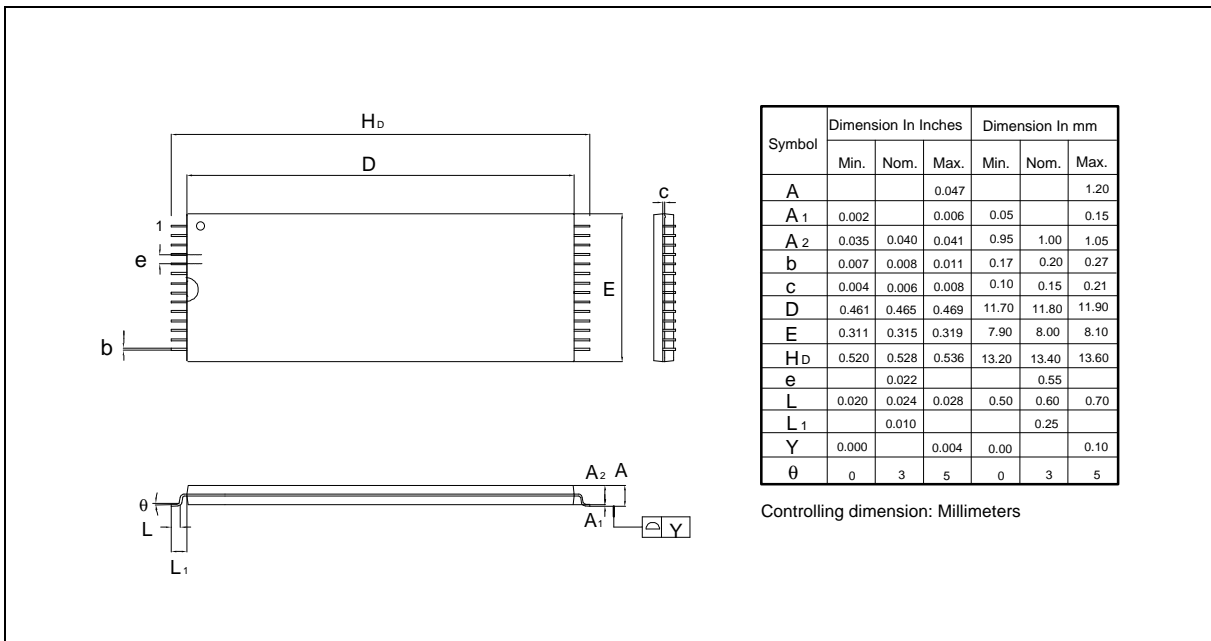
Note: For bare chip form (C.O.B.) applications, the substrate must be connected to VDD or left floating in the PCB layout.

PACKAGE DIMENSIONS

28-pin SOP



28-pin Standard Type One TSOP





VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	May 2000	-	Initial Issued
A2	Nov. 2000	1, 2, 3, 4, 7	Add in 5V specification
		1, 9	Modify package as 330 mil SOP and standard type one TSOP (8 mm × 13.4 mm)
		2, 3, 7, 8	Add in LE, LI specification
A3	Dec. 2000	2, 4, 5	Modify the 3.3V ±10%, to 3.3V ±5%
A4	Jun. 2001	8	Correct Ordering Information SOP description
		8	Correct Standby Current
A5	Oct. 3, 2001	4	Correct Write Recover Time (TWR) parameter



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Note: All data and specifications are subject to change without notice.

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