Ultra Low-Power ARM Cortex-M3 MCU with Integrated Power Management

Preliminary Technical Data

ADuCM3027/ADuCM3029

FEATURES

- Ultra low-power active and hibernate modes
  - Active < 38 µA/MHz (typical)
  - Flexi < 11.5 µA/MHz (typical)
  - Hibernate < 750 nA (typical)
  - Shutdown < 60 nA (typical)
- ARM® Cortex®-M3 processor with MPU
  - Up to 26 MHz with serial wire debug interface
- Power management
  - Single supply operation
    - Wide voltage range (VBAT): 1.8 V to 3.6 V
  - Coin-cell battery compatible
  - Internally generated 1.2 V (typical) domain with the following options:
    - LDO+ Buck converter for improved efficiency (optional)
    - LDO only
  - Power modes
    - Active – Full on mode
    - Flexi – Autonomous sensor data movement with processor sleeping
    - Hibernate – With configurable SRAM retention
    - Shutdown – With optional RTC active
  - Power Supply Monitor (PSM)
  - Power-on Reset (POR)
- Memory options
  - 128/256K bytes of embedded flash memory with ECC[1]
  - 4K bytes of cache memory to reduce active power when executing from flash
  - 64K bytes of configurable system SRAM with parity with the following options:
    - 32K_ISRAM+32K_DSRAM, CACHE OFF
    - 28K_ISRAM+32K_DSRAM, 4K_CACHE
    - 64K_DSRAM, CACHE OFF
    - 60K_DSRAM, 4K_CACHE
- Security/Safety
  - Hardware Crypto Accelerator supporting AES-128, AES-256 along with various modes (ECB, CBC, CTR, CBC-MAC, CCM, CCM*) and SHA-256
  - Watchdog timer operating using independent 32 kHz on-chip oscillator
  - True Random Number Generator (TRNG)
  - Hardware CRC with programmable generator polynomial
  - Multi parity-bit-protected SRAM
  - User code protection
    - Protects customer IP software
    - Prevents re-purposing the part
    - Secure software upgrade via UART

DIGITAL PERIPHERALS

- 3 X SPI interface with hardware flow control to enable glueless interface to sensors, radios, and converters
- I^2C and UART peripheral interfaces
- SPORT for natively interfacing with converters and radios
- Programmable GPIOs
- 3 X general-purpose timers
- 1 X RTC, 1 X FLEX_RTC
  - SensorStrobe™ for synchronization with external sensors to the FLEX_RTC
- Programmable beeper
- 25-channel DMA controller supporting dedicated DMA channels for each peripheral

CLOCKING FEATURES

- 26 MHz clock
  - On-chip oscillator
  - External crystal oscillator
  - SYS_CLKIN for external clock
- 32 kHz clock
  - On-chip oscillator
  - Low-power crystal oscillator
- Integrated PLL with programmable divider

ANALOG PERIPHERALS

- Up to 1.8 MSPS housekeeping ADC
  - 12-bit SAR
  - Eight channels, single ended
  - Digital comparator
- High-precision voltage reference
- Temperature sensor

PACKAGES AND TEMPERATURE RANGE

- 64-pin LFCSP, 54-pin WLCSP
- Industrial temperature range

[1] Flash memory size varies by product.
See Table 1 (Product Offerings) for more information.

Rev. PrF
Document Feedback

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GENERAL DESCRIPTION

The ADuCM302x processor is an ultra low-power integrated mixed-signal microcontroller system for processing, control and connectivity. The MCU system is based on ARM Cortex-M3 processor, a collection of digital peripherals, embedded SRAM and flash memory, and an analog subsystem which provides clocking, reset and power management capability in addition to an ADC subsystem. For a feature comparison across ADuCM302x product offerings, see Table 1.

Table 1. Product Offerings

Part Number[1]	Embedded Flash Memory Size
ADuCM3027	128K bytes
ADuCM3029	256K bytes

[1] ADuCM3029 replaces ADuCM3025. The ADuCM3025 has no ADC.

System features that are common across all ADuCM302x processors include the following:

- Up to 26 MHz ARM Cortex-M3 processor
- Up to 256K bytes of embedded flash memory with ECC
- Optional 4K cache for lower active power
- 64K bytes system SRAM with parity
- Power Management Unit (PMU)
- Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
- Central direct memory access (DMA) controller
- Beeper interface
- SPORT, SPI, I²C, and UART peripheral interfaces
- Crypto hardware support with AES and SHA256
- Real time clock (RTC)
- General-purpose and watchdog timers
- Programmable general-purpose I/O pins
- Hardware CRC calculator with programmable generator polynomial
- Power-on Reset (POR) and Power Supply Monitor (PSM)
- 12-bit SAR analog-to-digital converter
- True random number generator (TRNG)

To support extremely low dynamic and hibernate power management, the ADuCM302x processor provides a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

For full details on the ADuCM302x processor, refer to the *ADuCM302x Mixed-Signal Control Processor with ARM Cortex-M3 Hardware Reference.*

ARM CORTEX-M3 PROCESSOR

The ARM Cortex-M3 core shown in Figure 1, is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8 bits, 16 bits, or 32 bits. The length of the instruction word is 16 or 32 bits.

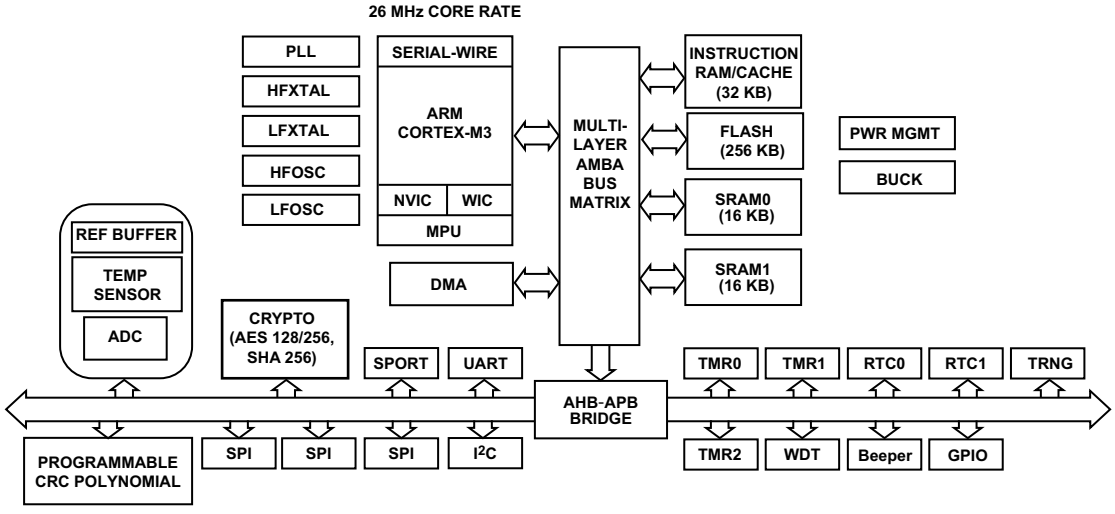


Figure 1. Functional Block Diagram

The processor has the following features:

- Cortex-M3 Architecture
  - Thumb-2 ISA technology
  - 3-stage pipeline with branch speculation
  - Low-latency interrupt processing with tail chaining
  - Single cycle multiply
  - Hardware divide instructions
  - NVIC interrupt controller (64 interrupts and 8 priorities)
  - Two breakpoints and one watchpoint (unlimited software breakpoints using Segger JLink)
- MPU
  - 8-region MPU with subregions and background region
  - Programmable clock generator unit
- Configurable for ultra low-power operation
  - Deep sleep mode, dynamic power management
  - Programmable clock generator unit

MEMORY ARCHITECTURE

The internal memory of the ADuCM302x processor is shown in Figure 2. This processor incorporates up to 256K bytes of embedded flash memory for program code and nonvolatile data storage, 32K bytes of data SRAM, and 32K bytes of SRAM (which is configurable between instruction space and data space).

SRAM Region

This memory space contains the application instructions and literal (constant) data which must be executed real time. It supports read/write access by the ARM Cortex-M3 core and read/write DMA access by system peripherals. Byte, half word and word accesses are supported.

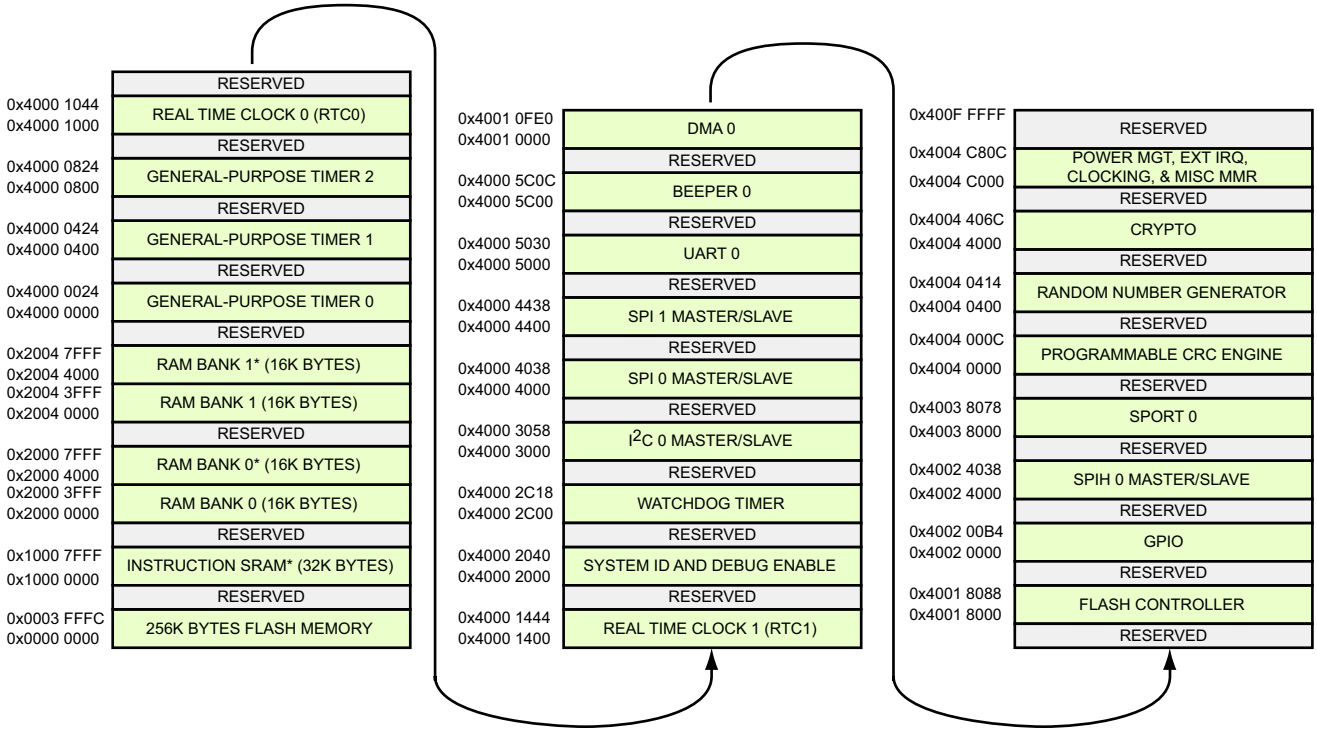
SRAM is divided into data SRAM of 32K bytes and Instruction SRAM of 32K bytes. If instruction SRAM is not enabled, then the associated 32K bytes can be mapped as data SRAM, resulting in 64K bytes data SRAM.

Parity bit error detection (optional) is available on all SRAM memories. Two parity bits are associated with each 32-bit word.

When cache controller is enabled, 4K bytes of the instruction SRAM are reserved for cache memory.

During hibernate mode, up to 32K bytes of SRAM may be retained:

- Out of 32K bytes instruction SRAM, option to retain 16K bytes
- Out of 32K bytes of data SRAM, option to retain 8K bytes or 16K bytes



* See the "SRAM Region" description in the "Introduction" chapter of the processor hardware reference for more information.

Figure 2. ADuCM302x Memory Map

Memory-Mapped Registers (Peripheral Control/Status)

Refer to Figure 2 for the address space containing memory-mapped registers. These registers provide control and status for the processor's on-chip peripherals.

Flash Memory

The ADuCM302x processor includes 128K to 256 bytes of embedded flash memory, which is accessed using a flash controller. For memory available on each product, see Table 1. The flash controller is coupled with a cache controller which provides two AHB ports: one port for reading data (DCode), the other for reading instructions (ICode). A prefetch mechanism is implemented in the flash controller to optimize ICode read performance.

Flash writes are supported by a key-hole mechanism via APB writes to memory mapped registers. The flash controller provides support for DMA-based key-hole writes.

With respect to flash integrity, the device supports:

- A fixed user key required for running protected commands including mass erase and page erase
- An optional and user definable user failure analysis key (FAA key); if set, this key may be required by Analog Devices personnel when performing failure analysis
- An optional and user definable write protection for user accessible memory
- An optional 8-bit error correction code (ECC); this code may be enabled by user code (off by default)

Cache Controller

The ADuCM302x family has an optional 4K byte instruction cache. In certain applications enabling the cache and executing the code can result in lower power consumption than operating directly from flash. When the cache controller is enabled, 4K bytes of instruction SRAM is reserved for cache data. In hibernate mode, the cache memory is not retained.

ARM Cortex-M3 Memory Subsystem

The memory map of the ADuCM302x family is based on the Cortex-M3 model from ARM. By retaining the standardized memory mapping, it becomes easier to port applications across M3 platforms.

ADuCM302x application development is typically based on memory blocks across CODE/SRAM regions. Sufficient internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in this region (0x0000 0000 to 0x0003 FFFF) are performed by the core on its ICODE and DCODE interfaces, and they target the memory and cache resources.

SRAM Region

Accesses in this region (0x2000 0000 to 0x2004 7FFF) are performed by the ARM Cortex-M3 core on its SYS interface. The SRAM region of the core can otherwise act as a data region for an application.

- **Internal SRAM Data Region.** This space can contain read/write data. Internal SRAM can be partitioned between CODE and DATA (SRAM region in M3 space) in 32K byte blocks. Access to this region occurs at core clock speed, with no wait states. It supports read/write access by the M3 core and read/write DMA access by system devices. It supports exclusive memory accesses via the global exclusive access monitor within the Analog Devices Cortex-M3 platform.
- **System MMRs.** Various system MMRs reside in this region.

System Region

Accesses in this region (0xE000 0000 to 0xF7FF FFFF) are performed by the ARM Cortex-M3 core on its SYS interface, and are handled within the Analog Devices Cortex-M3 platform.

- **CoreSight ROM.** The ROM table entries point to the debug components of the processor.
- **ARM PPB Peripherals.** This space is defined by ARM and occupies the bottom 256K bytes of the SYS region (0xE000 0000 to 0xE004 0000). The space supports read/write access by the M3 core to the ARM core's internal peripherals (SCS, NVIC, WIC) and the CoreSight ROM. It is not accessible by system DMA.
- **Platform Control Registers.** This space has registers within the Analog Devices Cortex-M3 platform component that control the ARM core, its memory, and the code cache. It is accessible by the M3 core via its SYS port (but is not accessible by system DMA).

SYSTEM AND INTEGRATION FEATURES

The ADuCM302x processor provides a number of features that ease system integration.

Processor Reset

There are four kinds of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the Cortex core.

A hardware reset is performed by toggling the $\overline{\text{SYS\_HWRST}}$ pin, which is active low.

Booting

The processor supports two boot modes: booting from internal flash and upgrading software through UART download.

Table 2. Boot Modes

Boot Mode	Description
0	UART download mode
1	Flash boot. Boot from integrated flash memory.

Security Features

The processor provides a combination of hardware and software protection mechanisms that lock out access to the part in secure mode, but grant access in open mode. These mechanisms include password-protected slave boot modes (SPI and UART), as well as password-protected SWD debug interfaces.

- Mechanisms are provided to protect the device contents (flash, SRAM, CPU registers, and peripheral registers) from being read through an external interface by an unauthorized user. This is referred to as read-protection.
- It shall be possible to protect the device from being reprogrammed in-circuit with unauthorized code. This is referred to as in-circuit write-protection.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

The device can be configured with no protection, read protection, or read and in-circuit write protection. It is not necessary to provide in-circuit write protection without read protection.

Reliability and Robustness Features

The processor provides a number of features which can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness:

- **ECC enabled flash memory.** The entire flash array can be protected to either correct single bit errors or detect two-bit errors per 64-bit flash data.
- **Multi-parity-bit-protected SDRAM.** In the processor's SRAM and cache memory space, each word is protected by multiple parity bits to allow detection of random soft errors.
- **Software watchdog.** The on-chip watchdog timer can provide software-based supervision of the ADuCM3027/ADuCM3029 core.

Crypto Accelerator

Crypto is a 32-bit APB DMA capable peripheral. There are two buffers provided for data I/O operations. These buffers are 32-bit wide and read in or read out 128 bits in 4 data accesses. Big Endian and Little Endian data formats are supported.

Supported modes

- ECB mode - AES mode
- CTR mode - Counter mode
- CBC mode - Cipher block chaining mode
- MAC mode - Message authentication code mode
- CCM/CCM* mode -Cipher block chaining-message authentication code mode
- SHA-224 and SHA-256 modes

CRC Accelerator

The CRC accelerator can be used to compute the CRC for a block of memory locations. The exact memory location can be in the SRAM, flash, or any combination of memory mapped registers. The CRC accelerator generates a checksum that can be used to compare it with an expected signature.

The main features of the CRC include:

- Generates a CRC signature for a block of data
- Supports programmable polynomial length of up to 32 bits
- Operates on 32 bit of data at a time
- Supports MSB first as well as LSB first implementations of CRC
- Various data mirroring capabilities
- Initial seed to be programmed by user
- DMA controller (memory-to-memory transfer) used for data transfer to offload the processor

True Random Number Generator

The random number generator is used during operations where nondeterministic values are required. This may include generating challenges for secure communication or keys used for an encrypted communication channel. The generator can be run multiple times to generate a sufficient number of bits for the strength of the intended operation. The true random number generator can be used to seed a deterministic random bit generator.

Programmable GPIOs

The ADuCM302x processor has 44 GPIO pins, most of which have multiple, configurable functions defined by user code. They can be configured as an I/O and have programmable pull-up resistors. All I/O pins are functional over the full supply range.

In power-saving mode, GPIO pins retain state; they tristate on reset to prevent any bus irritation.

Timers

The processor contains general-purpose timers and a watchdog timer.

General-Purpose Timers

The ADuCM302x processor has three identical general-purpose timers, each with a 16-bit count-up/count-down counter. The count-up/count-down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

Watchdog Timer (WDT)

The watchdog timer is a 16-bit count-down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The watchdog timer is clocked by the 32 kHz on-chip oscillator (LFOSC).The watchdog timer (WDT) is used to recover from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt of the processor.

ADC (Analog-to-Digital Converter)

The ADuCM302x processor integrates a 12-bit analog-to-digital converter with up to eight external channels. Conversions can be performed in single or auto cycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the channels. Auto cycle mode is provided to reduce processor overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using dedicated channels. Temperature sensing and battery monitoring cannot be included in auto cycle mode.

A digital comparator is provided to allow an interrupt to be triggered if ADC input is above or below a programmable threshold. Input channels AIN0, AIN1, AIN2, and AIN3 can be used with the digital comparator.

ADC can be used in DMA mode to reduce processor overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions has been completely logged to memory.

The main features of the ADC subsystem include:

- 12-bit resolution
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS
- Integrated input mux that supports up to eight channels
- Temperature sensing support
- Battery monitoring support
- Software-selectable on-chip reference voltage generation: 1.25 V, 2.5 V, VBAT
- Software-selectable internal or external reference
- Auto cycle mode: Ability to automatically select a sequence of input channels for conversion
- Averaging function: Converted data on single or multiple channels can be averaged over up to 256 samples
- Alert function: Internal digital comparator for AIN0, AIN1, AIN2, and AIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above/below a user-defined threshold.
- Dedicated DMA channel support
- Each channel, including temperature sensor and battery monitoring, has its own data register for conversion result

Power Management

The ADuCM302x processor includes power management and clocking features, relating to power modes and power management.

Power Modes

The PMU provides control of the ADuCM302x processor power modes and allows the ARM Cortex-M3 to control the clocks and power gating to reduce the dynamic power and hibernate power.

There are a number of power modes available; each mode provides an additional low-power benefit with a corresponding reduction in functionality.

- Active mode – All peripherals can be enabled. Active power is managed by optimized clock management.
- Flexi mode – The core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals and memory.
- Hibernate mode – This mode provides configurable SRAM and port pin retention, a limited number of wake-up interrupts, and (optionally) an active RTC.
- Shutdown mode – This mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from 4 possible wake-up sources. The RTC can be (optionally) enabled in this mode and the part can be periodically woken up by the RTC interrupt.

Power Management

The ADuCM302x processor has an integrated power management system to optimize performance and extend battery life of the device.

The power management system consists of:

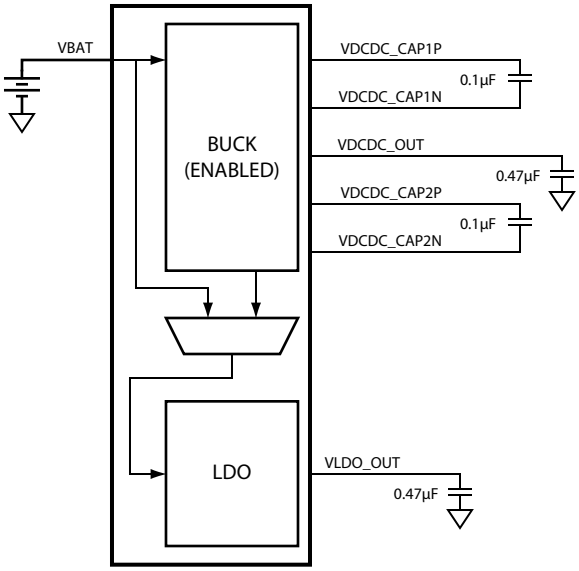
- Integrated 1.2 V LDO and optional Buck
- Hibernate mode
- Integrated power switches for low standby current in hibernate mode

Additional power management features include:

- Customized clock gating for active modes
- Power gating to reduce leakage in hibernate/shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency Buck converter to reduce power
- Integrated low-power oscillators

The following features are available for power management and control:

- Full-on mode: See Table 4 for details on active mode power.
- Low-power mode:
  - Lower leakage if using internal oscillator or external wake-up source
  - See Table 5 for low power mode specifications
- Voltage range of 1.8 V to 3.6 V, using a single supply (such as the CR2032)
- Pad I/O is driven directly from the battery. The I/O configuration and pin state are retained in hibernate mode.
- Wake-up from external interrupt (GPIO) and RTC
- (Optional) High-power Buck converter for 1.2 V full on support; for processor usage only. See Figure 3 for suggested external circuitry



Note: The figure shows a Buck enabled design. For designs in which the optional Buck is not used, the following pins must be left unconnected—VDCDC_CAP1P, VDCDC_CAP1N, VDCDC_OUT, VDCDC_CAP2P, and VDCDC_CAP2N.

Figure 3. Buck Enabled

Clocking

The ADuMC302x processor has the following clocking options:

- 26 MHz
  - Internal oscillator – HFOSC (26 MHz)
  - External crystal oscillator – HFXTAL (26 or 16 MHz)
  - GPIO clock in – SYS_CLK_IN
- 32 kHz
  - Internal oscillator – LFOSC
  - External crystal oscillator –LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled for use cases where internal Buck regulator is used
- LFOSC cannot be disabled even if LFXTAL is used

Real-Time Clock

The ADuCM302x processor has two real-time clock blocks, RTC0 and RTC1 (also called FLEX_RTC). The clock blocks share a low-power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC and correlates the count to the time of day.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

FLEX_RTC supports a unique feature, SensorStrobe via Output Compare Pin (OPCx). Using this feature, the ADuCM302x processor can be used as a programmable clock generator in all power modes including the Hibernate mode. In this way, the external sensors can have their timing domains mastered by the ADuC302x processor, as the OPC can output a programmable divider from FLEX_RTC, which can operate up to a resolution of 30.7 us. The sensors and microcontroller are in sync, which removes the need for additional re-sampling of data to time-align it.

In the absence of this feature:

- The external sensor uses its own RC oscillator (~+/-30% typical variation). The processor has to sample the data and re-sample it on the processor's Time domain before using it.

Or

- The processor remains in a higher power state and drives each data conversion on the sensor side

This feature allows the ADuC302x processor to be in a lower power state for a long duration, and also avoids unnecessary data processing. This extends the battery life of the end product.

The key differences between RTC0 and RTC1 (FLEX_RTC) are shown in Table 3.

Table 3. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of time base (prescaling)	RTC0 counts time at 1 Hz in units of seconds. Operationally, when used by the customer, RTC0 always prescales to 1 Hz (for example, divide by 32,768) and always counts real time in units of seconds.	RTC1 (FLEX_RTC) can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16384, or 32768.
Wake-up timer	Wake-up time is specified in units of seconds.	RTC1 supports alarm times down to a resolution of 30.7µs, i.e. where the time is specified down to a specific 32 kHz clock cycle.
Number of alarms	One alarm only. Uses an absolute, non-repeating alarm time, specified in units of one second.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
Output compare	N/A	Output compare is an alarm function in the RTC which causes an output pulse to be sent via GPIOs to an external device, to instruct that device to take a measurement or perform some action at a specific time. Output compare events are scheduled at a specific target time relative to the real time count of the RTC. Output compare can be enabled in the Hibernate mode.
Input capture	N/A	Input capture takes a snapshot of the RTC real-time count when an external device signals an event via a transition on one of the GPIO inputs to ADuCM302x processor. Typically an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM302x processor that the RTC must take a snapshot of time corresponding to the event. The taking of this snapshot can wake up the ADuCM302x processor and cause an interrupt to its CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle and thus the exact time that the input-capture event occurred.

Beeper Driver

The ADuCM302x processor has an integrated audio driver for a beeper.

The beeper driver module in the ADuCM302x processor generates a differential square wave of programmable frequency. It drives an external piezoelectric sound component whose two terminals connect to the differential square wave output.

The beeper driver consists of a module that can deliver frequencies from 8 kHz to ~0.25 kHz. It operates on a fixed independent 32 kHz (32,768 Hz) clock source that is unaffected by changes in system clocks.

A timer allows for programmable tone durations from 4 ms to 1.02 s in 4 ms increments. Single-tone (pulse) and multi-tone (sequence) modes provide versatile playback options.

In sequence mode, the beeper can be programmed to play any number of tone pairs from 1 to 254 (2 to 508 tones) or be programmed to play forever (until stopped by the user). Interrupts are available to indicate the start or end of any beep, the end of a sequence, or that the sequence is nearing completion.

Debug Capability

The ADuMC320x processor supports serial wire debug.

ON-CHIP PERIPHERAL FEATURES

The processor contains a rich set of peripherals connected to the core via several concurrent high-bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1).

The processor contains high-speed serial ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

Serial Ports (SPORT)

The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. The frame sync and clock are shared. Some of the ADCs/DACs require two control signals for their conversion process. To interface with such devices, an extra signal SPT_CONVT signal is provided. To use this signal, enable the timer enable mode. In this mode, a PWM timer inside the module is used to generate the programmable SPT_CONVT signal.

Serial ports operate in two modes:

- Standard DSP serial mode
- Timer enable mode

Serial Peripheral Interface (SPI) Ports

SPI is an industry standard, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received, that is, full duplex. The SPI incorporates two DMA channels that interface with the DMA controller. One DMA channel is used for transmit and the other is used for receive. The SPI on the processor eases interfacing to external serial flash devices.

The SPI features include the following:

- Serial clock phase mode and serial clock polarity mode
- Loopback mode
- Continuous transfer mode
- Wired-OR output mode
- Read-command mode for half-duplex operation (Tx first and Rx next)
- Flow control support
- Multiple CS line support
- CS software override support
- Support for 3-pin SPI

UART Port

The processor provides a full-duplex UART port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, and none, even, or odd parity. A frame is terminated by one, one and a half, or two stop bits.

I^2C

The I^2C bus peripheral has two pins for data transfer. SCL is a serial clock and SDA is a serial data pin. The pins are configured in a Wired-AND format that allows arbitration in a multi-master system. A master device can be configured to generate the serial clock. The frequency is programmed by the user in the serial clock divisor register. The master channel can be set to operate in fast mode (400 kHz) or standard mode (100 kHz).

DEVELOPMENT SUPPORT

Development support for the ADUCM302x processor includes documentation, evaluation hardware, and development software tools.

Documentation

The *ADuCM302x Mixed-Signal Control Processor with ARM Cortex-M3 Hardware Reference* details the functionality of each block on the ADuCM302x processor. It includes power management, clocking, memories, peripherals, and the AFE.

Hardware

The EVAL-ADuCM302xEBZ evaluation kit is available to prototype a user's sensor configuration with theADuCM302x processor.

Software

The EVAL-ADuCM302xEBZ includes a complete development and debug environment for the ADuCM302x processor. The software development kit (SDK) for the ADuCM302x processor uses the IAR Embedded Workbench for ARM as its development environment.

The SDK also includes operating system (OS) aware drivers and example code for all the peripherals on the device, including SPI and I^2C.

ADDITIONAL INFORMATION

The following publications that describe the ADuCM302x processors can be ordered from any Analog Devices sales office or accessed electronically on our website:

- *ADuCM302x Mixed-Signal Control Processor with ARM Cortex-M3 Hardware Reference*
- *ADuCM302x Mixed-Signal Microcontroller Anomaly List*

This document describes the ARM Cortex-M3 core and memory architecture used on the ADuCM302x processor, but does not provide detailed programming information for the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M3 processor include:

- *ARM Cortex-M3 Devices Generic User Guide*
- *ARM Cortex-M3 Technical Reference Manual*

RELATED SIGNAL CHAINS

A signal chain is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The application signal chains page in the Circuits from the Lab® site (http://www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

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SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Condition	Min	Nominal	Max	Unit
V_{BAT}[1,2]	External Battery Supply Voltage		1.8	3.0	3.6	V
V_{IH}	High Level Input Voltage	V_{BAT} = 3.6 V	2.5			V
V_{IL}	Low Level Input Voltage	V_{BAT} = 1.8 V			0.45	V
V_{BAT_ADC}	ADC Supply Voltage		TBD	TBD	TBD	V
T_J	Junction Temperature	$T_{AMBIENT}$ = −40°C to +85°C	−40		85	°C

[1] Must remain powered (even if the associated function is not used).
[2] Value applies to VBAT_ANA1,VBAT_ANA2,VBAT_DIG1,VBAT_DIG2 pin

ELECTRICAL CHARACTERISTICS

Parameter		Condition	Min	Typical	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{BAT} = Min V, I_{OH} = −1.0 mA	1.4			V
V_{OL}[1]	Low Level Output Voltage	V_{BAT} = Min V, I_{OL} = 1.0 mA			0.4	V
I_{IHPU}[2]	High Level Input Current Pull-Up	V_{BAT} = Max V, V_{IN} = V_{BATMAX} V		0.01	1	µA
I_{ILPU}[2]	Low Level Input Current Pull-Up	V_{BAT} = Max V, V_{IN} = 0 V			100	µA
I_{OZH}[3]	Three-State Leakage Current	V_{BAT} = Max V, V_{IN} = $V_{BAT\ MAX}$ V		0.01	1	µA
I_{OZL}[3]	Three-State Leakage Current	V_{BAT} = Max V, V_{IN} = 0 V		0.01	1	µA
I_{OZLPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = Max V, V_{IN} = 0 V			100	µA
I_{OZHPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = Max V, V_{IN} = $V_{BAT\ MAX}$ V			1	µA
I_{OZLPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = Max V, V_{IN} = 0 V			1	µA
I_{OZHPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = Max V, V_{IN} = $V_{BAT\ MAX}$ V			100	µA
C_{IN}[6]	Input Capacitance	f_{IN} = 1 MHz, T_J = 25°C, V_{IN} = TBD V		10		pF

[1] Applies to output and bidirectional pins: P1_10, P0_10, P0_11, P1_2, P1_3, P1_4, P1_5, P2_1, P0_13, P0_15, P1_0, P1_1, P1_15, P2_0, P0_12, P2_11, P1_6, P1_7, P1_8, P1_9, P0_0, P0_1, P0_2, P0_3, P0_6, P0_7, P2_4, P2_10, P0_4, P0_5, P0_14, P2_2, P1_14, P1_13, P1_12, P1_11, P0_8, P0_9.
[2] Applies to input pins with pull-up: $\overline{\text{SYS\_HWRST}}$.
[3] Applies to three-statable pins: P1_10, P0_10, P0_11, P1_2, P1_3, P1_4, P1_5, P2_1, P0_13, P0_15, P1_0, P1_15, P2_0, P0_12, P2_11, P1_6, P1_7, P1_8, P1_9, P0_0, P0_1, P0_2, P0_3, P2_4, P2_10, P0_4, P0_5, P0_14, P2_2, P1_14, P1_13, P1_12, P1_11, P0_8, P0_9.
[4] Applies to three-statable pins with pull-ups: P1_10, P0_10, P0_11, P1_2, P1_3, P1_4, P1_5, P2_1, P0_13, P0_15, P1_0, P1_15, P2_0, P0_12, P2_11, P1_6, P1_7, P1_8, P1_9, P0_0, P0_1, P0_2, P0_3, P2_4, P2_10, P0_4, P0_5, P0_14, P2_2, P1_14, P1_13, P1_12, P1_11, P0_8, P0_9, P0_7, P1_1.
[5] Applies to three-statable pin with pull-down: P0_6.
[6] Guaranteed, but not tested.

Power Supply Current

Table 4 and Table 5 describe power supply current for V_{BAT} as it relates to a variety of operating modes and conditions.

Table 4. Active Mode—Current Consumption from V_{BAT} = 3.0 V

Mode/Condition	Buck Enabled/ Disabled	Typ[1]	Max[2]	Unit
Active Mode: Code[3] Executing from FLASH, With Cache Enabled	Enabled	0.98	TBD	mA
Peripheral Clocks OFF, HCLK = 26 MHz	Disabled	1.75	TBD	mA
Active Mode: Code[3] Executing from FLASH, With Cache Disabled	Enabled	1.28	TBD	mA
Peripheral Clocks OFF, HCLK = 26 MHz	Disabled	2.34	TBD	mA
Active Mode: Code[3] Executing from SRAM	Enabled	0.95	TBD	mA
Peripheral Clocks OFF, HCLK = 26 MHz	Disabled	1.78	TBD	mA
Active Mode: Code[3] Executing from FLASH, With Cache Enabled	Enabled	1.08	TBD	mA
Peripheral Clocks ON, HCLK = 26 MHz, PCLK = 26 MHz	Disabled	1.99	TBD	mA
Active Mode: Code[3] Executing from FLASH, With Cache Disabled	Enabled	1.37	TBD	mA
Peripheral Clocks ON, HCLK = 26 MHz, PCLK = 26 MHz	Disabled	2.55	TBD	mA
Active Mode: Code[3] Executing from SRAM	Enabled	1.08	TBD	mA
Peripheral Clocks ON, HCLK = 26 MHz, PCLK = 26 MHz	Disabled	2.03	TBD	mA
Flexi Mode: Peripheral Clocks OFF	Enabled	0.3	TBD	mA
	Disabled	0.52	TBD	mA
Flexi Mode: Peripheral Clocks ON, PCLK = 26 MHz	Enabled	0.39	TBD	mA
	Disabled	0.7	TBD	mA

[1] T_J = 25°C.
[2] T_J = 85°C.
[3] Code being executed is prime number generation in a continuous loop, with HFOSC as the system clock source.

Table 5. Low Power Mode[1]—Current Consumption from V_{BAT} = 3.0 V

Mode	Condition	-40°C Typ	25°C Typ	85°C Typ	85°C Max	Unit
Hibernate	RTC 1,0 Disabled + 8K bytes SRAM retained, LFXTAL = OFF	TBD	0.75	TBD	TBD	µA
	RTC 1,0 Disabled + 16K bytes SRAM retained, LFXTAL = OFF	TBD	0.77	TBD	TBD	µA
	RTC 1,0 Disabled + 24K bytes SRAM retained, LFXTAL = OFF	TBD	0.79	TBD	TBD	µA
	RTC 1,0 Disabled + 32K bytes SRAM retained, LFXTAL = OFF	TBD	0.81	TBD	TBD	µA
	RTC 1 Enabled +8K bytes SRAM retained, LFOSC as source for RTC1	TBD	0.78	TBD	TBD	µA
	RTC 1 Enabled + 8K bytes SRAM retained, LFXTAL as source for RTC1	TBD	0.83	TBD	TBD	µA
	RTC 1,0 Enabled + 8K bytes SRAM retained, LFXTAL as source for RTC1,0	TBD	0.924	TBD	TBD	µA
Shutdown	RTC 0 Enabled, LFXTAL as source for RTC0	TBD	340	TBD	TBD	nA
	RTC 0 Disabled	TBD	56	TBD	TBD	nA

[1] Buck Enable/Disable selection does not affect power consumption in low-power mode.

SYSTEM CLOCKS/TIMERS

The following tables show the system clock specifications for the ADuCM302x processor.

Platform External Crystal Oscillator

Table 6. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Condition/Comment
LOW FREQUENCY					
CEXT1 = CEXT2	TBD	8	TBD	pF	External capacitor, C1 = C2 (symmetrical load)
Frequency		32,768		Hz	
HIGH FREQUENCY					
CEXT1 = CEXT2	TBD	20	TBD	pF	External capacitor
Frequency		16 or 26		MHz	

On-Chip RC Oscillators

Table 7. On-Chip RC Oscillators Specifications

Parameter	Min	Typ	Max	Unit	Condition/Comment
HIGH FREQUENCY RC OSCILLATOR					
Frequency	TBD	26	TBD	MHz	
LOW FREQUENCY RC OSCILLATOR					
Frequency	TBD	32,768	TBD	Hz	

ADC SPECIFICATIONS

Table 8. ADC Specifications

Parameter	Test Conditions	Typ	Unit
Offset Error	TBD	TBD	LSB
Gain Error	TBD	TBD	LSB
Differential Linearity Error	TBD	TBD	LSB
Integral Linearity Error	TBD	TBD	LSB

FLASH SPECIFICATIONS

Table 9. Flash Specifications

Parameter	Min	Typ	Max	Unit	Condition/Comment
FLASH/GP FLASH					
Endurance	10,000			Cycles	
Data Retention		10		Years	

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 10 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 10. Absolute Maximum Ratings

Parameter	Rating
External Battery Supply Voltage (V_{BAT})	TBD
Digital Input Voltage[1, 2]	TBD
Digital Output Voltage Swing	TBD
Analog Input Voltage	TBD
Voltage Reference Input Voltage	TBD
Storage Temperature Range	TBD
Junction Temperature While Bias	TBD

[1] Applies to 100% transient duty cycle. For other duty cycles, see Table 11.
[2] Applies only when V_{BAT} is within specifications. When V_{BAT} is outside specifications, the range is V_{BAT} ± 0.2 V.

Table 11. Maximum Duty Cycle for Input Transient Voltage[1]

V_{IN} Min (V)	V_{IN} Max (V)	Maximum Duty Cycle
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD

[1] Applies to all signal pins with the exception of SYS_CLKIN, SYS_XTAL.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

The information presented in Table 12 and Figure 4 provides details about package branding. For a complete listing of product availability, see Future (Planned) Products on Page 32.

Figure 4. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 12. Package Brand Information

Brand Key	Field Description
ADuCM3027/ADuCM3029	Product model[1]
t	Temperature range
pp	Package type
Z	RoHS compliant designation
ccc	See Future (Planned) Products
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

[1] See available products in Future (Planned) Products on Page 32.

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Reset Timing

Table 13 and Figure 5 describe reset operation.

Table 13. Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{WRST}	$\overline{SYS\_HWRST}$ Asserted Pulse Width Low[1]	4		µs

[1] Applies after power-up sequence is complete.

Figure 5. Reset Timing

System Clock and PLL

Table 14 describes system clock and PLL specifications.

Table 14. System Clock and PLL

Parameter		Min	Max	Unit
Timing Requirements				
t_{CK}	PLL Input CLKIN Period[1]	38.5	62.5	ns
t_{CKL}	PLL Input CLKIN Width Low	19.2	31.25	ns
t_{CKH}	PLL Input CLKIN Width High	19.2	31.25	ns
f_{PLL}	PLL Output Frequency[2, 3]	16	60	MHz
f_{VCO}	VCO Output Frequency[3, 4]	32	60	MHz
t_{PCLK}	System Peripheral Clock Period	38.5	62.5	ns
t_{HCLK}	AHB Sub System Clock Period	38.5	62.5	ns

[1] The input to the PLL can come either from the high frequency external crystal or from the high frequency internal RC oscillator. Refer to the *ADuCM302x Mixed-Signal Control Processor with ARM Cortex-M3 Hardware Reference*.

[2] For the min value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16, PLL_DIV2 = 1 for PLL input clock = 26 MHz and PLL_MSEL = 13, PLL_NSEL = 26, PLL_DIV2 = 1 for PLL input clock = 16 MHz.

[3] For the max value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 30, PLL_DIV2 = 0 for PLL input clock = 26 MHz and PLL_MSEL = 8, PLL_NSEL = 30, PLL_DIV2 = 0 for 16 MHz.

[4] For the min value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16 for PLL input clock = 26 MHz and PLL_MSEL = 13, PLL_NSEL = 26 for PLL input clock = 16 MHz.

Serial Ports

To determine whether communication is possible between two devices at a particular clock speed, the following specifications must be confirmed:

- Frame sync delay and frame sync setup and hold
- Data delay and data setup and hold
- Serial clock (SPT_CLK) width

In Figure 6 either the rising edge or the falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in MHz is set by the following equation, where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535:

$$f_{SPTCLKPROG} = \frac{f_{PCLK}}{2 \times (CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 15. Serial Ports—External Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	5		ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in either Transmit or Receive Mode)[1]	5		ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	5		ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	8		ns
t_{SCLKW}	SPT_CLK Width[2]	38.5		ns
t_{SPTCLK}	SPT_CLK Period[2]	77		ns
Switching Characteristics				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]		20	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in either Transmit or Receive Mode)[3]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]		20	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	1		ns

[1] Referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.
[3] Referenced to the drive edge.

Table 16. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
Timing Requirements				
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	25		ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	0		ns
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]		20	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	–8		ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]		20	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	–7		ns
t_{SCLKIW}	SPT_CLK Width	t_{PCLK} – 1.5		ns
t_{SPTCLK}	SPT_CLK Period	2 × t_{PCLK} – 1		ns

[1] Referenced to the sample edge.
[2] Referenced to the drive edge.

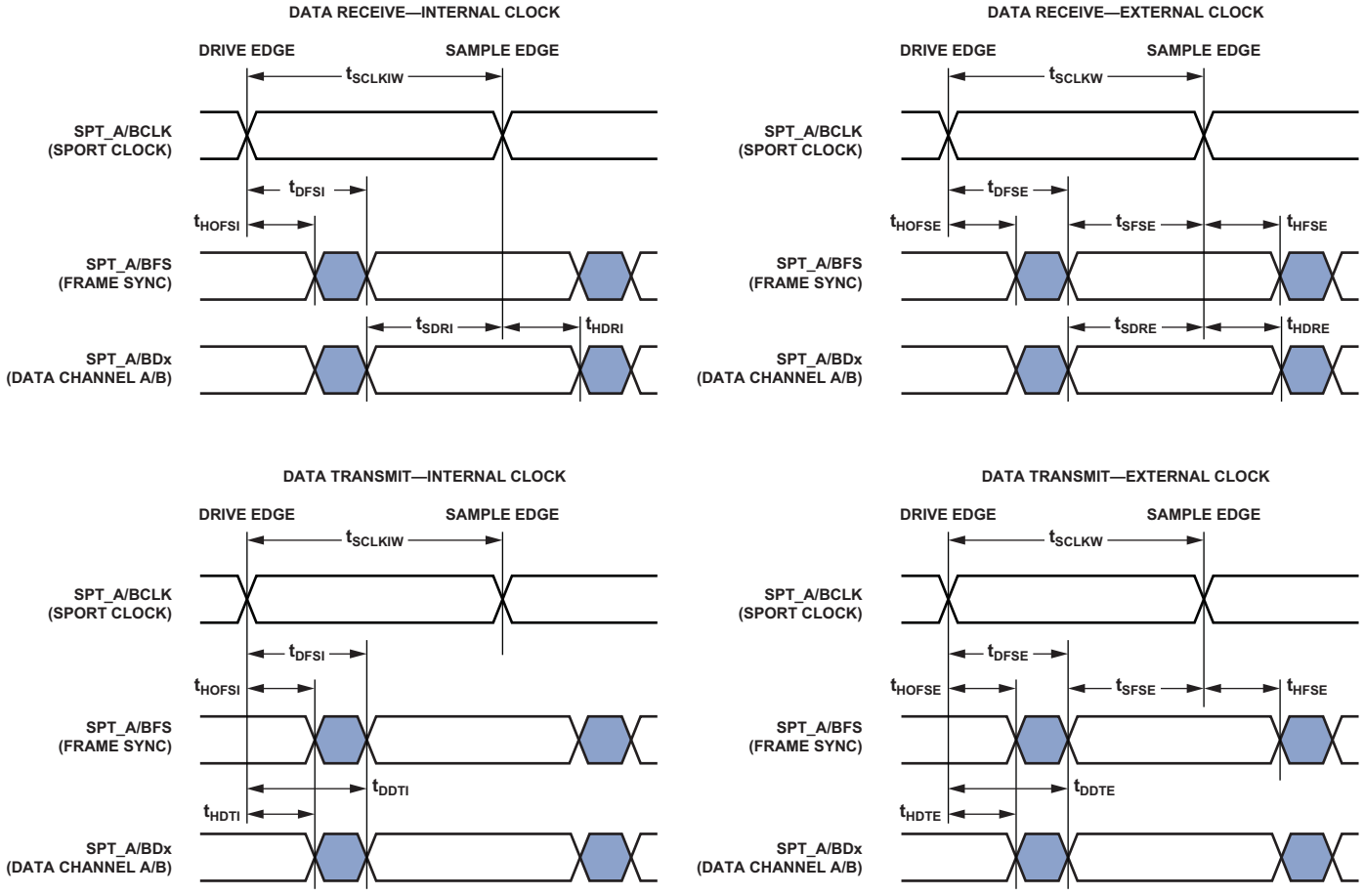


Figure 6. Serial Ports

Table 17. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
Switching Characteristics				
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	3		ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]		160	ns

[1] Referenced to the drive edge.

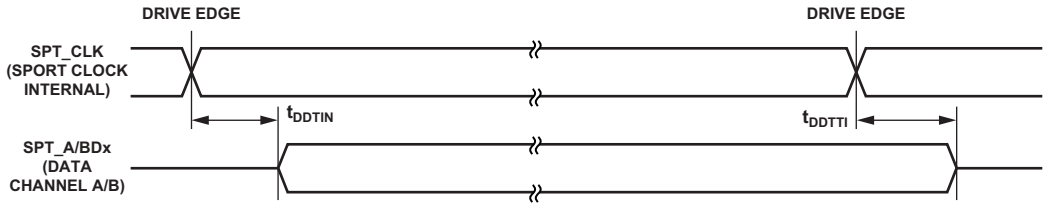


Figure 7. Serial Ports—Enable and Three-State

I²C Serial Interface

The I²C receive and transmit operations are described in the *ADuCM302x Mixed-Signal Control Processor with ARM Cortex-M3 Hardware Reference Manual*.

SPI Timing

Table 18, Figure 8, and Figure 9 (for master mode) and Table 19, Figure 10, and Figure 11 (for slave mode) describe SPI timing specifications. SPIH can be used for high data rate peripherals.

Table 18. SPI Master Mode Timing

Parameter	Description	Min	Max	Unit
t_{SL}	SCLK Low Pulse Width	$t_{PCLK} - 2$		ns
t_{SH}	SCLK High Pulse Width	$t_{PCLK} - 2$		ns
t_{DAV}	Data Output Valid After SCLK Edge		25	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	$t_{PCLK} - 2.2$		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	25		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	0		ns
t_{CS}	$\overline{CS}$ to SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	$0.5 \times t_{PCLK} - 3$		ns

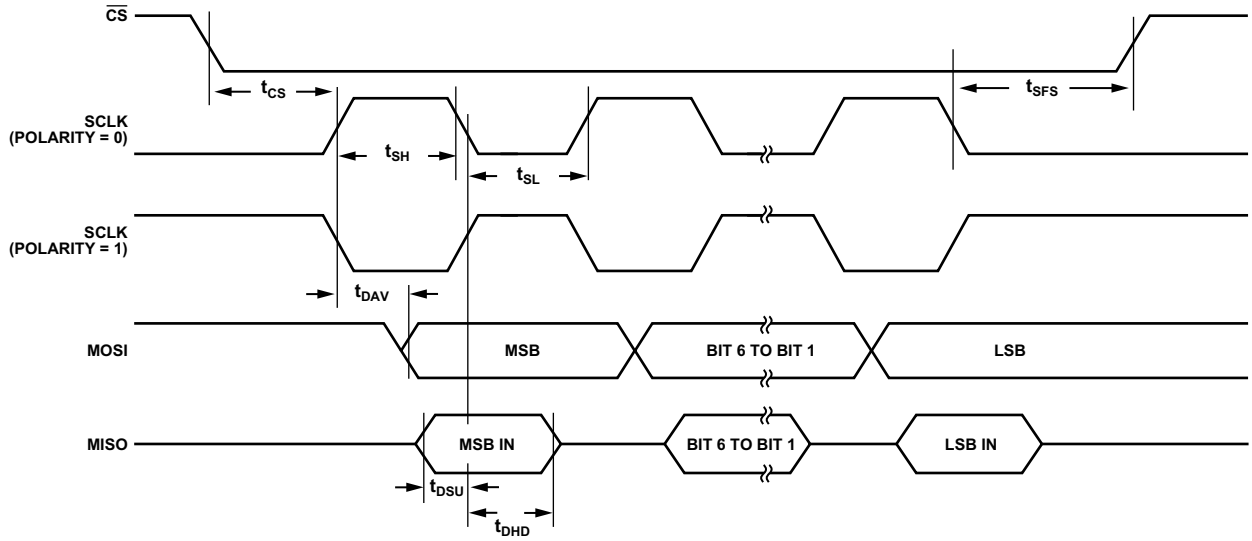


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

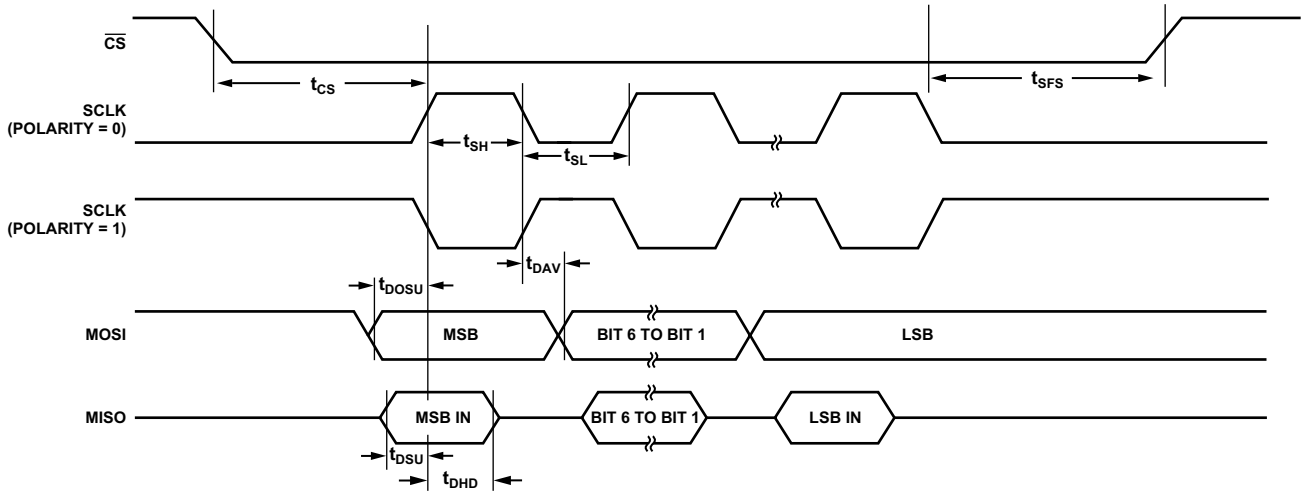


Figure 9. SPI Master Mode Timing (Phase Mode = 0)

Table 19. SPI Slave Mode Timing

Parameter	Description	Min	Max	Unit
t_{CS}	$\overline{CS}$ to SCLK Edge	38.5		ns
t_{SL}	SCLK Low Pulse Width	38.5		ns
t_{SH}	SCLK High Pulse Width	38.5		ns
t_{DAV}	Data Output Valid After SCLK Edge	25		ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	6		ns
t_{DHD}	Data Input Hold Time After SCLK Edge	8		ns
t_{DOCS}	Data Output Valid After $\overline{CS}$ Edge		20	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	38.5		ns

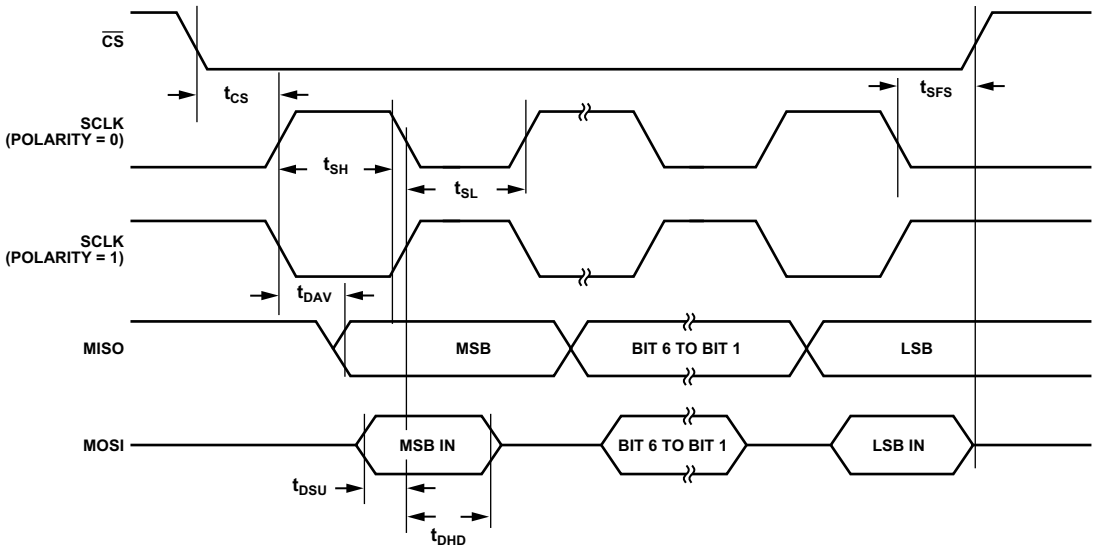


Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

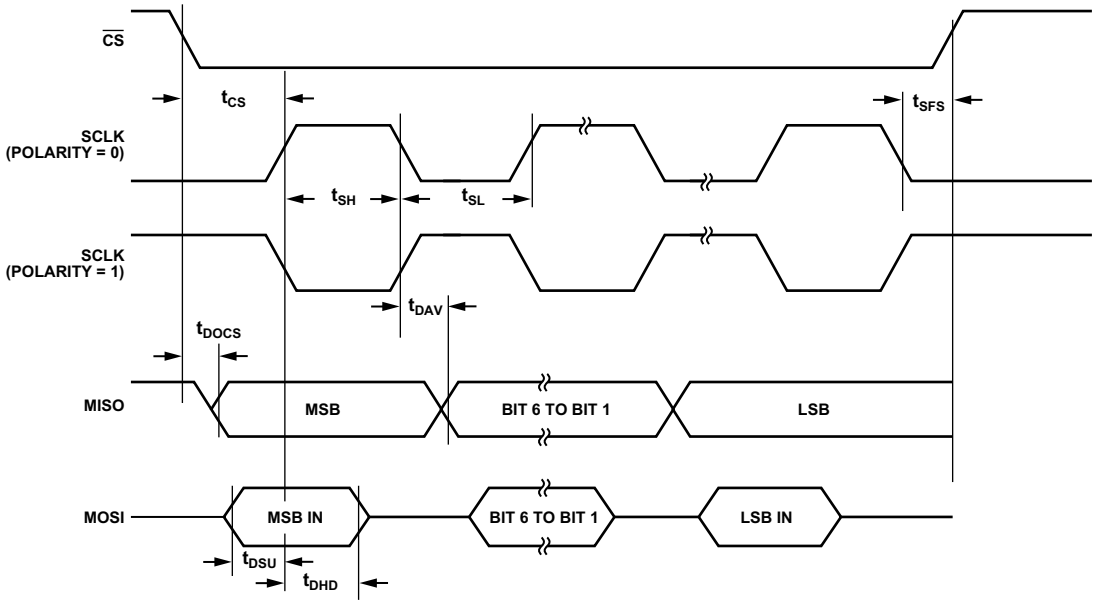


Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

General-Purpose Port Timing

Table 20 and Figure 12 describe general-purpose port operations.

Table 20. General-Purpose Port Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$4 \times t_{PCLK}$		ns

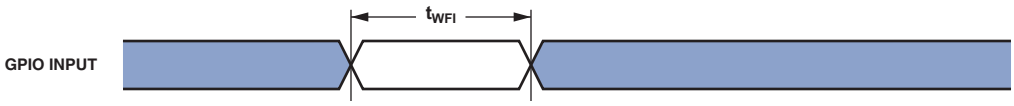


Figure 12. General-Purpose Port Timing

Timer PWM_OUT Cycle Timing

Table 21 and Figure 13 describe timing specifications for PWM_OUT operations.

Table 21. Timer Cycle Timing (Internal Mode)

Parameter		Min	Max	Unit
Switching Characteristic				
t_{PWMO}	Timer Pulse Width Output	$4 \times t_{PCLK} - 2$	$256 \times (2^{16} - 1)$	ns

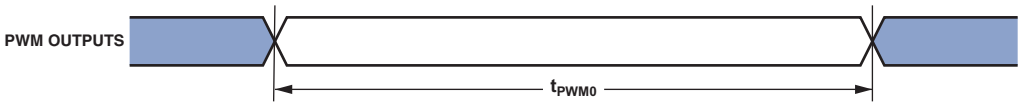


Figure 13. Timer Cycle Timing

(UART) Port—Receive and Transmit Timing

The UART port receives and transmits operations. The port is described in the *ADuCM302x Mixed-Signal Control Processor with ARM Cortex-M3 Hardware Reference*.

PROCESSOR TEST CONDITIONS

The AC signal specifications (timing parameters) appearing in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 14. All delays (in ns/µs) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is set to $V_{BAT}/2$.

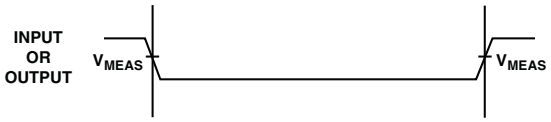
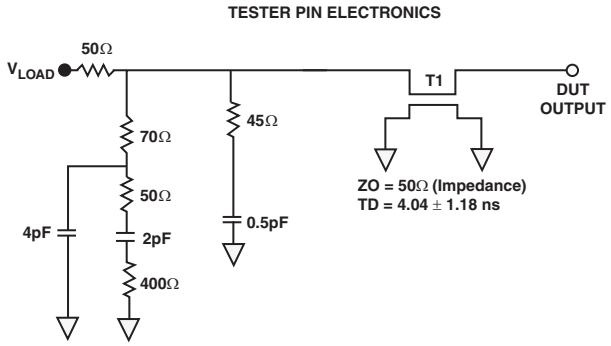


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES:
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 15. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

OUTPUT DRIVE CURRENTS

Table 22 (TBD) shows driver types and Figure 16 (TBD) and Figure 17 (TBD) show typical current-voltage characteristics for the output drivers of the processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 22. Driver Types (TBD)

Driver Type	Associated Pins
TBD	TBD

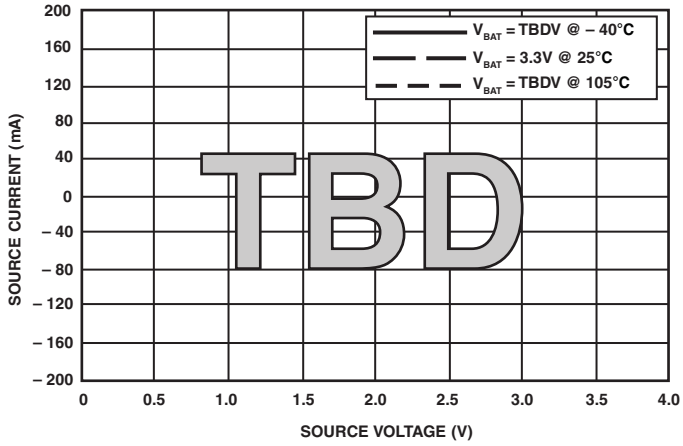


Figure 16. Driver Type A Current

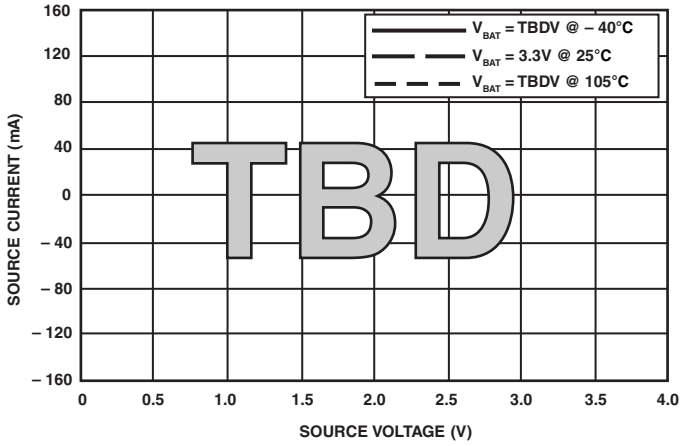


Figure 17. Driver Type B Current

ENVIRONMENTAL CONDITIONS

To determine the junction temperature on the application printed circuit board use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

T_J = Junction temperature (°C)

T_{CASE} = Case temperature (°C) measured by customer at top center of package.

Ψ_{JT} = From Table 23

P_D = Power dissipation (see Power Supply Current on Page 13 to calculate P_D)

Table 23. Thermal Characteristics (64-Lead LFCSP)

Parameter	Condition	Typical	Unit
θ_{JA}	0 linear m/s airflow	TBD	°C/W
θ_{JA}	1 linear m/s airflow	TBD	°C/W
θ_{JA}	2 linear m/s airflow	TBD	°C/W
θ_{JC}		TBD	°C/W
Ψ_{JT}	0 linear m/s airflow	TBD	°C/W
Ψ_{JT}	1 linear m/s airflow	TBD	°C/W
Ψ_{JT}	2 linear m/s airflow	TBD	°C/W

Values of θ_{JA} are provided for package comparison and printed circuit board design considerations. θ_{JA} can be used for a first order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

T_A = Ambient temperature (°C)

Values of θ_{JC} are provided for package comparison and printed circuit board design considerations when an external heat sink is required.

In Table 23, airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6. The junction-to-case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 24. Signal Functional Descriptions

GPIO Signal Name	Description
SPIn_CLK	SPI Clock
SPIn_MOSI	SPI Master Out Slave In
SPIn_MISO	SPI Master In Slave Out
SPIn_RDY	SPI Ready Signal
SPIn_CSm	SPI Chip Select Signal
SPTn_ACLK	SPORT A Clock Signal
SPTn_AFS	SPORT A Frame Sync
SPTn_AD0	SPORT A Data Pin 0
SPTn_ACNV	SPORT A Converter Signal For interface with ADC
SPTn_BCLK	SPORT B Clock Signal
SPTn_BFS	SPORT B Frame Sync
SPTn_BD0	SPORT B Data Pin 0
SPTn_BCNV	SPORT B Converter Signal For interface with ADC
I2Cn_SCL	I2C Clock
I2Cn_SDA	I2C Data
SWD_CLK	Serial Wire Debug Clock
SWD_DATA	Serial Wire Debug Data
BPRn_TONE_N	Beeper Tone Negative Pin
BPRn_TONE_P	Beeper Tone Positive Pin
UARTn_TX	UART Transmit Pin
$\overline{\text{UARTn\_RX}}$	UART Receive Pin
XINT0_WAKEn	System Wake-up Pin (Capable to wake up from hibernate FLEXI/hibernate/shutdown modes)[1]
TMRn_OUT	Timer Output Pin
SYS_BMODE0	Pin when asserted at reset gets boot kernel to UART download mode
SYS_CLKIN	External Clock In pin
SYS_CLKOUT	External Clock Out pin
ADC0_VINn	ADC Voltage Input pin

[1] For shutdown, XINT0_WAKE3 is not capable of waking the part from shutdown mode.

Table 25. 64-Lead FCSP_WQ Package Pin Assignments

Pin #	GPIO#	Signal Name	Description	Default GPIO PULL
1		VBAT_ANA1	Analog 3 V Supply	
2		SYS_HFXTAL_IN	26 MHz High Frequency Crystal	
3		SYS_HFXTAL_OUT	26 MHz High Frequency Crystal	
4		SYS_LFXTAL_IN	32 kHz Low Frequency Crystal	
5		SYS_LFXTAL_OUT	32 kHz Low Frequency Crystal	
6		VDCDC_CAP1N	Buck Fly Cap	
7		VDCDC_CAP1P	Buck Fly Cap	
8		VBAT_ANA2	Analog 3 V Supply	
9		VDCDC_OUT	Buck Output Cap	
10		VDCDC_CAP2N	Buck Fly Cap	
11		VDCDC_CAP2P	Buck Fly Cap	
12		VLDO_OUT	LDO Output (For placing load cap)	
13		VREF_ADC [1]	Analog Reference voltage for ADC	
14		VBAT_ADC	Analog 3 V Supply for ADC	
15		GND_VREFADC [1]	Reference Ground for ADC	
16	P2_03	ADC0_VIN0 / GPIO35 [1]		PU
17	P2_04	ADC0_VIN1 / GPIO36		PU
18	P2_05	ADC0_VIN2 / GPIO37 [2]		PU
19	P2_06	ADC0_VIN3 / GPIO38 [2]		PU
20	P2_07	ADC0_VIN4 / SPI2_CS3 / GPIO39 [2]		PU
21	P2_08	ADC0_VIN5 / SPI0_CS2 / GPIO40 [2]		PU
22	P2_09	ADC0_VIN6 / SPI0_CS3 / GPIO41 [2]		PU
23	P2_10	ADC0_VIN7 / SPI2_CS2 / GPIO42		PU
24	P0_05	I2C0_SDA / GPIO05		PU
25		$\overline{\text{SYS\_HWRST}}$	System Hardware Reset	
26	P0_04	I2C0_SCL / GPIO04		PU
27	P0_07	GPIO07 / SWD0_DATA		PU
28	P0_06	GPIO06 / SWD0_CLK		PD
29	P1_09	SPI1_CS0 / GPIO25		PU
30	P1_08	SPI1_MISO / GPIO24		PU
31	P1_07	SPI1_MOSI / GPIO23		PU
32	P1_06	SPI1_CLK / GPIO22		PU
33	P2_11	SPI1_CS1 / SYS_CLKOUT / GPIO43		PU
34		VBAT_DIG1	Digital 3 V Supply	
35	P0_12	SPT0_AD0 / GPIO12		PU
36	P2_00	SPT0_AFS / GPIO32		PU
37	P1_15	SPT0_ACLK / GPIO31		PU
38	P1_01	GPIO17 / SYS_BMODE0		PU
39	P0_09	BPR0_TONE_P / SPI2_CS1 / GPIO09		PU
40	P0_08	BPR0_TONE_N / GPIO08		PU
41	P1_11	TMR1_OUT / GPIO27		PU
42	P1_12	GPIO28		PU
43	P1_13	GPIO29		PU

Table 25. 64-Lead FCSP_WQ Package Pin Assignments (Continued)

Pin #	GPIO#	Signal Name	Description	Default GPIO PULL
44	P1_14	SPI0_RDY / GPIO30		PU
45	P2_02	SPT0_ACNV / SPI1_CS2 / GPIO34		PU
46	P0_14	TMR0_OUT / SPI1_RDY / GPIO14		PU
47	P1_00	XINT0_WAKE1 / GPIO16		PU
48		GND_DIG	Digital Ground	
49		VBAT_DIG2	Digital 3 V Supply	
50	P0_15	XINT0_WAKE0 / GPIO15		PU
51	P0_13	XINT0_WAKE2 / GPIO13		PU
52	P2_01	XINT0_WAKE3 / TMR2_OUT / GPIO33		PU
53	P1_05	SPI2_CS0 / GPIO21		PU
54	P1_04	SPI2_MISO / GPIO20		PU
55	P1_03	SPI2_MOSI / GPIO19		PU
56	P1_02	SPI2_CLK / GPIO18		PU
57	P0_11	$\overline{\text{UART0\_RX}}$ / GPIO11		PU
58	P0_10	UART0_TX / GPIO10		PU
59	P1_10	SPI0_CS1 / SYS_CLKIN / SPI1_CS3 / GPIO26		PU
60	P0_03	SPI0_CS0 / SPT0_BCNV / SPI2_RDY / GPIO03		PU
61	P0_02	SPI0_MISO / SPT0_BD0 / GPIO02		PU
62	P0_01	SPI0_MOSI / SPT0_BFS / GPIO01		PU
63	P0_00	SPI0_CLK / SPT0_BCLK / GPIO00		PU
64		GND_ANA	Analog Ground	

[1] Silicon anomaly note: This pin is a no connect (NC) for revision 0.0 silicon.
[2] Silicon anomaly note: This pin must be connected to ground (GND) for revision 0.0 silicon.

Table 26. 54-Ball WLCSP Package Pin Assignments

Pin #	GPIO#	Pin Label
B1	P0_00	SPI0_CLK / SPT0_BCLK / GPIO00
C3	P0_01	SPI0_MOSI / SPT0_BFS / GPIO01
C5	P0_02	SPI0_MISO / SPT0_BD0 / GPIO02
C1	P0_03	SPI0_CS0 / SPT0_BCNV / SPI2_RDY / GPIO03
E9	P0_04	I2C0_SCL / GPIO04
D13	P0_05	I2C0_SDA / GPIO05
E13	P0_06	GPIO06 / SWD0_CLK
E11	P0_07	GPIO07 / SWD0_DATA
H8	P0_08	BPR0_TONE_N / GPIO08
H10	P0_08	BPR0_TONE_P / SPI2_CS1 / GPIO09
D1	P0_10	UART0_TX / GPIO10
D5	P0_11	UART0_RX / GPIO11
H12	P0_12	SPT0_AD0 / GPIO12/UART0_SOUT_EN
G5	P0_13	XINT0_WAKE2 / GPIO13
H4	P0_14	TMR0_OUT / SPI1_RDY / GPIO14
G3	P0_15	XINT0_WAKE0 / GPIO15
H2	P1_00	XINT0_WAKE1 / GPIO16
G7	P1_01	GPIO17 / SYS_BMODE0
E3	P1_02	SPI2_CLK / GPIO18

Table 26. 54-Ball WLCSP Package Pin Assignments (Continued)

Pin #	GPIO#	Pin Label
E1	P1_03	SPI2_MOSI / GPIO19
F6	P1_04	SPI2_MISO / GPIO20
F4	P1_05	SPI2_CS0 / GPIO21
G9	P1_06	SPI1_CLK / GPIO22
F12	P1_07	SPI1_MOSI / GPIO23
F10	P1_08	SPI1_MISO / GPIO24
F8	P1_09	SPI1_CS0 / GPIO25
D3	P1_10	SPI0_CS1 / SYS_CLKIN / SPI1_CS3 / GPIO26
H6	P1_14	SPI0_RDY / GPIO30
F2	P2_01	XINT0_WAKE3 / TMR2_OUT / GPIO33
D9	P2_04	ADC0_VIN1 / GPIO36
C13	P2_05	ADC0_VIN2 / GPIO37
D11	P2_06	ADC0_VIN3 / GPIO38
G11	P2_11	SPI1_CS1 / SYS_CLKOUT / GPIO43/RTC1_OPC1
E7		SYS_HWRST
A5		SYS_LFXTAL_IN
B5		SYS_LFXTAL_OUT
B3		SYS_HFXTAL_IN
A3		SYS_HFXTAL_OUT
B13	P2_03	ADC0_VIN0 / GPIO35
A1		VBAT_ANA1
C7		VBAT_ANA2
G1		VBAT_DIG2
G13		VBAT_DIG1
A13		VBAT_ADC
C9		VDCDC_OUT
A11		VLDO_OUT
D7		GND_ANA
E5		GND_DIG
A7		VDCDC_CAP1P
B7		VDCDC_CAP1N
B9		VDCDC_CAP2P
A9		VDCDC_CAP2N
B11		VREF_ADC
C11		GND_VREFADC

OUTLINE DIMENSIONS

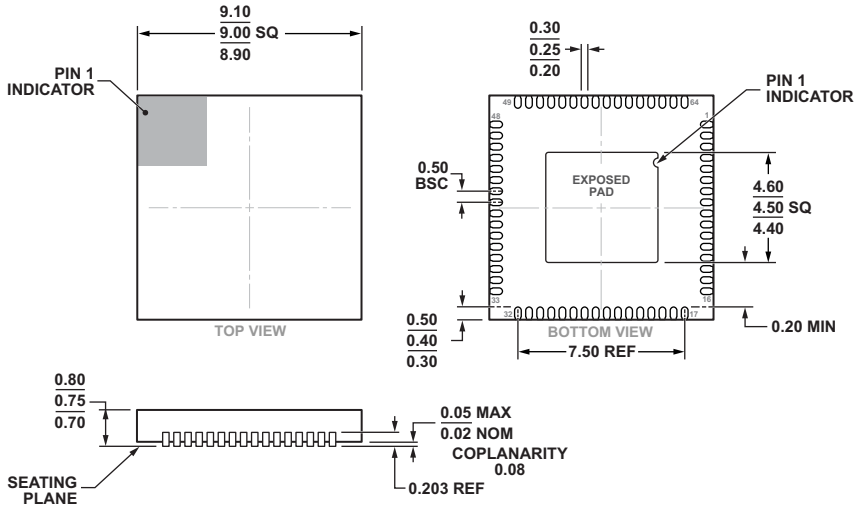


Figure 18. 64-Lead Frame Chip Scale Package [LFCSP_WQ]
9 x 9 mm Body, Very Thin Quad
(CP-64-16)
Dimensions shown in mm

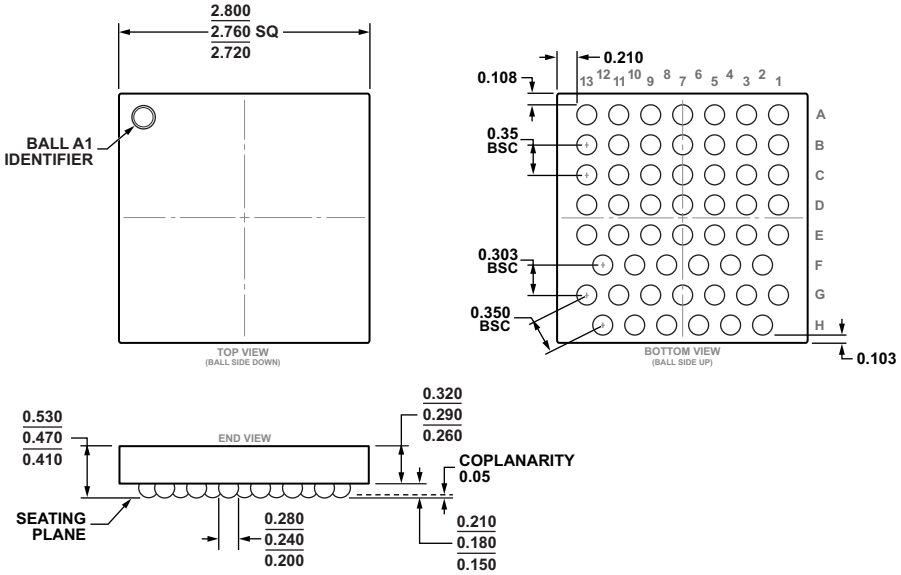


Figure 19. 54-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-54-1)
Dimensions shown in mm

FUTURE (PLANNED) PRODUCTS

Generic Part Number	SAP Part Number[1]	Description	Package (Code)	Temperature Range[2, 3]	Reel Info
ADuCM3027	ADUCM3027BCBZ	ULP ARM Cortex-M3 with128K Embedded Flash	54 WLCSP (CB-54-1)	−40°C to +85°C	Individual
	ADUCM3027BCBZ-RL				13″ Reel
	ADUCM3027BCBZ-R7				7″ Reel
	ADUCM3027BCPZ	ULP ARM Cortex-M3 with128K Embedded Flash	64 LFCSP (CP-64-16)	−40°C to +85°C	Individual
	ADUCM3027BCPZ-RL				13″ Reel
	ADUCM3027BCPZ-R7				7″ Reel
ADuCM3029	ADUCM3029BCBZ	ULP ARM Cortex-M3 with 256K Embedded Flash	54 WLCSP (CB-54-1)	−40°C to +85°C	Individual
	ADUCM3029BCBZ-RL				13″ Reel
	ADUCM3029BCBZ-R7				7″ Reel
	ADUCM3029BCPZ	ULP ARM Cortex-M3 with 256K Embedded Flash	64 LFCSP (CP-64-16)	−40°C to +85°C	Individual
	ADUCM3029BCPZ-RL				13″ Reel
	ADUCM3029BCPZ-R7				7″ Reel

[1] Z =RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See Operating Conditions on Page 12 for the junction temperature (T_J) specification which is the only temperature specification.

[3] These are pre-production parts. See ENG-Grade agreement for details.

PR14168-0-2/16(PrF)