TLV3502-Q1, 4.5-ns Rail-to-Rail High-Speed Comparator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- High Speed: 4.5 ns
- Rail-To-Rail I/O
- Supply Voltage: 2.7 V To 5.5 V
- Push-Pull CMOS Output Stage
- Shutdown
- Micro Package: SOT23-8
- Low Supply Current: 3.2 mA

2 Applications

- HEV/EV, Powertrain, and Passive Safety:
  - Threshold Detector
  - Zero-Crossing Detector
  - Window Comparator
  - Oscillator

3 Description

The TLV3502-Q1 push-pull output comparators feature a fast 4.5-ns propagation delay and operation from 2.7 V to 5.5 V. Beyond-the-rails input common-mode range makes the device an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

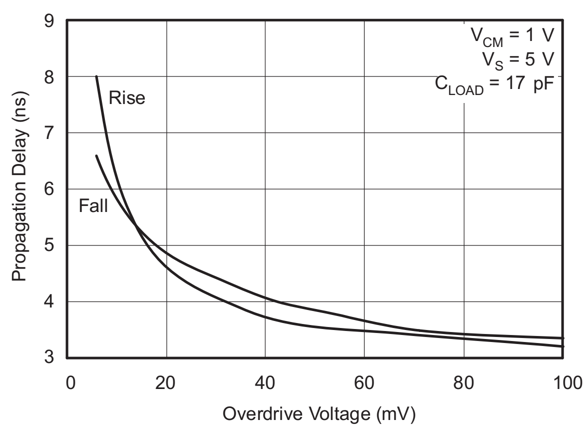
A microsize package provides options for portable and space-restricted applications. The TLV3502-Q1 device is available in the SOT23-8 (DCN) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV3502-Q1	SOT-23 (8)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Propagation Delay vs Overdrive Voltage



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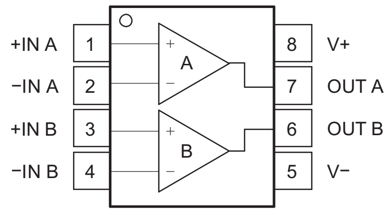
4 Revision History

Changes from Original (February 2010) to Revision A — **Page**

- Deleted references to the TLV3501 device and changed the TLV3502 device name to TLV3502-Q1 1
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4

5 Pin Configuration and Functions

8-Pin SOT-23
DCN Package
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	+IN A	I	Non inverting input, channel A
2	–IN A	I	Inverting input, channel A
3	+IN B	I	Non inverting input, channel B
4	–IN B	I	Inverting input, channel B
5	V–	Supply	Negative (lowest) power supply
6	OUT B	O	Output, channel B
7	OUT A	O	Output, channel A
8	V+	Supply	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage		5.5	V
Signal input terminal voltage (2)	(V−) − 0.3	(V+) + 0.3	V
Signal input terminal current (2)		10	mA
Output short-circuit current (3)		74	mA
Thermal impedance, junction to free air	200	200	°C/W
Operating temperature	−40	125	°C
Junction temperature		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10mA or less.
(3) Short circuit to ground, one comparator per package

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (+IN A, –IN B, V+, and V–)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	2.2	2.7	5.5	V
V_{IL}	Low-level input voltage, shutdown (comparator is enabled) (1)			(V+) - 1.7	V
V_{IH}	High-level input voltage, shutdown (comparator is disabled) (1)	(V+) – 0.9			V
T_A	Operating temperature	–40		125	°C

(1) When the shutdown pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

6.4 Thermal Information

THERMAL METRIC (1)		TLV3502-Q1 SOT-23 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	191.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	120.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	118.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C and V_S = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage (1)	V_{CM} = 0 V, I_O = 0 mA		±1	±6.5	mV
$\Delta V_{OS}/\Delta T$	Offset voltage vs temperature	T_A = –40°C to 125°C		±5		µV/°C
PSRR	Offset voltage vs power supply	V_S = 2.7 V to 5.5 V		100	400	µV/V
	Input hysteresis			6		mV
I_B	Input bias current	V_{CM} = V_{CC}/2, ΔV_{IN} = ±5.5 V		±2	±10	pA
I_{OS}	Input offset current (2)	V_{CM} = V_{CC}/2, ΔV_{IN} = ±5.5 V		±2	±10	pA
V_{CM}	Common-mode voltage range		(V–) - 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection	V_{CM} = –0.2 V to (V+) + 0.2 V	57	70		dB
		T_A = −40°C to 125°C V_{CM} = –0.2 V to (V+) + 0.2 V	55			
	Common-mode input impedance			10^{13} || 2		Ω || pF
	Differential input impedance			10^{13} || 4		Ω || pF
V_{OH}	High-level voltage output from rail	I_{OUT} = ±1 mA		30	50	mV
V_{OL}	Low-level voltage output from rail	I_{OUT} = ±1 mA		30	50	mV
	Input bias current of shutdown pin			2		pA
I_Q	Quiescent current per comparator	V_S = 5 V, V_O = High		3.2	5	mA
$I_{Q(SD)}$	Quiescent current in shutdown			2		µA

(1) V_{OS} is defined as the average of the positive and the negative switching thresholds.
(2) The difference between I_{B+} and I_{B-}.

6.6 Switching Characteristics

T_A = 25°C and V_S = 2.7 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time (1)(2)	ΔV_{IN} = 100 mV, Overdrive = 20 mV		4.5	6.4	ns
		T_A = −40°C to 125°C ΔV_{IN} = 100 mV, Overdrive = 20 mV			7	ns
		ΔV_{IN} = 100 mV, Overdrive = 5 mV		7.5	10	ns
		T_A = −40°C to 125°C ΔV_{IN} = 100 mV, Overdrive = 5 mV			12	ns
$\Delta t_{(SKEW)}$	Propagation delay skew (3)	ΔV_{IN} = 100 mV, Overdrive = 20 mV		0.5		ns
f_{MAX}	Maximum toggle frequency	Overdrive = 50 mV, V_S = 5 V		80		MHz
t_R	Rise time (4)			1.5		ns
t_F	Fall time (4)			1.5		ns
t_{OFF}	Shutdown turn-off time			30		ns
t_{ON}	Shutdown turn-on time			100		ns

(1) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization at 100-mV overdrive.
(2) Not production tested
(3) The difference between the propagation delay going high and the propagation delay going low.
(4) Measured between 10% of V_S and 90% of V_S.

6.7 Typical Characteristics

T_A = 25°C, V_S = 5 V, Input Overdrive = 100 mV (unless otherwise noted)

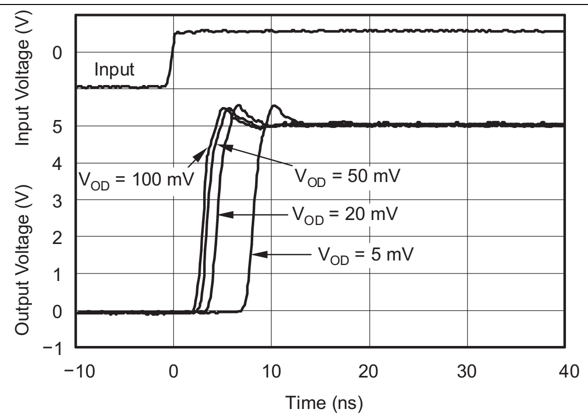


Figure 1. Output Response for Various Overdrive Voltages (rising)

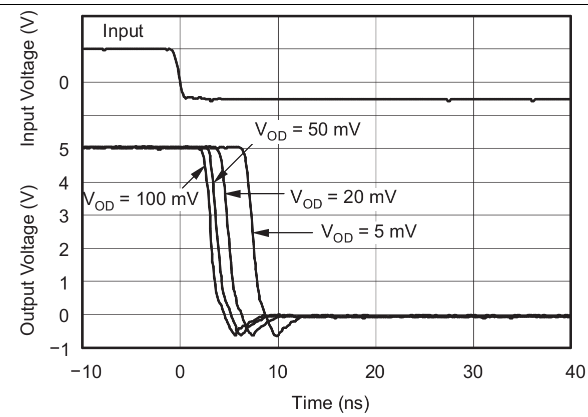


Figure 2. Output Response for Various Overdrive Voltages (falling)

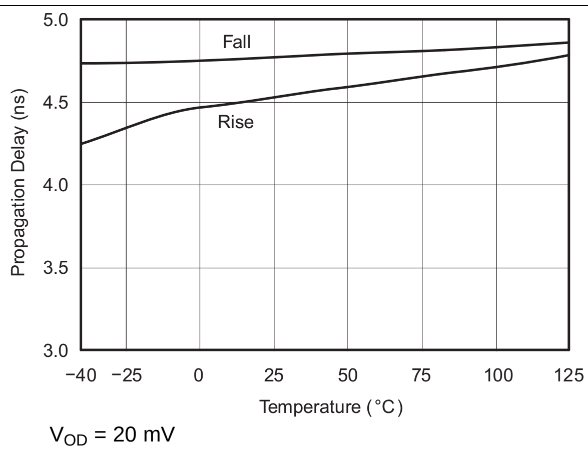


Figure 3. Propagation Delay vs Temperature

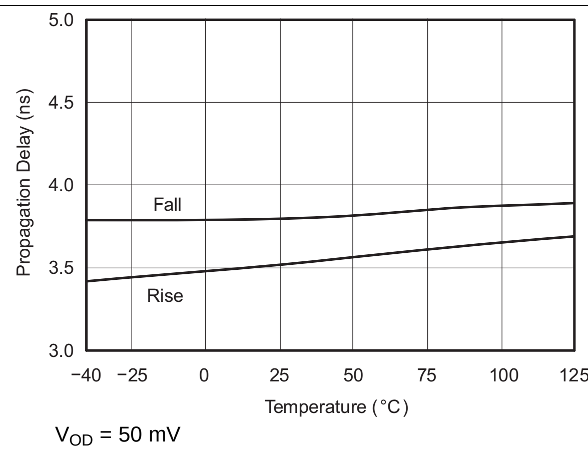


Figure 4. Propagation Delay vs Temperature

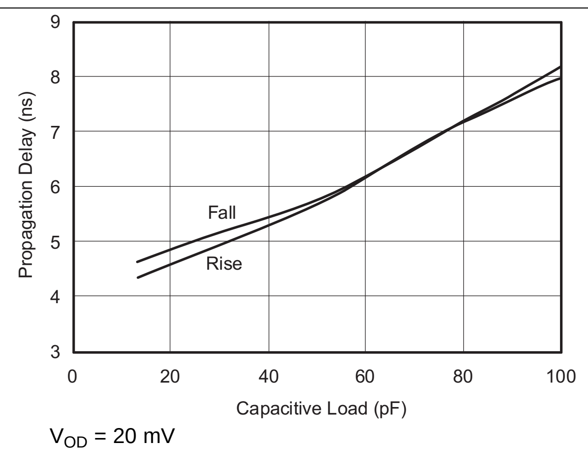


Figure 5. Propagation Delay vs Capacitive Load

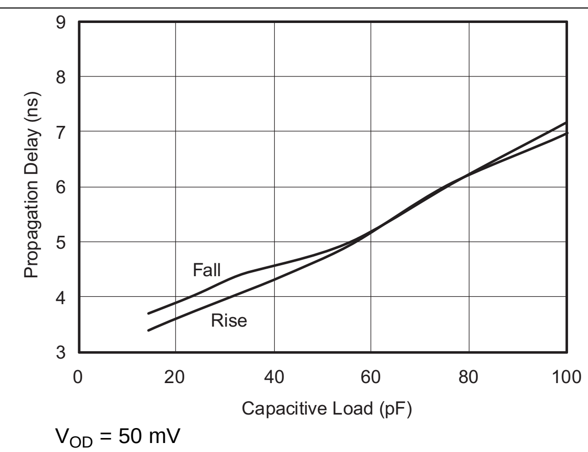
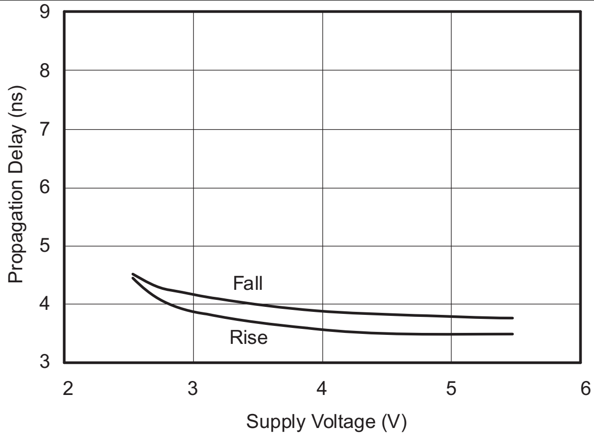


Figure 6. Propagation Delay vs Capacitive Load

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, Input Overdrive = 100 mV (unless otherwise noted)



V_{DD} = 5 V V_{IN} = 20 mV_{pp}

Figure 7. Propagation Delay vs Supply Voltage

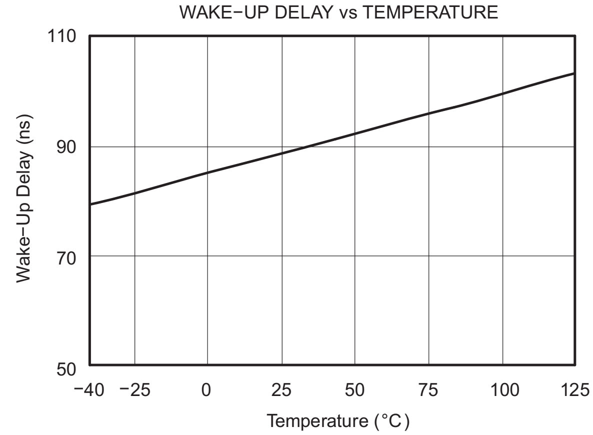
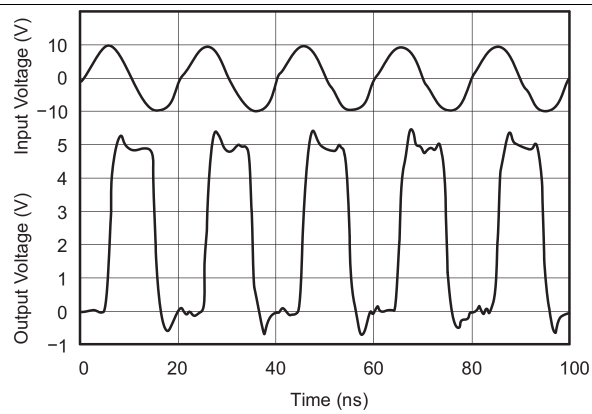
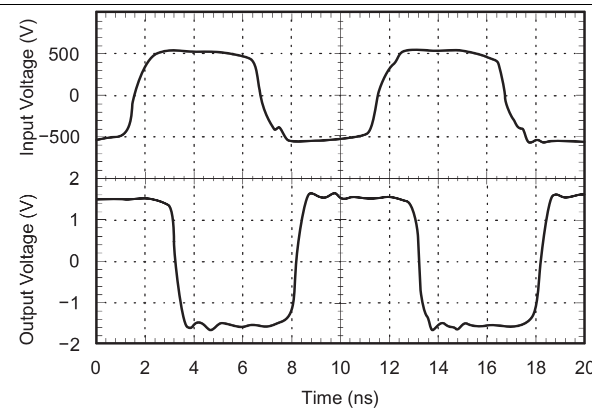


Figure 8. Wake-Up Delay vs Temperature



V_{DD} = 5 V V_{IN} = 20 mV_{pp}

Figure 9. Response to 50-MHz Sine Wave



±2.5-V dual supply into 50-Ω oscilloscope input

Figure 10. Response to 100 MHz Sine Wave

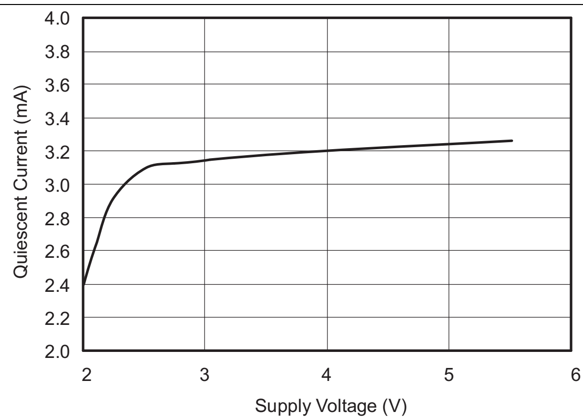


Figure 11. Quiescent Current vs Supply Voltage

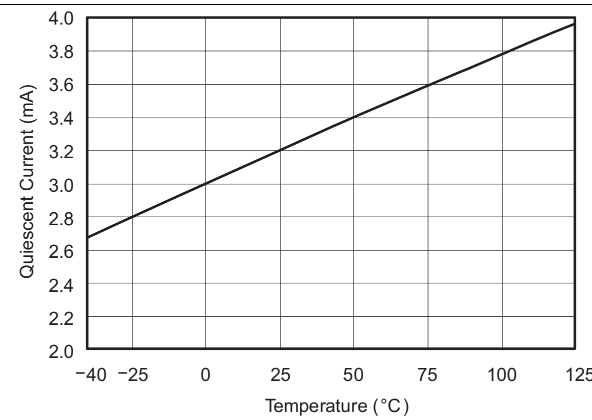


Figure 12. Quiescent Current vs Temperature

Typical Characteristics (continued)

T_A = 25°C, V_S = 5 V, Input Overdrive = 100 mV (unless otherwise noted)

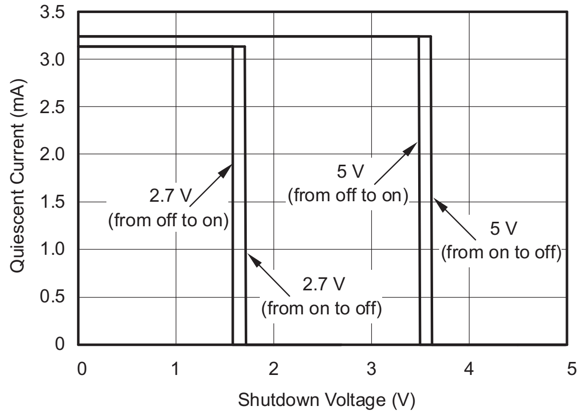


Figure 13. Quiescent Current vs Shutdown Voltage

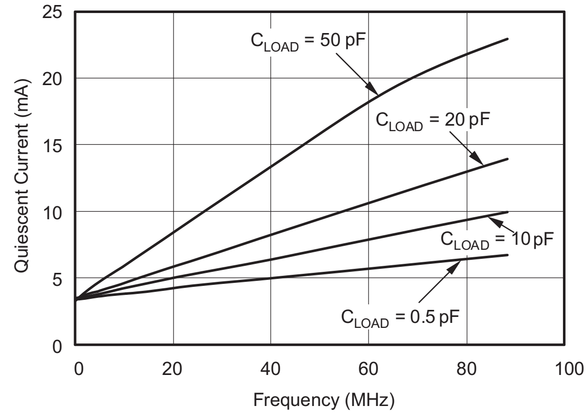


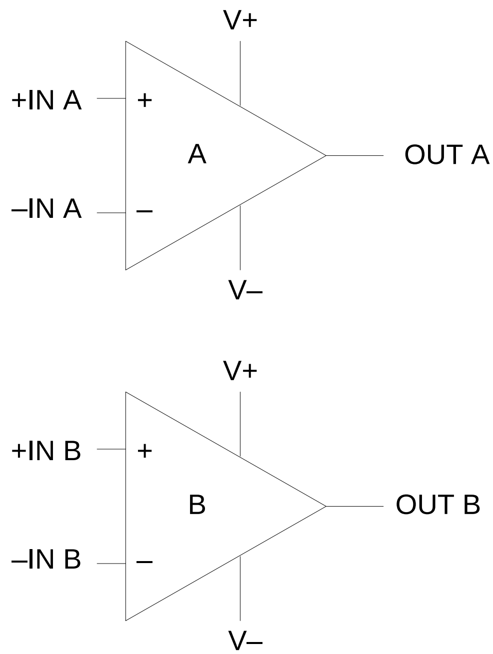
Figure 14. Quiescent Current vs Frequency

7 Detailed Description

7.1 Overview

The TLV3502-Q1 push-pull output comparator features a fast 4.5-ns propagation delay and operation from 2.7 V to 5.5 V. Beyond-the-rails input common-mode range makes it an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic.

7.2 Functional Block Diagram



7.3 Feature Description

The TLV3502-Q1 device feature fast 4.5-ns propagation delay with a push-pull output. The device operates from 2.7 V to 5.5 V. It has beyond-the-rails input common-mode range and rail-to-rail output directly drives either CMOS or TTL logic.

7.3.1 Input Over-Voltage Protection

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in Figure 15.

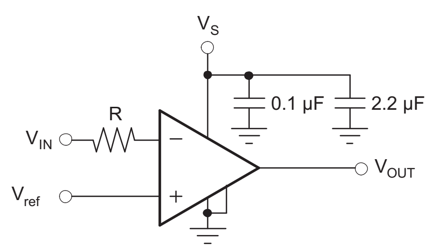


Figure 15. Input Current Protection for Voltages Exceeding the Supply Voltage

Feature Description (continued)

7.3.2 Relaxation Oscillator

The TLV350x can easily be configured as a simple and inexpensive relaxation oscillator. In Figure 16, the R2 network sets the trip threshold at 1/3 and 2/3 of the supply. Since this is a high-speed circuit, the resistor values are rather low to minimize the effect of parasitic capacitance. The positive input alternates between 1/3 of V+ and 2/3 of V+ depending on whether the output is low or high. The time to charge (or discharge) is $0.69R_1C$. Therefore, the period is $1.38R_1C$. For 62 pF and 1 kΩ as shown in Figure 16, the output is calculated to be 10.9MHz. An implementation of this circuit oscillated at 9.6 MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

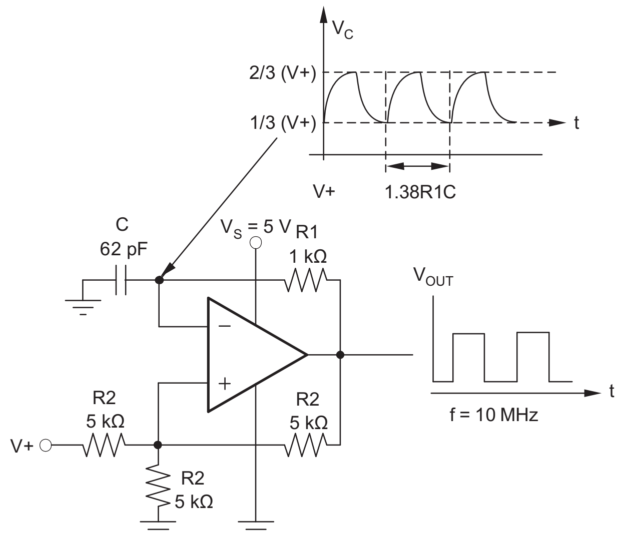


Figure 16. Relaxation Oscillator

7.3.3 High-Speed Window Comparator

A window comparator circuit is used to determine when a signal is between two voltages. The TLV3502-Q1 device can readily be used to create a high-speed window comparator. V_{HI} is the upper voltage threshold, and V_{LO} is the lower voltage threshold. When V_{IN} is between these two thresholds, the output in Figure 17 is high. Figure 18 shows a simple means of obtaining an active low output. Note that the reference levels are connected differently between Figure 17 and Figure 18. The operating voltage range of either circuit is 2.7 V to 5.5 V.

Feature Description (continued)

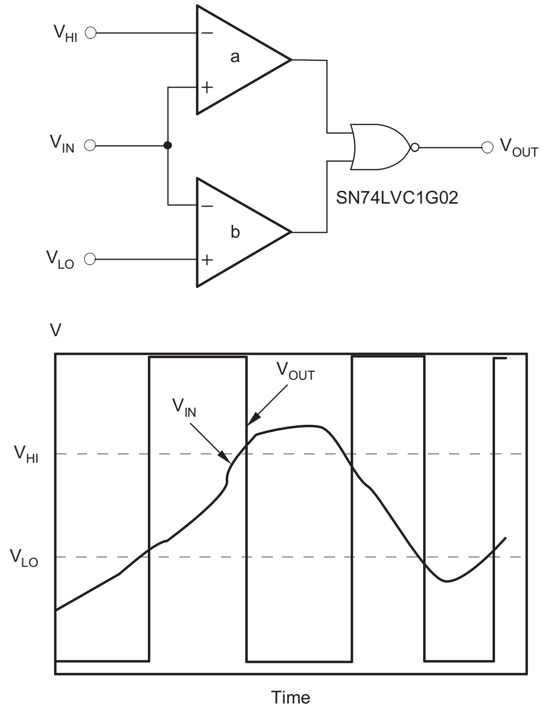


Figure 17. Window Comparator—Active High

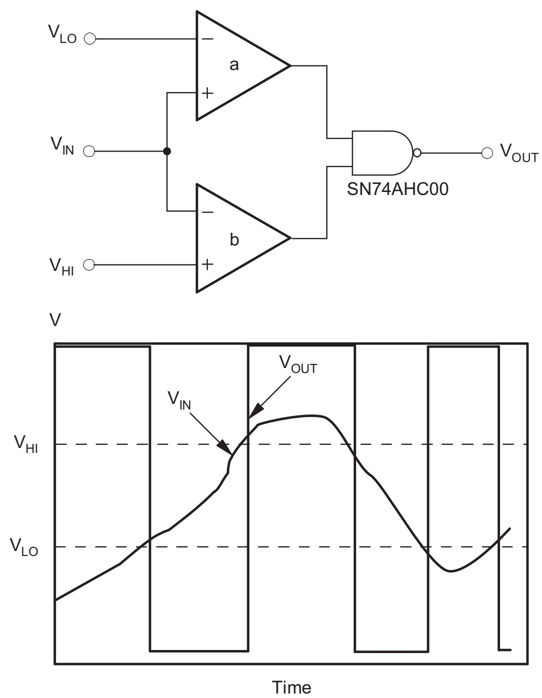


Figure 18. Window Comparator—Active Low

7.4 Device Functional Modes

This device has no special operating modes outside of the normally powered dual comparator function.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV3502-Q1 device features high-speed response and includes 6 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

8.2 Typical Application

In this example, we will show how can we add external hysteresis to TLV3502-Q1 device to achieve greater noise immunity. First, let's understand when and why external hysteresis may be required.

The TLV3502-Q1 device has a robust performance when used with a good layout. However, comparator inputs have little noise immunity within the range of specified offset voltage (±5 mV). For slow moving or noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. In such applications, the 6mV of internal hysteresis of the TLV3502-Q1 device might not be sufficient. In cases where greater noise immunity is desired, external hysteresis may be added by connecting a small amount of feedback to the positive input.

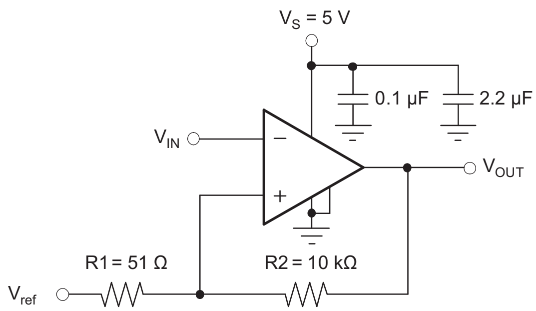


Figure 19. Application Adding Hysteresis to the TLV350x

8.2.1 Design Requirements

Figure 19 shows a typical topology used to introduce 25 mV of additional hysteresis, for a total of 31-mV hysteresis when operating from a single 5-V supply.

8.2.2 Detailed Design Procedure

Use Equation 1 to calculate the total hysteresis.

$$V_{HYST} = \frac{(V+) \times R1}{R1 + R2} + 6\text{ mV} \quad (1)$$

V_{HYST} sets the value of the transition voltage required to switch the comparator output by enlarging the threshold region, thereby reducing sensitivity to noise.

Typical Application (continued)

8.2.3 Application Curve

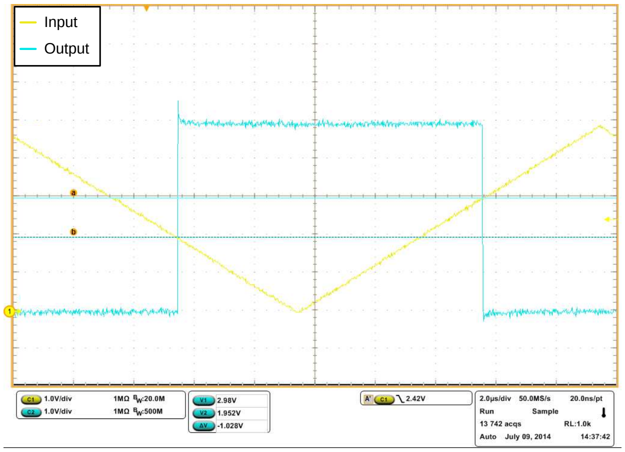


Figure 20. TLV3502 With Upper and Lower Threshold With 1-V Hysteresis

9 Power Supply Recommendations

The TLV3505-Q1 comparator is specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified.

Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

- For any high-speed comparator or amplifier, proper design and printed circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.
- Minimizing resistance from the signal source to the comparator input is necessary in order to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV3502-Q1 device along with stray capacitance from an input pin to ground results in several picofarads of capacitance.
- The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2-μF tantalum capacitor do not need to be as close to the device as the 0.1-μF capacitor, and may be shared with other devices. The 2.2-μF capacitor buffers the power-supply line against ripple, and the 0.1-μF capacitor provides a charge for the comparator during high frequency switching.
- In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow right under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.
- Figure 21 shows an evaluation layout for the TLV3502-Q1 SOT23-8 package. The device is shown with SMA connectors bringing signals on and off the board. RT1, RT2, RT3 and RT4 are termination resistors for + IN A, + IN B, –IN A, and –IN B respectively. C1 and C2 are power-supply bypass capacitors. Place the 0.1-μF capacitor closest to the comparator. The ground plane is not shown, but the pads that the resistors and capacitors connect to are shown. Figure 22 shows a schematic of this circuit.

10.2 Layout Example

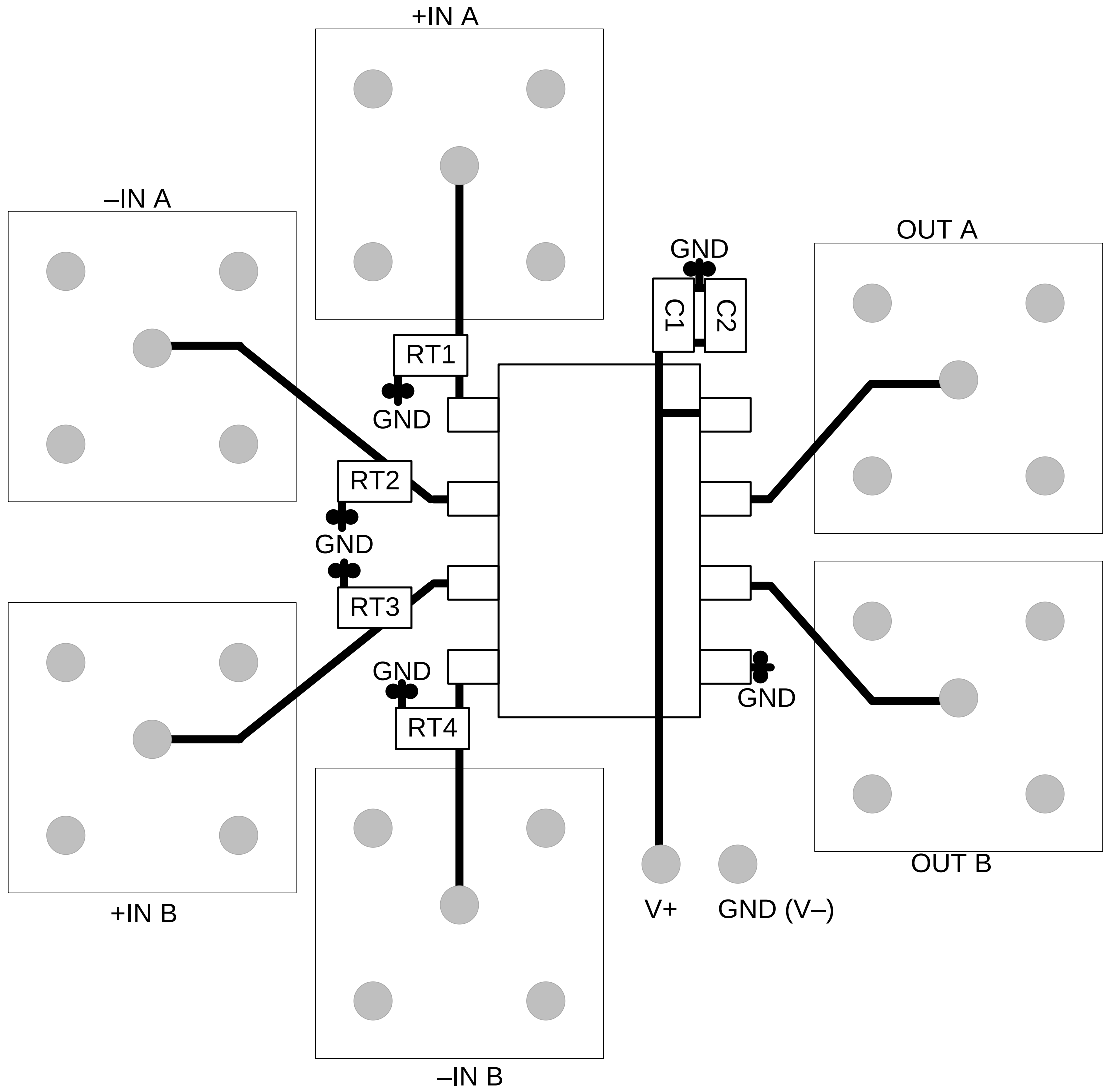


Figure 21. TLV3502-Q1 Sample Layout

Layout Example (continued)

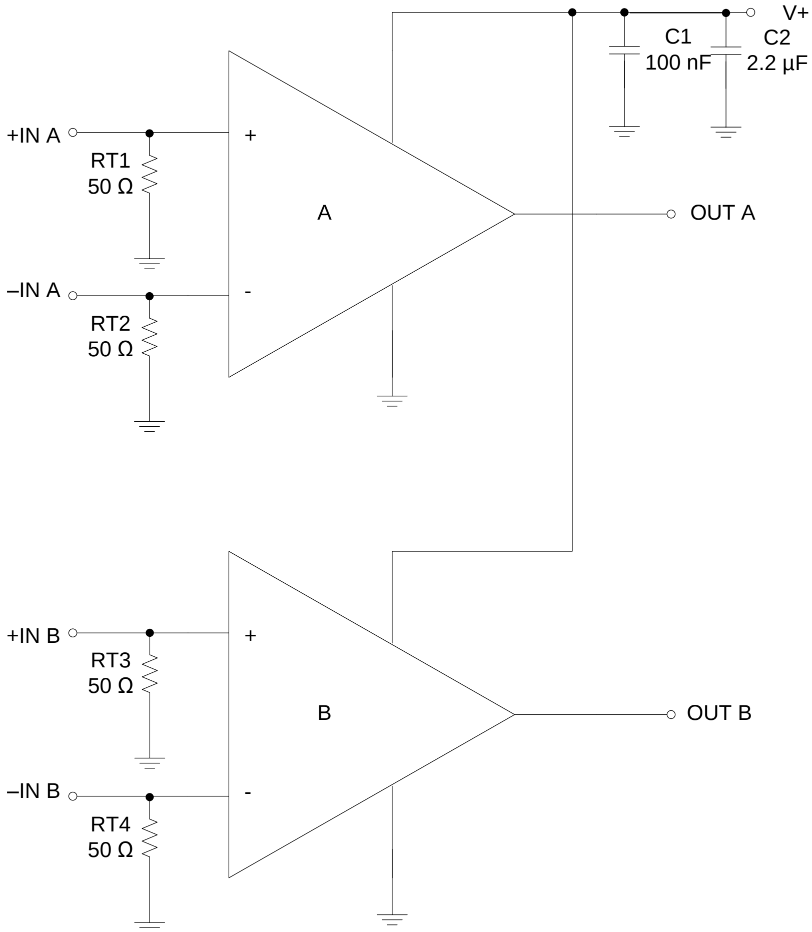


Figure 22. Schematic for Figure 21

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3502AQDCNRQ1	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	3502	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3502-Q1 :

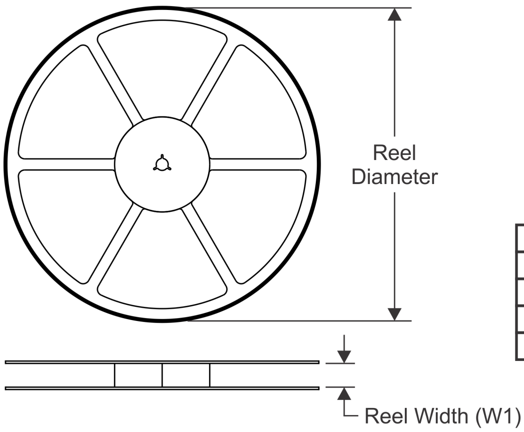
- Catalog: TLV3502

NOTE: Qualified Version Definitions:

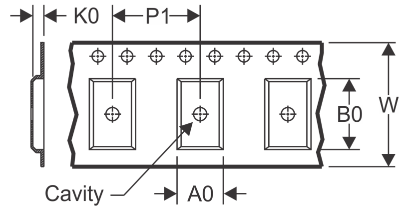
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

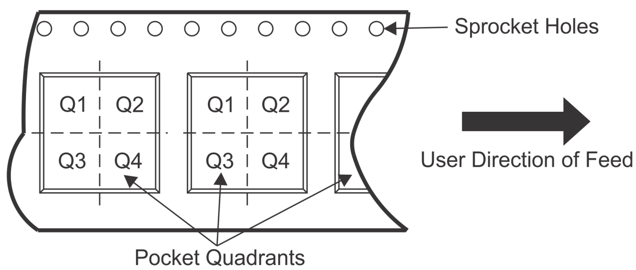


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

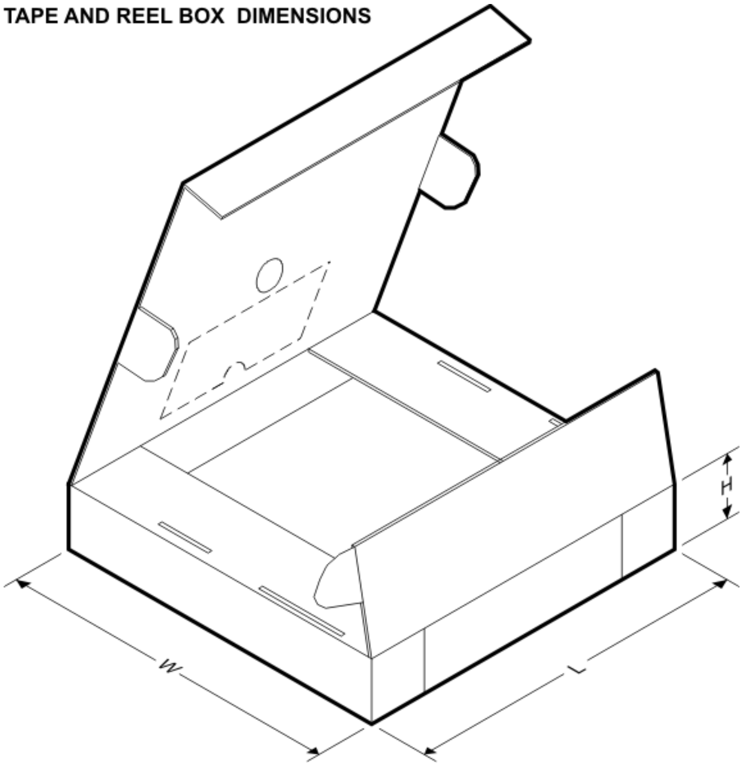
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3502AQDCNRQ1	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

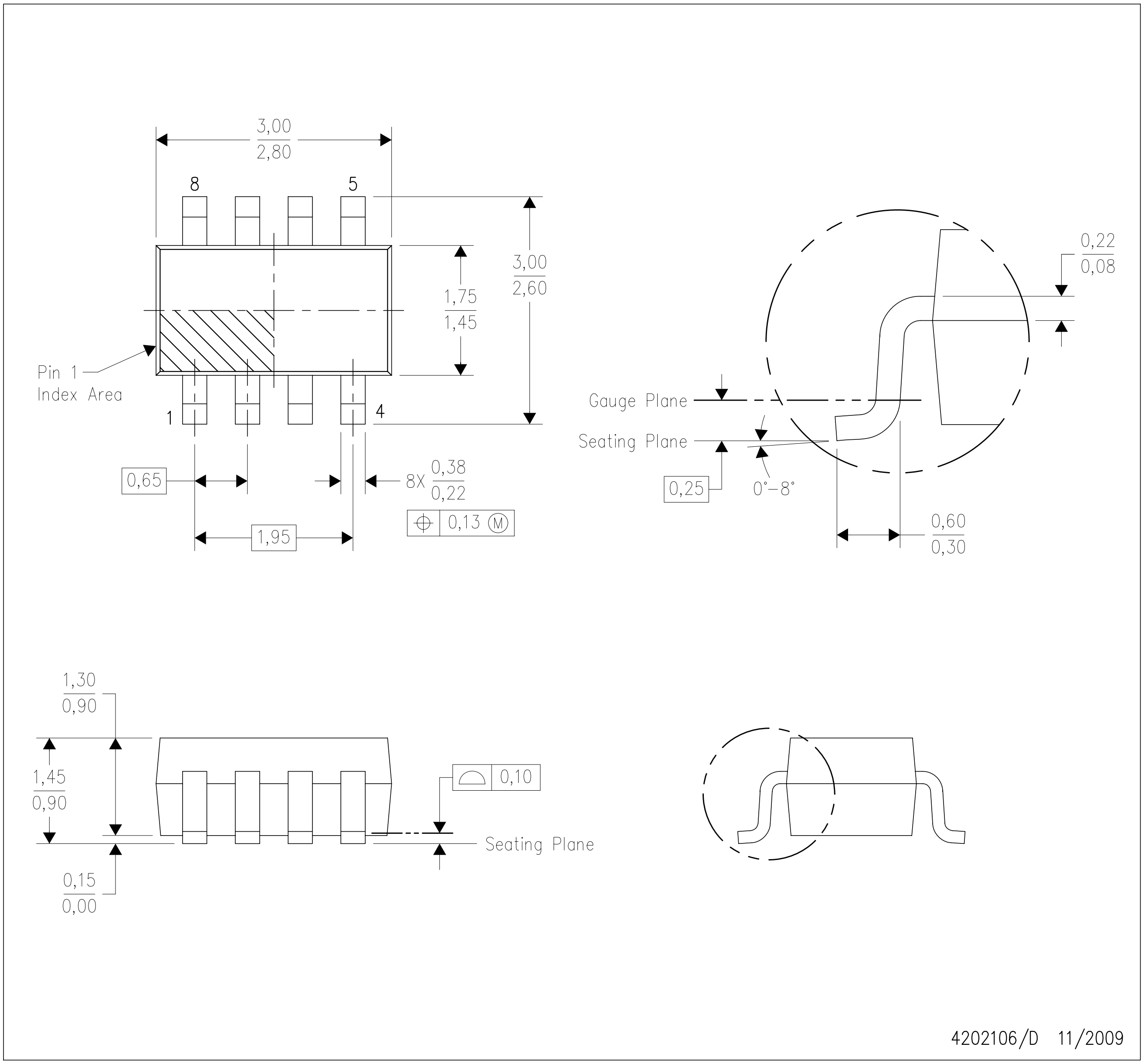
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

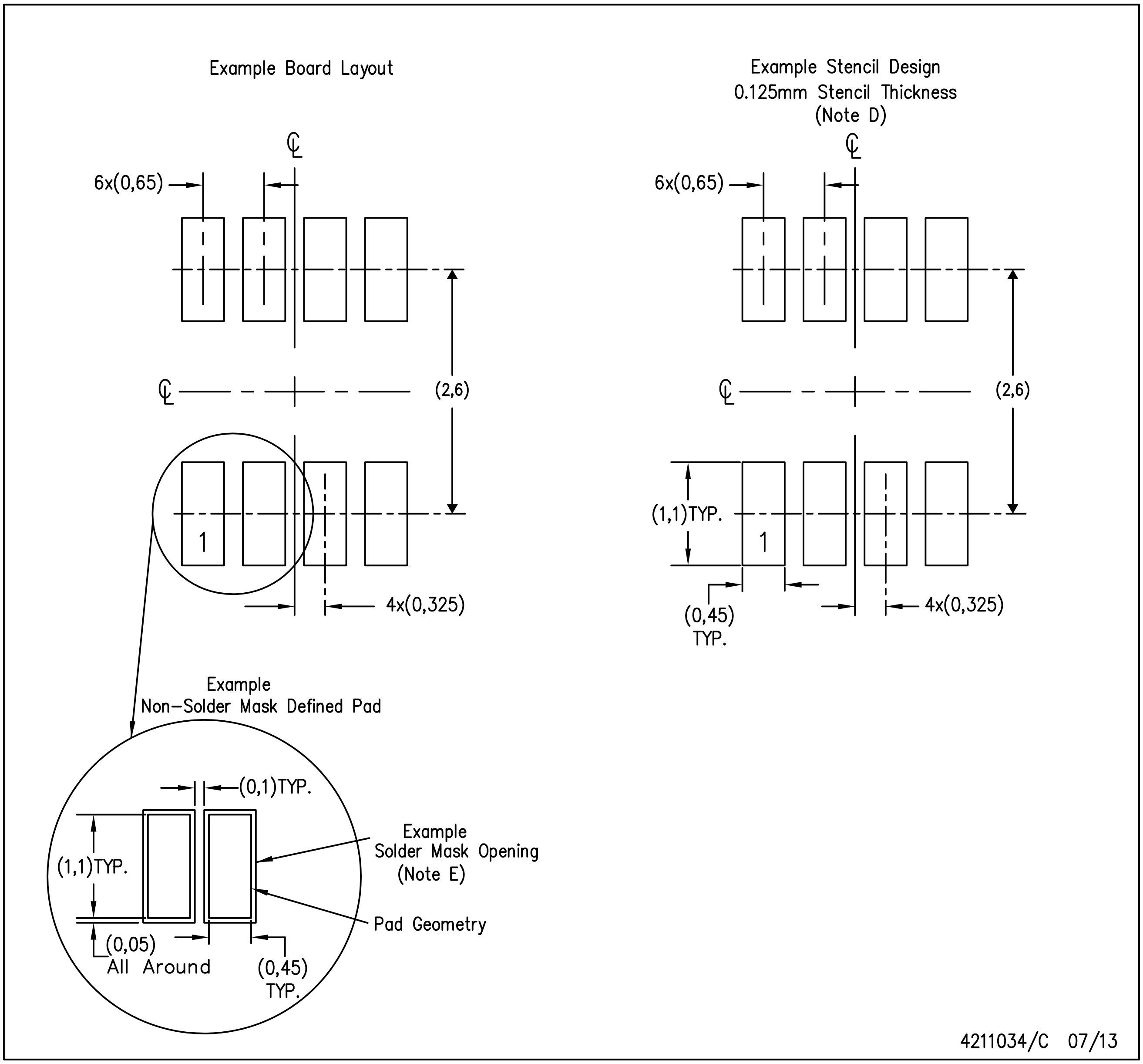
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3502AQDCNRQ1	SOT-23	DCN	8	3000	195.0	200.0	45.0

DCN (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
D. Package outline inclusive of solder plating.
E. A visual index feature must be located within the Pin 1 index area.
F. Falls within JEDEC MO-178 Variation BA.
G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.