1.8V to 3.3V LVCMOS High Performance Clock Buffer Family

5PB11xx

DATASHEET

Description

The 5PB11xx is a high-performance LVCMOS Clock Buffer Family. It has best-in-class Additive Phase Jitter of 50fsec RMS.

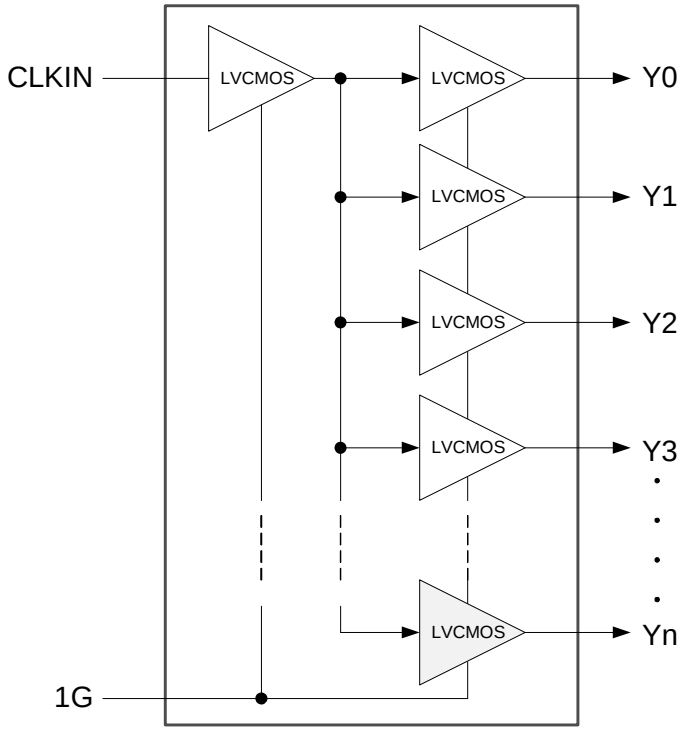
There are five different fan-out variations, 1:2 to 1:10, available.

The IDT5PB11xx also supports a synchronous glitch-free Output Enable function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It comes in various packages and can operate from a 1.8V to 3.3V supply.

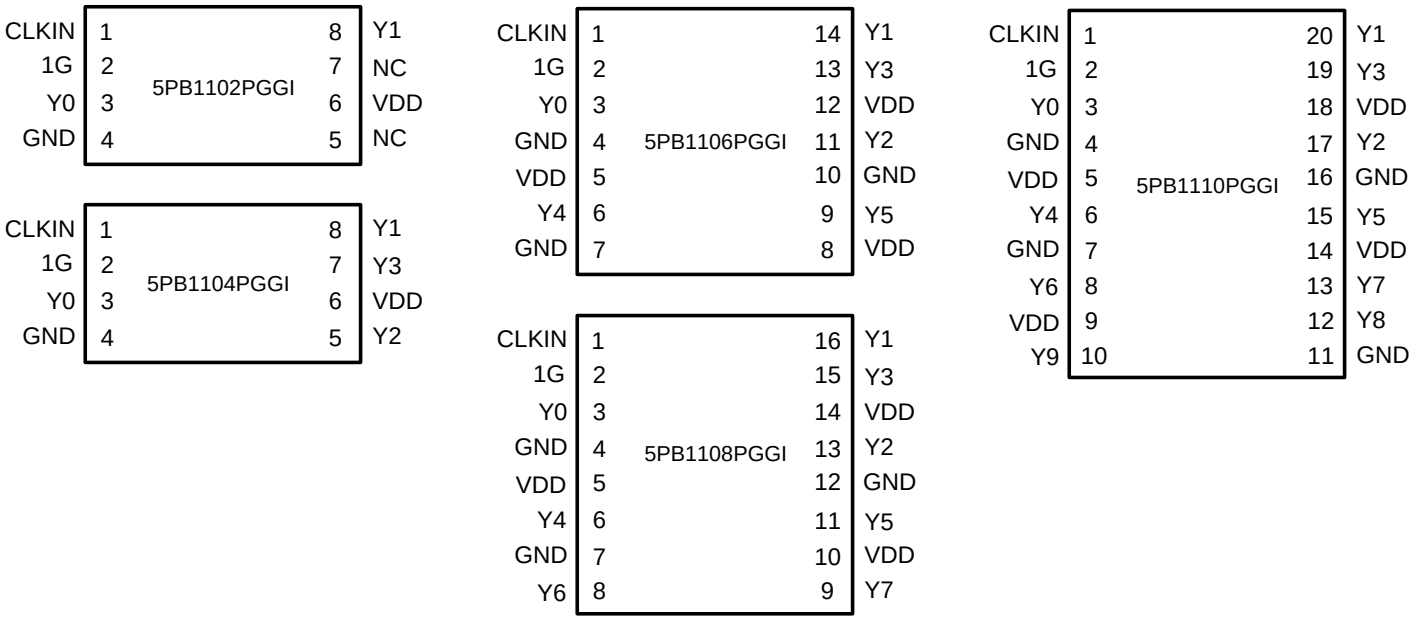
Features

- High performance 1:2, 1:4, 1:6, 1:8, 1:10 LVCMOS clock buffer
- Very low pin-to-pin skew <50ps
- Very low additive jitter <50fs
- Supply voltage: 1.8V to 3.3V
- f_{MAX} = 200MHz
- Integrated serial termination for 50ohm channel
- Packaged in 8-, 14-, 16-, 20-pin TSSOP and small DFN and QFN packages
- Extended (-40°C to +105°C) temperature range

Block Diagram



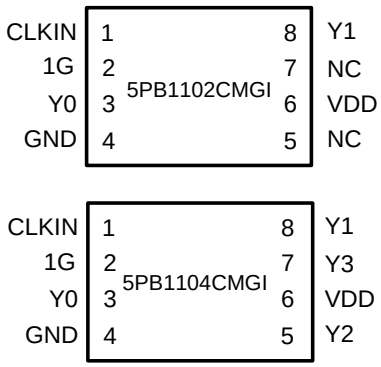
Pin Assignments for TSSOP Packages

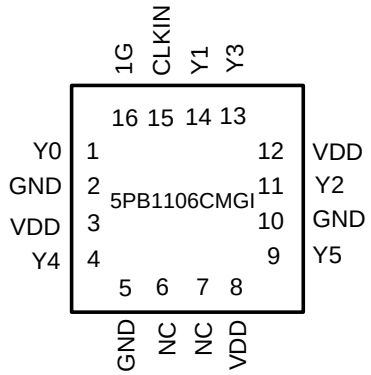


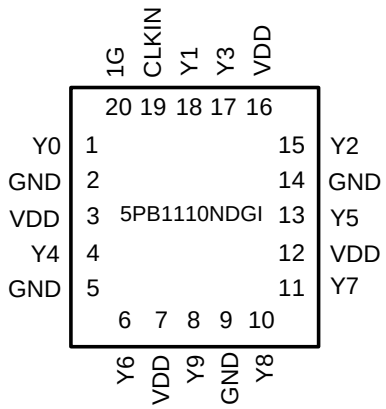
Pin Descriptions for TSSOP Packages

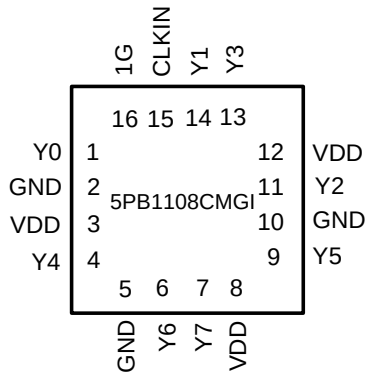
Device Number	LVCMOS Clock Input	Clock Output Enable	LVCMOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, . . . Y9	V_{DD}	GND
5PB1102PGGI	1	2	3, 8	6	4
5PB1104PGGI	1	2	3, 8, 5, 7	6	4
5PB1106PGGI	1	2	3, 14, 11, 13, 6, 9	5, 8, 12	4, 7, 10
5PB1108PGGI	1	2	3, 16, 13, 15, 6, 11, 8, 9	5, 10, 14	4, 7, 12
5PB1110PGGI	1	2	3, 20, 17, 19, 6, 15, 8, 13, 12, 10	5, 9, 14, 18	4, 7, 11, 16

Pin Assignments for DFN/QFN Packages









Pin Descriptions for DFN/QFN Packages

Device Number	LVCMOS Clock Input	Clock Output Enable	LVCMOS Clock Output	Supply Voltage	Ground
	CLKIN	1G	Y0, Y1, . . . Y9	V_{DD}	GND
5PB1102CMGI	1	2	3, 8	6	4
5PB1104CMGI	1	2	3, 5, 7, 8	6	4
5PB1106CMGI	15	16	1, 4, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1108CMGI	15	16	1, 4, 6, 7, 9, 11, 13, 14	3, 8, 12	2, 5, 10
5PB1110NDGI	19	20	1, 4, 6, 8, 10, 11, 13, 15, 17, 18	3, 7, 12, 16	2, 5, 9, 14

Output Logic Table

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

After at least three cycles of input clock toggling. Output Enable function is asynchronous to eliminate any intermediate incorrect output clock cycles during transition which may cause frequency peaking to the downstream device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5PB11xx. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	3.465V
Output Enable and All Outputs	-0.5 V to VDD+0.5 V
CLKIN	3.465V
Ambient Operating Temperature (extended)	-40 to +105°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (extended)	-40		+105	°C
Power Supply Voltage (measured in respect to GND)	+1.71		+3.465	V

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD=1.8V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		1.71		1.89	V
Input High Voltage, CLKIN	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, CLKIN	V_{IL}	Note 1			0.3xVDD	V
Input High Voltage, 1G	V_{IH}		1.6		VDD	V
Input Low Voltage, 1G	V_{IL}				0.6	V
Output High Voltage	V_{OH}	I_{OH} = -5 mA	1.4			V
Output Low Voltage	V_{OL}	I_{OL} = 5 mA			0.4	V
Nominal Output Impedance	Z_O			50		Ω
Input Capacitance	C_{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		8		mA
5PB1104		100MHz, No load, 25°C		12		
5PB1105		100MHz, No load, 25°C		16		
5PB1102		100MHz, No load, 25°C		21		
5PB1110		100MHz, No load, 25°C		25		

Notes: 1. Nominal switching threshold is VDD/2

VDD=2.5 V ±5%, Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Input High Voltage, CLKIN	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, CLKIN	V_{IL}	Note 1			0.3xVDD	V
Input High Voltage, 1G	V_{IH}		1.8		VDD	V
Input Low Voltage, 1G	V_{IL}				0.7	V
Output High Voltage	V_{OH}	I_{OH} = -8 mA	1.9			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.5	V
Nominal Output Impedance	Z_O			50		Ω
Input Capacitance	C_{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		10		mA
5PB1104		100MHz, No load, 25°C		15		
5PB1105		100MHz, No load, 25°C		22		
5PB1102		100MHz, No load, 25°C		28		
5PB1110		100MHz, No load, 25°C		33		

VDD=3.3 V ±5% , Ambient temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15		3.45	V
Input High Voltage, CLKIN	V_{IH}	Note 1	0.7xVDD		VDD	V
Input Low Voltage, CLKIN	V_{IL}	Note 1			0.3xVDD	V
Input High Voltage, 1G	V_{IH}		2		VDD	V
Input Low Voltage, 1G	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.7	V
Nominal Output Impedance	Z_O			50		Ω
Input Capacitance	C_{IN}	CLKIN, 1G pin		5		pF
Operating Supply Current						
5PB1102	IDD	100MHz, No load, 25°C		12		mA
5PB1104		100MHz, No load, 25°C		20		
5PB1105		100MHz, No load, 25°C		25		
5PB1102		100MHz, No load, 25°C		35		
5PB1110		100MHz, No load, 25°C		40		

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.36 to 1.44 V, C_L=5 pF		0.8	1.0	ns
Output Fall Time	t_{OF}	1.44 to 0.36 V, C_L=5 pF		0.8	1.0	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1		1.9	2.2	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04/06)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq 5$ pF			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq 5$ pF			3	cycles

VDD = 2.5 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.5 to 2.0 V, C_L=5 pF		0.75	1.0	ns
Output Fall Time	t_{OF}	2.0 to 0.5 V, C_L=5 pF		0.75	1.0	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1		2.4	2.9	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04/06)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq 5$ pF			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq 5$ pF			3	cycles

VDD = 3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency			0		200	MHz
Output Rise Time	t_{OR}	0.66 to 2.64 V, C_L=5 pF		0.7	1.0	ns
Output Fall Time	t_{OF}	2.64 to 0.66 V, C_L=5 pF		0.7	1.0	ns
Start-up Time	$t_{START-UP}$	Part start-up time for valid outputs after VDD ramp-up			3	ms
Propagation Delay		Note 1		2	2.4	ns
Buffer Additive Phase Jitter, RMS		156.25MHz, Integration Range: 12kHz-20MHz			0.05	ps
Output to Output Skew (5PB1102/04/06)		Rising edges at VDD/2, Note 2		35	50	ps
Output to Output Skew (5PB1108/10)		Rising edges at VDD/2, Note 2		45	65	ps
Device to Device Skew		Rising edges at VDD/2			200	ps
Output Enable Time	t_{EN}	$C_L \leq 5$ pF			3	cycles
Output Disable Time	t_{DIS}	$C_L \leq 5$ pF			3	cycles

Notes:
1. With rail to rail input clock
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

Phase Noise Plots

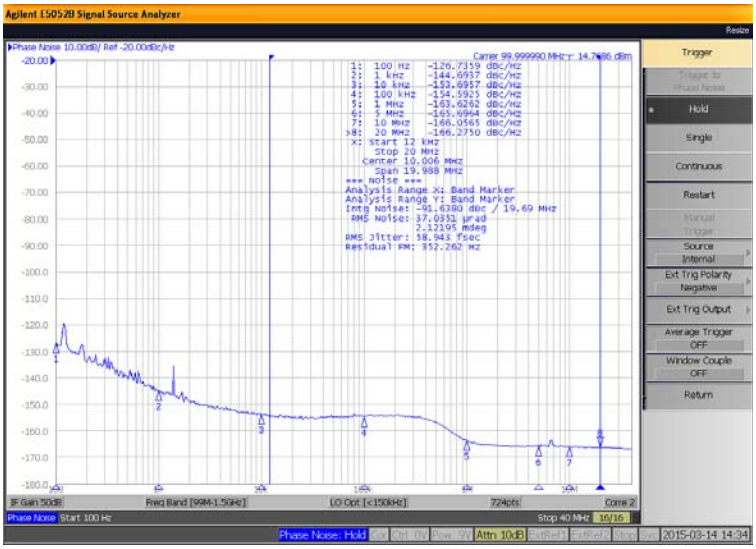


Figure 1. 5PB11xx Reference Phase Noise 58.9fs (12kHz to 20MHz)

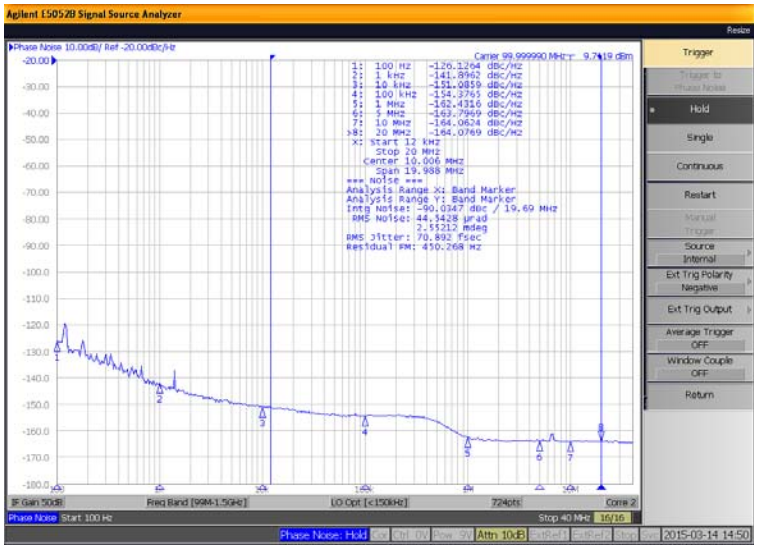
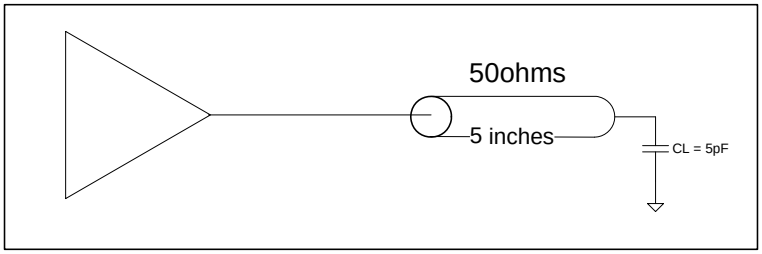


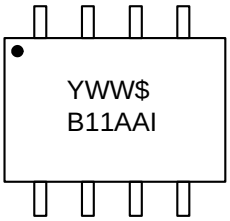
Figure 2. 5PB11xx Output Phase Noise 70.9fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 5PB11xx high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 58.9fs of RMS phase jitter while the output of 5PB11xx has about 70.9fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 39fs.

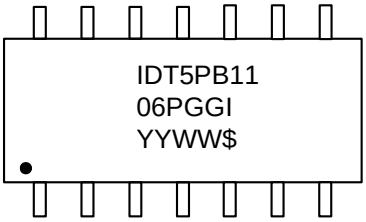
Test Load and Circuit



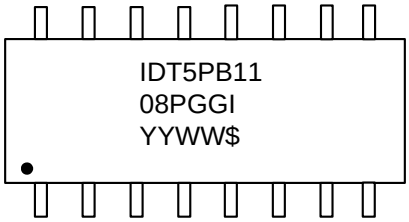
Marking Diagrams



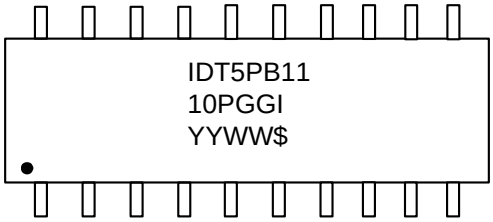
8-pin TSSOP



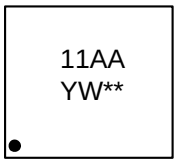
14-pin TSSOP



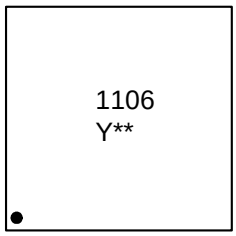
16-pin TSSOP



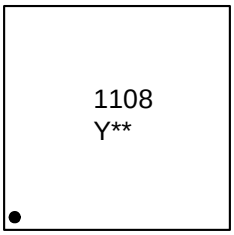
20-pin TSSOP



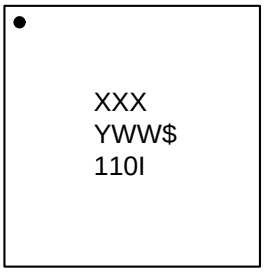
8-pin DFN



16-pin QFN



16-pin QFN

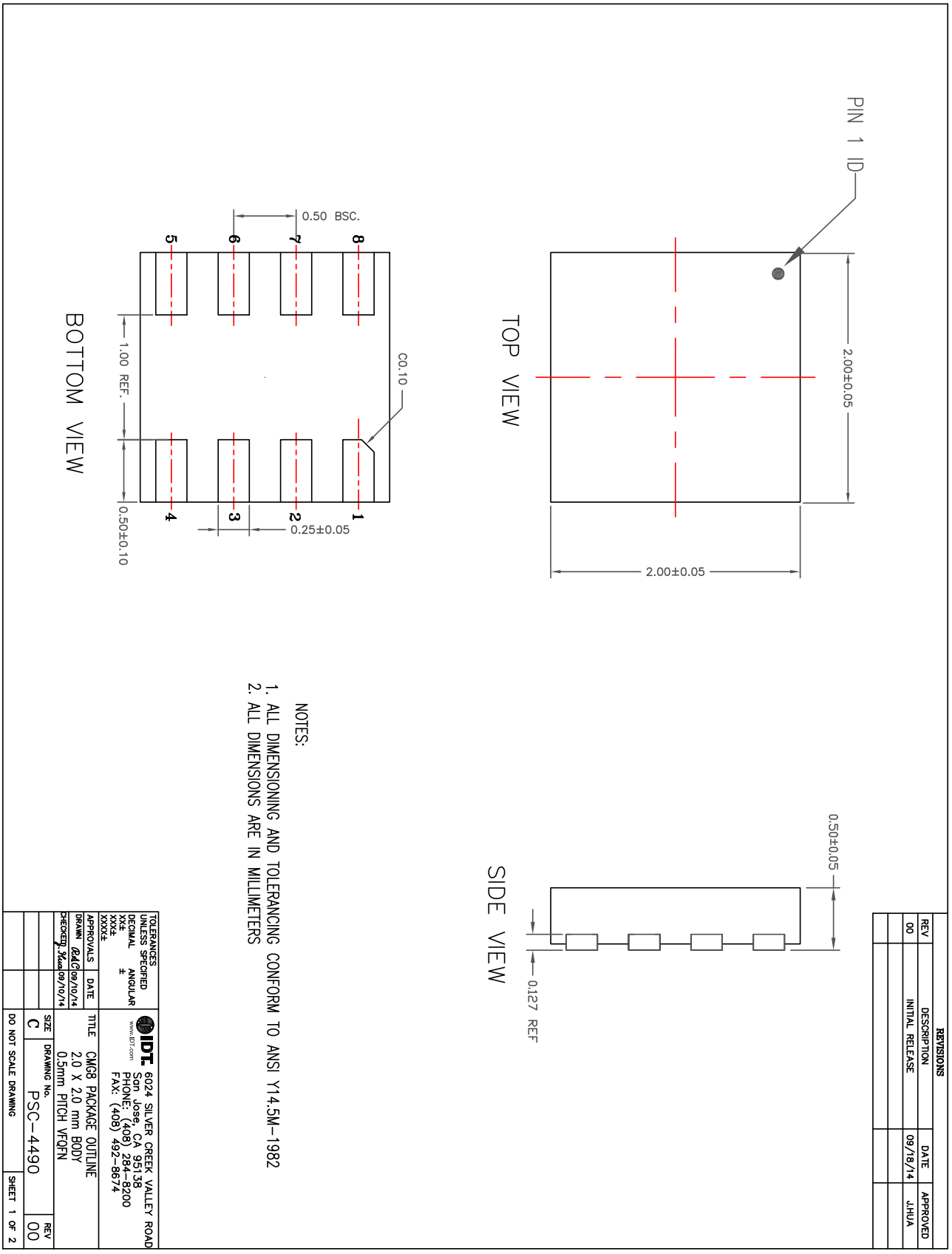


20-pin QFN

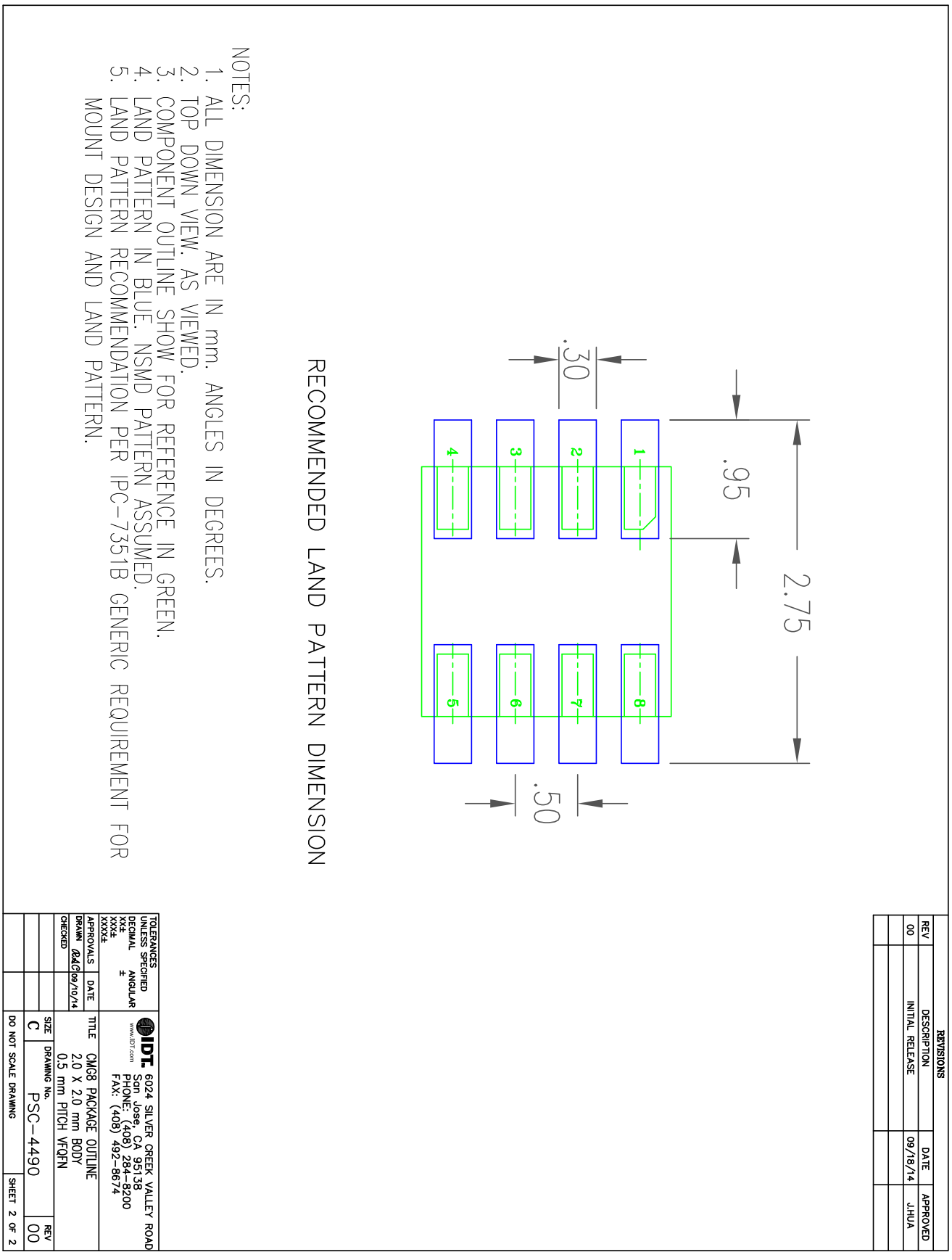
Notes:

1. “AA” denotes the last two digits of the part number for 8-pin TSSOP and DFN (e.g. 02, 04).
2. “**” is the lot sequence.
3. “XXX” denotes the last three characters of the Asm lot (20-pin QFN only).
4. “YYWW”, “YWW”, “YW”, or “Y” is the last digit(s) of the year and week that the part was assembled.
5. “$” denotes the mark code.
6. “G” after the two-letter package code denotes RoHS compliant package.
7. “I” denotes extended temperature range device.
8. Bottom marking: country of origin (TSSOP only).

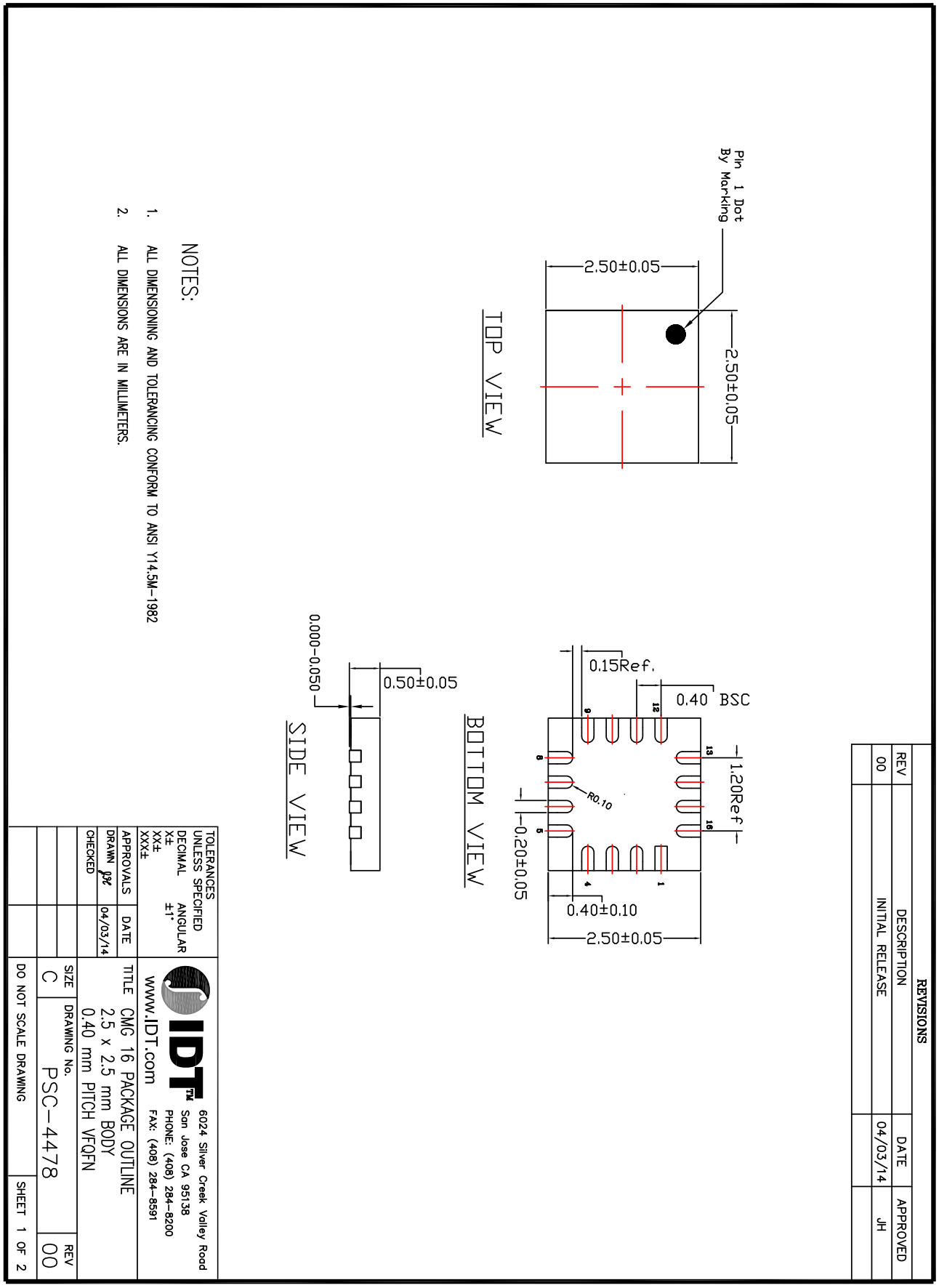
Package Outline and Package Dimensions (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



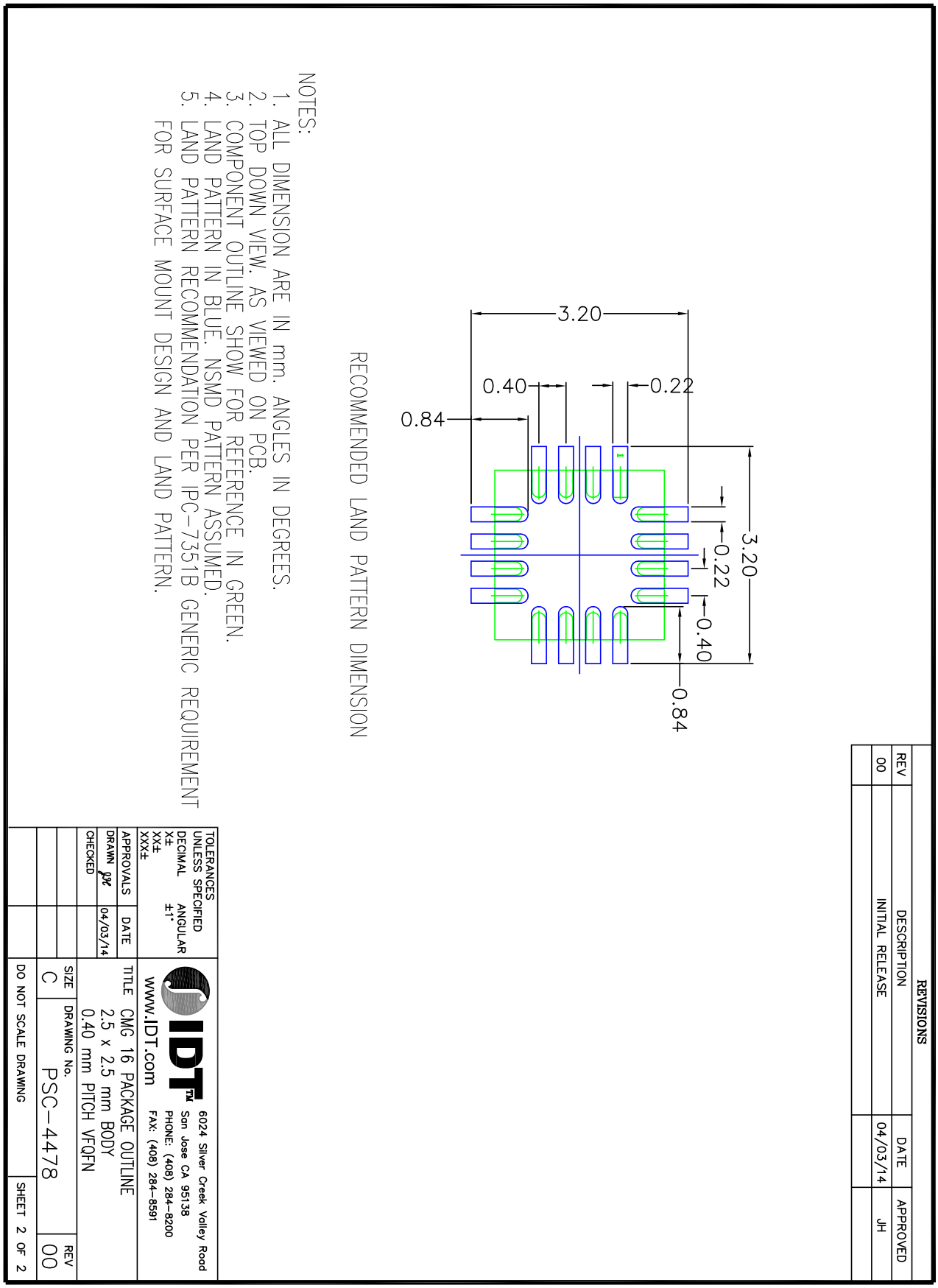
Package Outline and Package Dimensions, cont. (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



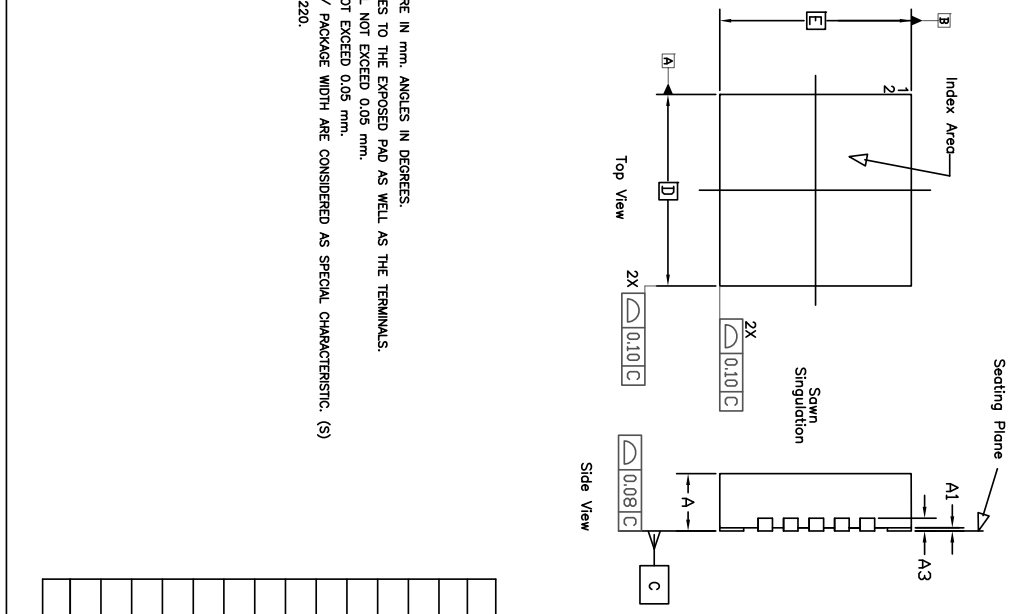
Package Outline and Package Dimensions (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



Package Outline and Package Dimensions, cont. (16-pin QFN, 2.5mm x 2.5mm Body, 0.4mm pitch)



Package Outline and Package Dimensions (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/14/08	RC
01	ADD EPAD OPTION	11/28/12	RC
02	COMBINE POD & LAND PATTERN	12/5/13	J.HUA
03	Change Dimension aaa	7/14/14	J.HUA

EPAD OPTION	P1			P2		
Symbol	MIN	NOM	MAX	MIN	NOM	MAX
E2	0.95	1.10	1.25	1.55	1.65	1.75
D2	0.95	1.10	1.25	1.55	1.65	1.75

NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.

COMMON DIMENSION

	DIMENSION		
Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 Ref	
b	0.17	0.20	0.25
e		0.40 BASIC	
N		20	
ND		5	
NE		5	
D		3.00 BASIC	
E		3.00 BASIC	
D2		SEE EPAD OPTION	
E2		SEE EPAD OPTION	
L	0.30	0.40	0.50

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± ±1°
XX±
XXX±

APPROVALS DATE
DRAWN RAC 11/14/08
CHECKED

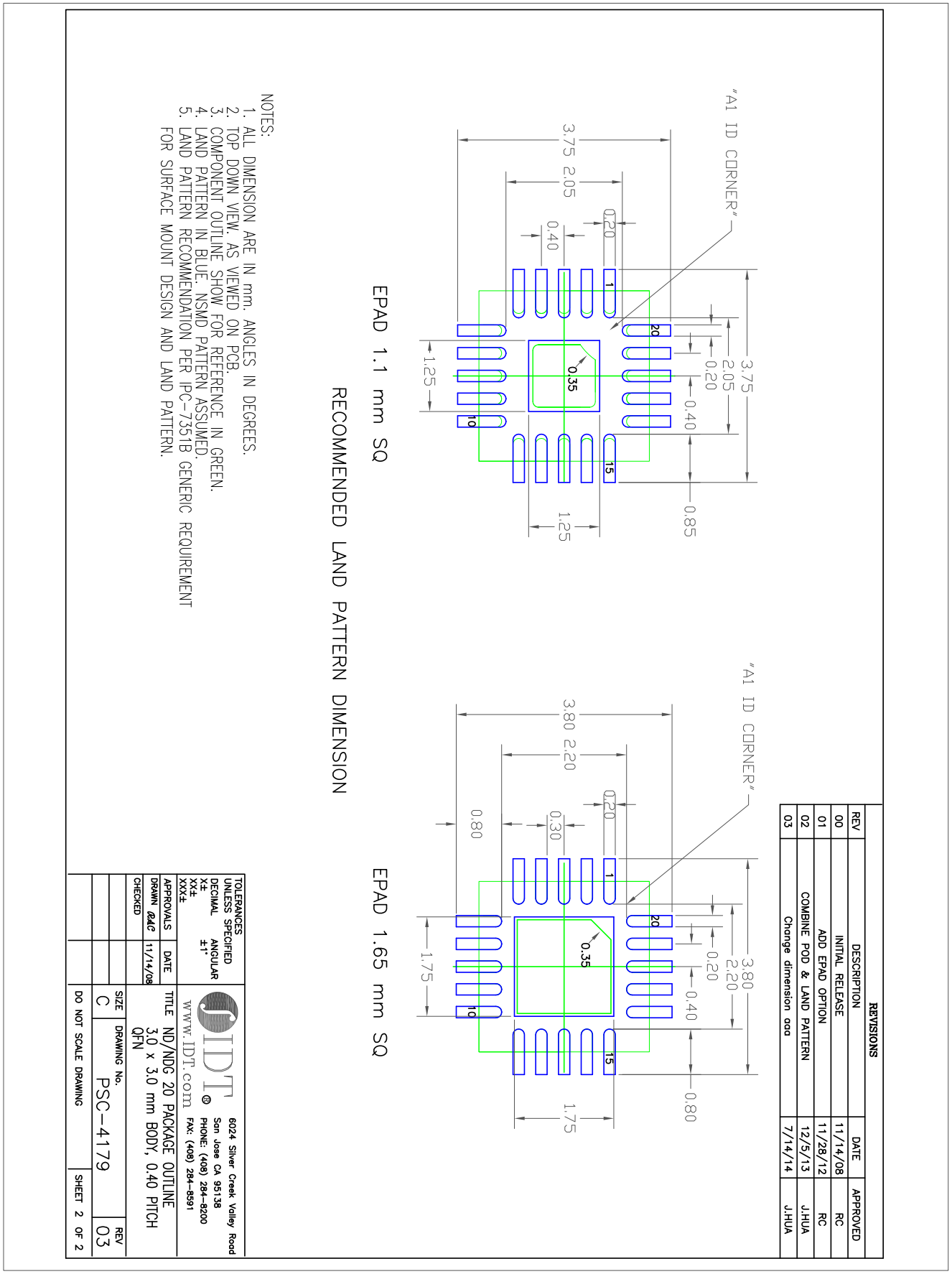
IDT® www.IDT.com
6024 Silver Creek Valley Road
San Jose CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-8591

TITLE ND/NDG 20 PACKAGE OUTLINE
3.0 x 3.0 mm BODY, 0.40 PITCH
QFN

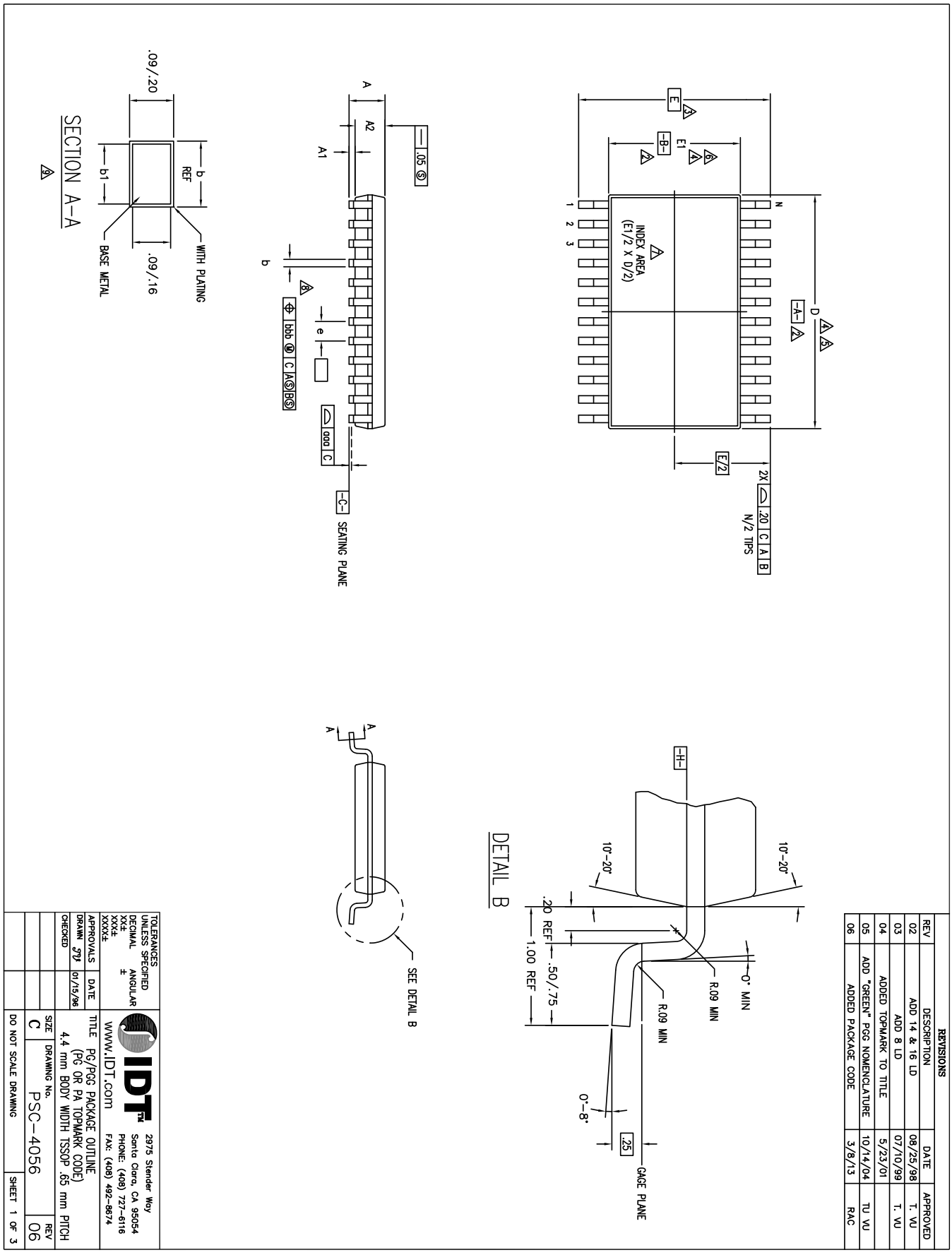
SIZE C | DRAWING No. PSC-4179 | REV 03

DO NOT SCALE DRAWING | SHEET 1 OF 2

Package Outline and Package Dimensions, cont. (20-pin QFN, 3mm x 3mm Body, 0.4mm pitch)



Package Outline and Package Dimensions (8-, 14-, 16-, 20-pin TSSOP)



Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC

	PG/PGG8				PG/PGG14				PG/PGG16				PG/PGG20			
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB–1			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.20		–	–	1.20		–	–	1.20		–	–	1.20	
A1	.05	–	.15		.05	–	.15		.05	–	.15		.05	–	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	2.90	3.00	3.10	4,5	4.90	5.00	5.10	4,5	4.90	5.00	5.10	4,5	6.40	6.50	6.60	4,5
E	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3
E1	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6
e	.65 BSC				.65 BSC				.65 BSC				.65 BSC			
b	.19	–	.30		.19	–	.30		.19	–	.30		.19	–	.30	
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25	
aaa	–	–	.10		–	–	.10		–	–	.10		–	–	.10	
bbb	–	–	.10		–	–	.10		–	–	.10		–	–	.10	
N	8				14				16				20			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

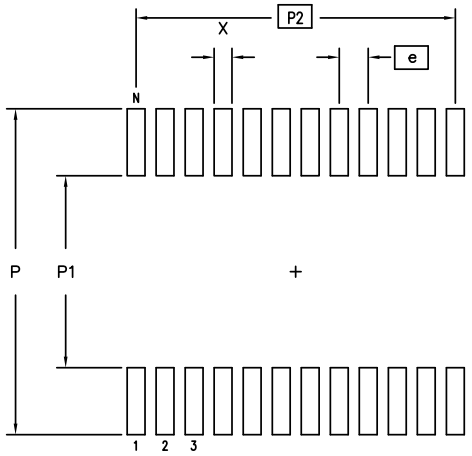
11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–153, VARIATION AA, AB–1, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com	2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727–6116 FAX: (408) 492–8674	
APPROVALS / DATE	TITLE	PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH	
DRAWN TV 01/15/96			
CHECKED	SIZE C	DRAWING No. PSC–4056	REV 06
	DO NOT SCALE DRAWING		SHEET 2 OF 3

Package Outline and Package Dimensions, cont. (8-, 14-, 16-, 20-pin TSSOP)

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	ADD 14 & 16 LD	08/25/98	T. VU
03	ADD 8 LD	07/10/99	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	
05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU
06	ADDED PACKAGE CODE	3/8/13	RAC

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95 BSC		3.90 BSC		4.55 BSC		5.85 BSC	
X	.30	.50	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	8		14		16		20	

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX± ANGULAR ±

APPROVALS	DATE
DRAWN JV	01/15/96
CHECKED	

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2975 Stender Way
Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE PG/PGG PACKAGE OUTLINE
(PG OR PA TOPMARK CODE)
4.4 mm BODY WIDTH TSSOP .65 mm PITCH

SIZE	DRAWING No.	REV
C	PSC-4056	06

DO NOT SCALE DRAWING | SHEET 3 OF 3

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
5PB1102PGGI	see page 8	Tubes	8-pin TSSOP	-40 to +105 °C
5PB1102PGGI8		Tape and Reel	8-pin TSSOP	-40 to +105 °C
5PB1104PGGI		Tubes	8-pin TSSOP	-40 to +105 °C
5PB1104PGGI8		Tape and Reel	8-pin TSSOP	-40 to +105 °C
5PB1106PGGI		Tubes	14-pin TSSOP	-40 to +105 °C
5PB1106PGGI8		Tape and Reel	14-pin TSSOP	-40 to +105 °C
5PB1108PGGI		Tubes	16-pin TSSOP	-40 to +105 °C
5PB1108PGGI8		Tape and Reel	16-pin TSSOP	-40 to +105 °C
5PB1110PGGI		Tubes	20-pin TSSOP	-40 to +105 °C
5PB1110PGGI8		Tape and Reel	20-pin TSSOP	-40 to +105 °C
5PB1102CMGI		Cut Tape	8-pin DFN	-40 to +105 °C
5PB1102CMGI8		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1104CMGI		Cut Tape	8-pin DFN	-40 to +105 °C
5PB1104CMGI8		Tape and Reel	8-pin DFN	-40 to +105 °C
5PB1106CMGI		Cut Tape	16-pin QFN	-40 to +105 °C
5PB1106CMGI8		Tape and Reel	16-pin QFN	-40 to +105 °C
5PB1108CMGI		Cut Tape	16-pin QFN	-40 to +105 °C
5PB1108CMGI8		Tape and Reel	16-pin QFN	-40 to +105 °C
5PB1110NDGI		Tubes	20-pin QFN	-40 to +105 °C
5PB1110NDGI8		Tape and Reel	20-pin QFN	-40 to +105 °C

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	03/20/15	B. Chandhoke	Initial release.
B	05/19/15	B. Chandhoke	1. Expanded Output Enable function text in General Description, and within the note under "Output Logic Table". 2. Updated all "Buffer Additive Phase Jitter, RMS" conditions from 125MHz to 156.25MHz.

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