SAM DA1

ARM-based Microcontroller

SUMMARY DATASHEET

Description

The Atmel® SAM DA1 is a series of low-power automotive microcontrollers using the 32-bit ARM® Cortex®-M0+ processor with 32 to 64 pins and up to 64KB of Flash, up to 8KB of SRAM and up to 2KB Read-While-Write (RWW) Flash section. The SAM DA1 devices operate at a maximum frequency of 48MHz and reach 2.14 Coremark/MHz.

They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin-compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, patented Atmel Event System for inter-peripheral signaling.

The Atmel SAM DA1 devices have the following features: In-system programmable Flash, eight-channel direct memory access (DMA) controller, 12-channel event system, programmable interrupt controller, up to 52 programmable I/O pins, 32-bit real-time clock and calendar, five 16-bit timer/counters (TC) and three 16-bit timer/counters for control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications.

The series provides up to six serial communication modules (SERCOM) that each can be configured to act as a USART, UART, SPI, I2C up to 3.4MHz, and LIN slave; up to twenty-channel 350ksps 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, one 10-bit 350ksps DAC, two analog comparators with window mode, programmable watchdog timer, brown-out detector and power-on reset and two-pin serial wire debug (SWD) program and debug interface. Peripheral Touch Controller supporting capacitive buttons, sliders, wheels and proximity sensing, one full-speed USB 2.0 embedded host and device interface and one inter-IC sound controller (I^2S).

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM DA1 devices offer two software-selectable sleep modes, idle and standby. In idle mode the CPU is stopped while all other functions can be kept running.

This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

In standby all clocks and functions are stopped except those selected to continue running. The device supports SleepWalking. SleepWalking allows peripherals to wake up from sleep based on predefined conditions, allowing the CPU to wake up only when needed, e.g., when a threshold is crossed or a result is ready. The Peripheral Event System supports synchronous and asynchronous events, allowing peripherals to receive, respond to and send events even in standby mode. The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for non-intrusive on-chip application code debugging. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

Atmel® SAM DA1 devices are supported by a complete suite of program and system development tools, including C compilers, macro-assemblers, program debugger/simulators, programmers and evaluation kits.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
  - Single-cycle hardware multiplier
  - Micro trace buffer
- Memories
  - 16/32/64KB in-system self-programmable Flash
  - 0.5/1/2KB Read-While-Write (RWW) Flash section
  - 4/4/8KB SRAM memory
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz digital frequency locked loop (DFLL48M) and 48MHz to 96MHz fractional digital phase locked loop (FDPLL96M)
  - External interrupt controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin serial wire debug (SWD) programming, test and debugging interface
- Low power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Peripherals
  - 8-channel direct memory access controller (DMAC)
  - 12-channel event system
  - Five 16-bit timer/counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - Three 16-bit timer/counters for control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering for enhancing resolution with up to 5-bit and reduce quantization error
  - 32-bit real time counter (RTC) with clock/calendar function
  - Watchdog timer (WDT)
  - CRC-32 generator

- One full speed (12Mbps) universal serial bus (USB) 2.0 controller
  - Device 2.0 and reduced-host low speed and full speed
  - Flexible end-point configuration and management with dedicated DMA channels
  - On-chip transceivers including pull-ups and serial resistors
  - Crystal-less operation in device mode
- Up to six serial communication interfaces (SERCOM), each configurable to operate as either:
  - USART with full-duplex and single-wire half-duplex configuration
  - I2C up to 3.4MHz
  - SPI
  - LIN slave
- One two-channel inter-IC sound (I^2S) interface
- One 12-bit, 350ksps analog-to-digital converter (ADC) with up to 20 channels
  - Differential and single-ended input
  - 1/2x to 16x programmable gain stage
  - Automatic offset and gain error compensation
  - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
- 10-bit, 350ksps digital-to-analog converter (DAC)
- Two analog comparators (AC) with window compare function
- Peripheral Touch Controller (PTC)
  - Up to 256-channel capacitive touch and proximity sensing

- I/O
  - Up to 52 programmable I/O pins
- Packages
  - 64-pin TQFP
  - 48-pin TQFP, QFN
  - 32-pin TQFP, QFN
- Operating voltage
  - 2.7V to 3.63V
- Temperature range
  - –40 to +105°C

1. Pinout

Figure 1-1. SAM DA1J

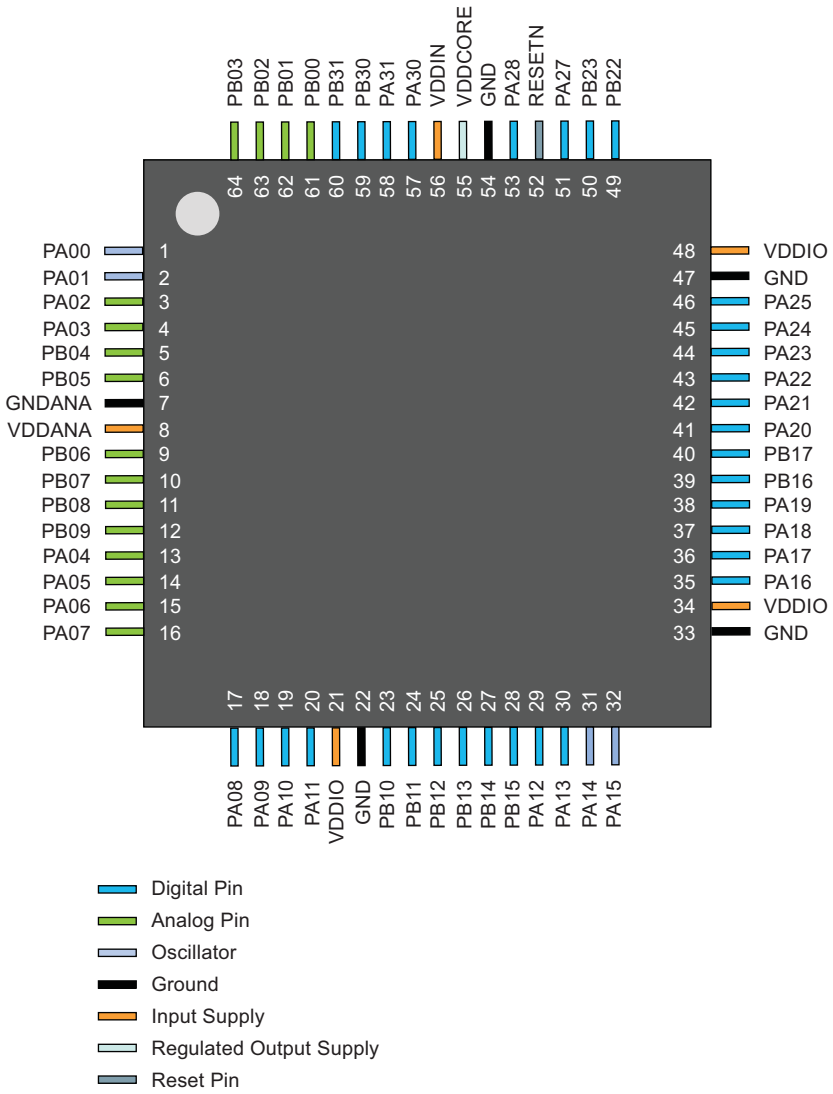


Figure 1-2. SAM DA1G

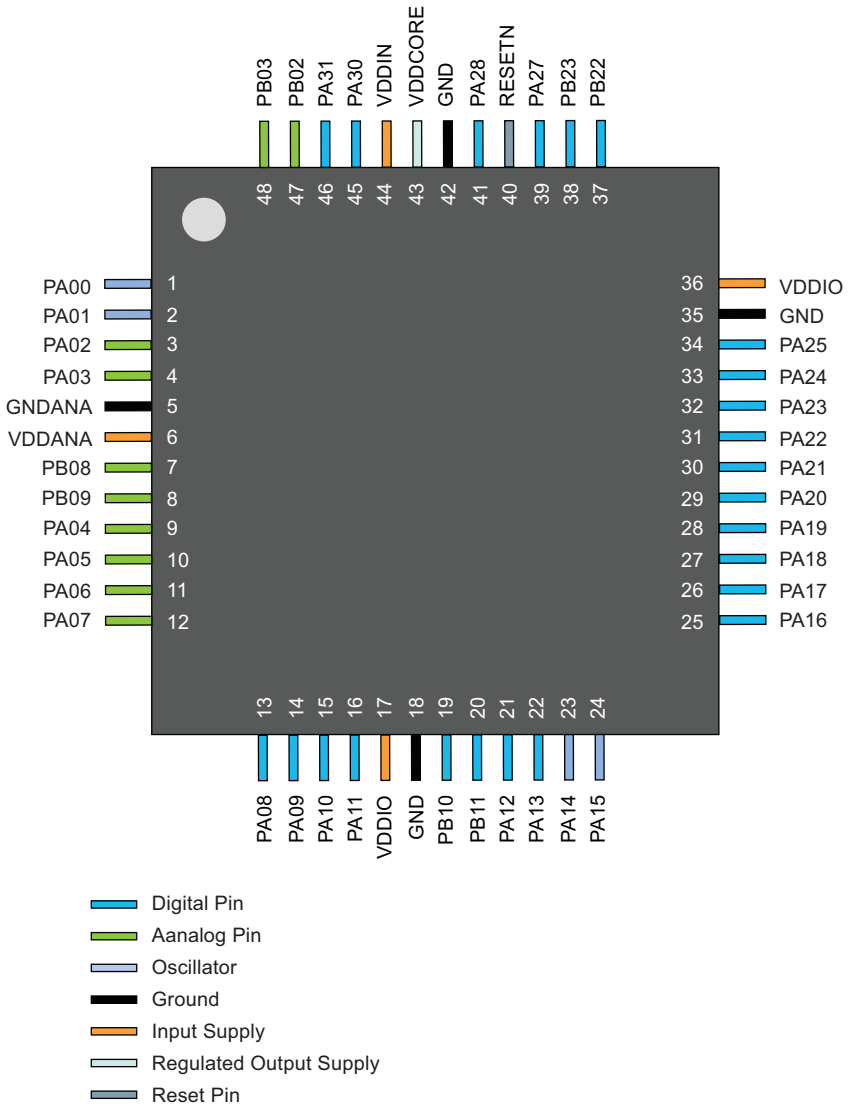
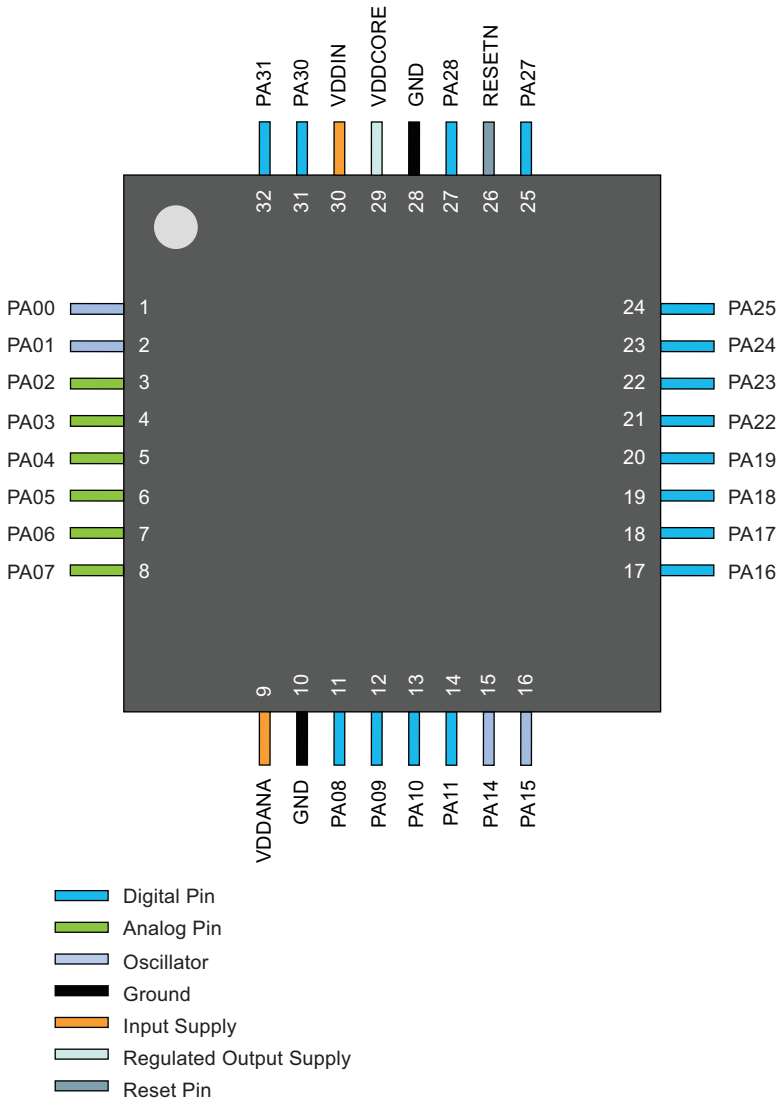


Figure 1-3. SAM DA1E



2. I/O Multiplexing and Considerations

2.1 Multiplexed Signals

By default each pin is controlled by the PORT as a general purpose I/O and alternatively can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the peripheral multiplexer enable bit in the pin configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to “1”. The selection of peripheral function A to H is done by writing to the peripheral multiplexing odd and even bits in the peripheral multiplexing register (PMUXn.PMUXE/O) in the PORT.

PIN			I/O Pin	Supply	Type	A	B					C	D	E	F	G	H
SAM DA1E	SAM DA1G	SAM DA1J				EIC	REF	ADC	AC	PTC	DAC	SERCOM	SEROM-ALT	TC/ TCC	TCC		AC/ CLK
1	1	1	PA00	VDD ANA		E00							SERCOM 1/Pad[0]	TCC2-WO[0]			
2	2	2	PA01	VDD ANA		E01							SERCOM 1-PAD[1]	TCC2-WO[1]			
3	3	3	PA02	VDD ANA		E02		AIN[0]		Y[0]	VOUT						
4	4	4	PA03	VDD ANA		E03	ADC/ VREF ADAC/ VREFP	AIN[1]		Y[1]							
		5	PB04	VDD ANA		E04		AIN[12]		Y[10]							
		6	PB05	VDD ANA		E05		AIN[13]		Y[11]							
		9	PB06	VDD ANA		E06		AIN[14]		Y[12]							
		10	PB07	VDD ANA		E07		AIN[15]		Y[13]							
	7	11	PB08	VDD ANA		E08		AIN[2]		Y[14]			SERCOM 4-PAD[0]	TC4-WO[0]			
	8	12	PB09	VDD ANA		E09		AIN[3]		Y[15]			SERCOM 4-PAD[1]	TC4-WO[1]			
5	9	13	PA04	VDD ANA		E04	ADC VREFP	AIN[4]	AIN[0]	Y[2]			SERCOM 0-PAD[0]	TCC0-WO[0]			
6	10	14	PA05	VDD ANA		E05		AIN[5]	AIN[1]	Y[3]			SERCOM 0-PAD[1]	TCC0-WO[1]			
7	11	15	PA06	VDD ANA		E06		AIN[6]	AIN[2]	Y[4]			SERCOM 0-PAD[2]	TCC1-WO[0]			
8	12	16	PA07	VDD ANA		E07		AIN[7]	AIN[3]	Y[5]			SERCOM 0-PAD[3]	TCC1-WO[1]		I2S/SD[0]	
11	13	17	PA08	VDDIO	I^2C	NMI		AIN[16]		X[0]		SERCOM 0-PAD[0]	SERCOM 2-PAD[0]	TCC0-WO[0]	TCC1-WO[2]	I2S/SD[1]	
12	14	18	PA09	VDDIO	I^2C	E09		AIN[17]		X[1]		SERCOM 0-PAD[1]	SERCOM 2-PAD[1]	TCC0-WO[1]	TCC1-WO[3]	I2S/MCK[0]	
13	15	19	PA10	VDDIO		E10		AIN[18]		X[2]		SERCOM 0-PAD[2]	SERCOM 2-PAD[2]	TCC1-WO[0]	TCC0-WO[2]	I2S/SCK[0]	GCLK_IO[4]
14	16	20	PA11	VDDIO		E11		AIN[19]		X[3]		SERCOM 0-PAD[3]	SERCOM 2-PAD[3]	TCC1-WO[1]	TCC0-WO[3]	I2S/FS[0]	GCLK_IO[5]
	19	23	PB10	VDDIO		E10							SERCOM 4-PAD[2]	TC5-WO[0]	TCC0-WO[4]	I2S/MCK[1]	GCLK_IO[4]
	20	24	PB11	VDDIO		E11							SERCOM 4-PAD[3]	TC5-WO[1]	TCC0-WO[5]	I2S/SCK[1]	GCLK_IO[5]

2.1 Multiplexed Signals (Continued)

By default each pin is controlled by the PORT as a general purpose I/O and alternatively can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the peripheral multiplexer enable bit in the pin configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to “1”. The selection of peripheral function A to H is done by writing to the peripheral multiplexing odd and even bits in the peripheral multiplexing register (PMUXn.PMUXE/O) in the PORT.

PIN			I/O Pin	Supply	Type	A	B					C	D	E	F	G	H
SAM DA1E	SAM DA1G	SAM DA1J				EIC	REF	ADC	AC	PTC	DAC	SERCOM	SEROM-ALT	TC/ TCC	TCC		AC/ CLK
		25	PB12	VDDIO	I2C	E12				X[12]		SERCOM 4-PAD[0]		TC4-WO[0]	TCC0-WO[6]	I2S/FS[1]	GCLK_IO[6]
		26	PB13	VDDIO	I2C	E13				X[13]		SERCOM 4-PAD[1]		TC4-WO[1]	TCC0-WO[7]		GCLK_IO[7]
		27	PB14	VDDIO		E14				X[14]		SERCOM 4-PAD[2]		TC5-WO[0]			GCLK_IO[0]
		28	PB15	VDDIO		E15				X[15]		SERCOM 4-PAD[3]		TC5-WO[1]			GCLK_IO[1]
	21	29	PA12	VDDIO	I2C	E12						SERCOM 2-PAD[0]	SERCOM 4-PAD[0]	TCC2-WO[0]	TCC0-WO[6]		AC/ CMP[0]
	22	30	PA13	VDDIO	I2C	E13						SERCOM 2-PAD[1]	SERCOM 4-PAD[1]	TCC2-WO[1]	TCC0-WO[7]		AC/ CMP[1]
15	23	31	PA14	VDDIO		E14						SERCOM 2-PAD[2]	SERCOM 4-PAD[2]	TC3-WO[0]	TCC0-WO[4]		GCLK_IO[0]
16	24	32	PA15	VDDIO		E15						SERCOM 2-PAD[3]	SERCOM 4-PAD[3]	TC3-WO[1]	TCC0-WO[5]		GCLK_IO[1]
17	25	35	PA16	VDDIO	I2C	E00				X[4]		SERCOM 1-PAD[0]	SERCOM 3-PAD[0]	TCC2-WO[0]			GCLK_IO[2]
18	26	36	PA17	VDDIO	I2C	E01				X[5]		SERCOM 1-PAD[1]	SERCOM 3-PAD[1]	TCC2-WO[1]			GCLK_IO[3]
19	27	37	PA18	VDDIO		E02				X[6]		SERCOM 1-PAD[2]	SERCOM 3-PAD[2]	TC3-WO[0]	TCC0-WO[2]		AC/ CMP[0]
20	28	38	PA19	VDDIO		E03				X[7]		SERCOM 1-PAD[3]	SERCOM 3-PAD[3]	TC3-WO[1]	TCC0-WO[3]	I2S/SD[0]	AC/ CMP[1]
		39	PB16	VDDIO	I2C	E00						SERCOM 5-PAD[0]		TC6-WO[0]	TCC0-WO[4]	I2S/SD[1]	GCLK_IO[2]
		40	PB17	VDDIO	I2C	E01						SERCOM 5-PAD[1]		TC6-WO[1]	TCC0-WO[5]	I2S/MCK[0]	GCLK_IO[3]
	29	41	PA20	VDDIO		E04				X[8]		SERCOM 5-PAD[2]	SERCOM 3-PAD[2]	TC7-WO[0]	TCC0-WO[6]	I2S/SCK[0]	GCLK_IO[4]
	30	42	PA21	VDDIO		E05				X[9]		SERCOM 5-PAD[3]	SERCOM 3-PAD[3]	TC7-WO[1]	TCC0-WO[7]	I2S/FS[0]	GCLK_IO[5]
21	31	43	PA22	VDDIO	I2C	E06				X[10]		SERCOM 3-PAD[0]	SERCOM 5-PAD[0]	TC4-WO[0]	TCC0-WO[4]		GCLK_IO[6]
22	32	44	PA23	VDDIO	I2C	E07				X[11]		SERCOM 3-PAD[1]	SERCOM 5-PAD[1]	TC4-WO[1]	TCC0-WO[5]	USB/SOF 1kHz	GCLK_IO[7]
23	33	45	PA24	VDDIO		E12						SERCOM 3-PAD[2]	SERCOM 5-PAD[2]	TC5-WO[0]	TCC1-WO[2]	USB/DM	
24	34	46	PA25	VDDIO		E13						SERCOM 3-PAD[3]	SERCOM 5-PAD[3]	TC5-WO[1]	TCC1-WO[3]	USB/DP	
	37	49	PB22	VDDIO		E06							SERCOM 5-PAD[2]	TC7-WO[0]			GCLK_IO[0]
	38	50	PB23	VDDIO		E07							SERCOM 5-PAD[3]	TC7-WO[1]			GCLK_IO[1]

2.1 Multiplexed Signals (Continued)

By default each pin is controlled by the PORT as a general purpose I/O and alternatively can be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the peripheral multiplexer enable bit in the pin configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to “1”. The selection of peripheral function A to H is done by writing to the peripheral multiplexing odd and even bits in the peripheral multiplexing register (PMUXn.PMUXE/O) in the PORT.

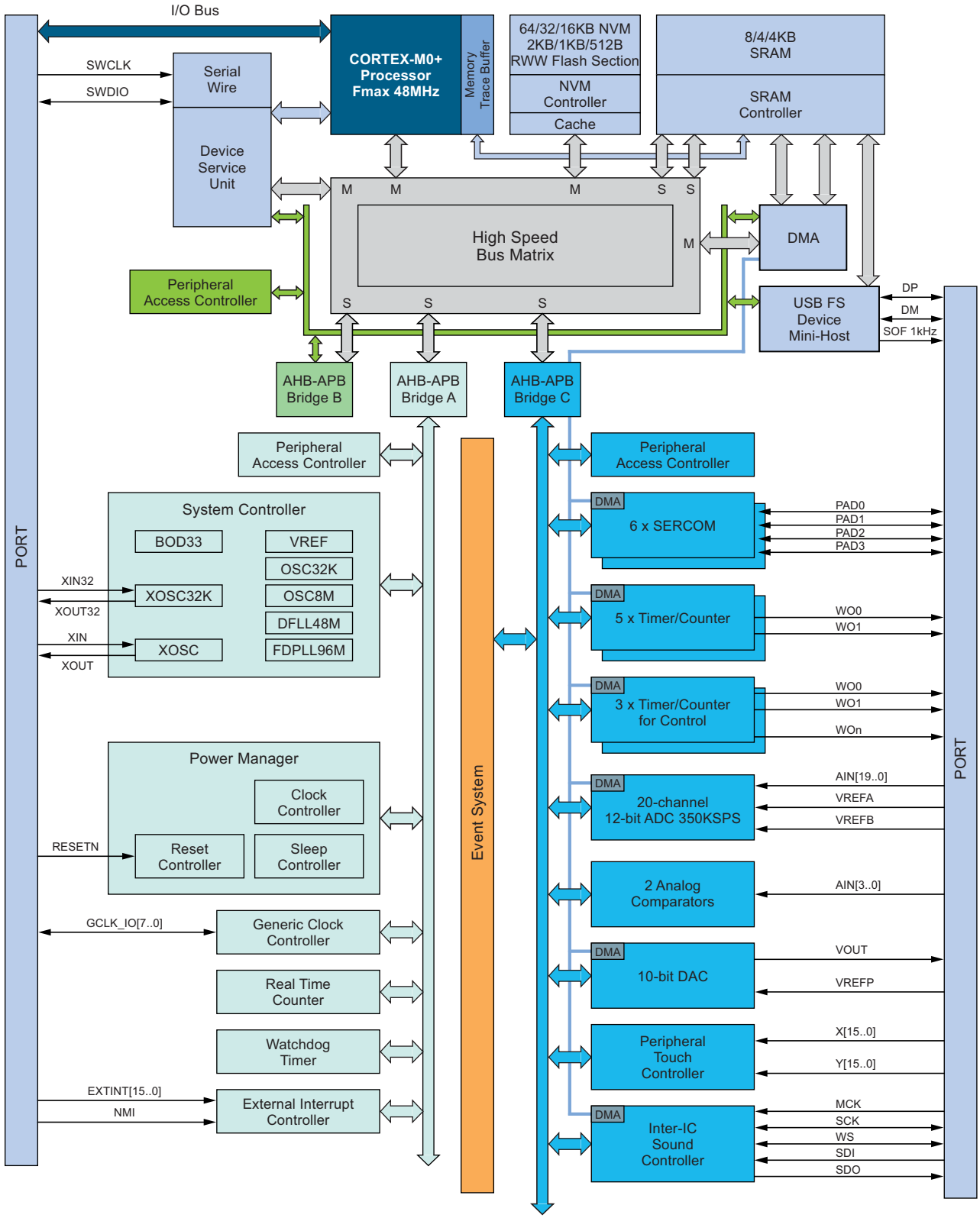
PIN			I/O Pin	Supply	Type	A	B					C	D	E	F	G	H
SAM DA1E	SAM DA1G	SAM DA1J				EIC	REF	ADC	AC	PTC	DAC	SERCOM	SEROM-ALT	TC/ TCC	TCC		AC/ CLK
25	39	51	PA27	VDDIO		E15											GCLK_ IO[0]
27	41	53	PA28	VDDIO		E08								TC6-WO[1]			GCLK_ IO[0]
31	45	57	PA30	VDDIO		E10							SERCOM 1-PAD[2]	TCC1-WO[0]		SWCLK	GCLK_ IO[0]
32	46	58	PA31	VDDIO		E11							SERCOM 1-PAD[3]	TCC1-WO[1]		SWIO	
		59	PB30	VDDIO	I^2C	E14							SERCOM 5-PAD[0]	TCC0-WO[0]	TCC1-WO[2]		
		60	PB31	VDDIO	I^2C	E15							SERCOM 5-PAD[1]	TCC0-WO[1]	TCC1-WO[3]		
		61	PB00	VDD ANA		E00		AIN[8]		Y[6]			SERCOM 5-PAD[2]	TC7-WO[0]			
		62	PB01	VDD ANA		E01		AIN[9]		Y[7]			SERCOM 5-PAD[3]	TC7-WO[1]			
	47	63	PB02	VDD ANA		E02		AIN[10]		Y[8]			SERCOM 5-PAD[0]	TC6-WO[0]			
	48	64	PB03	VDD ANA		E03		AIN[11]		Y[9]			SERCOM 5-PAD[1]	TC6-WO[1]			

3. Configuration Summary

Table 3-1. Configuration Summary

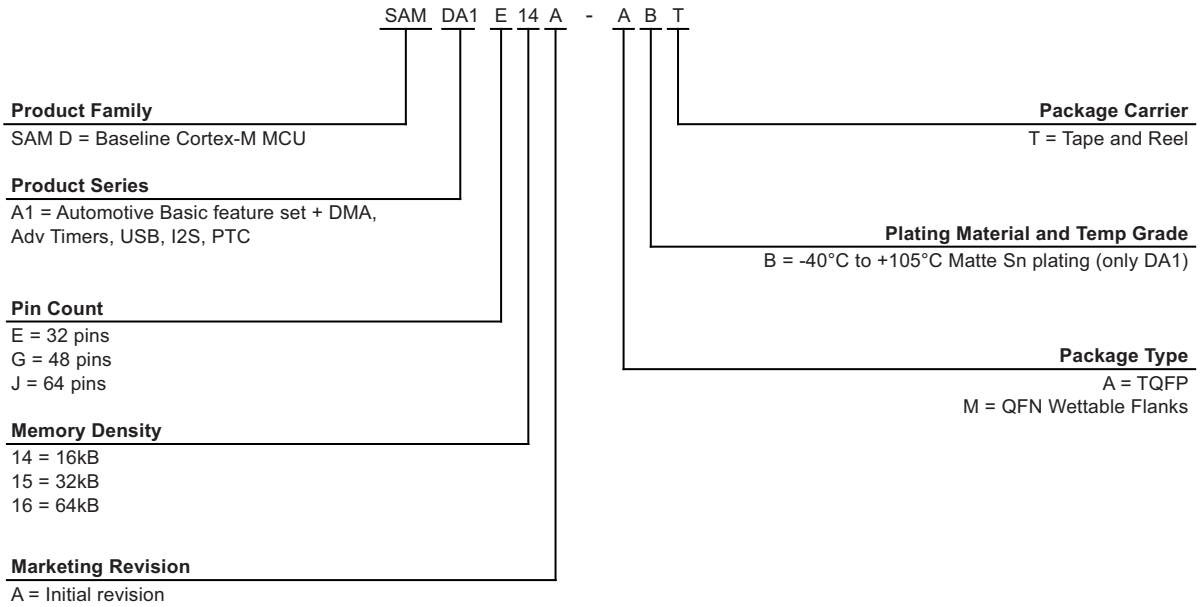
	SAM DA1J	SAM DA1G	SAM DA1E
Pins	64	48	32
General Purpose I/O-pins (GPIOs)	52	38	26
Flash	64/32/16KB	64/32/16KB	64/32/16KB
RWW Flash section	2KB/1KB/512B	2KB/1KB/512B	2KB/1KB/512B
SRAM	8/4/4KB	8/4/4KB	8/4/4KB
Timer counter (TC) instances	5	5	5
Waveform output channels per TC instance	2	2	2
Timer Counter for Control (TCC) instances	3	3	3
Waveform output channels per TCC	8/4/2	8/4/2	6/4/2
DMA channels	8	8	8
USB interface	1	1	1
Serial communication interface (SERCOM) instances	6	6	4
Inter-IC sound interface (I^2S)	1	1	1
Analog-to-digital converter (ADC) channels	20	14	10
Analog comparators (AC)	2	2	2
Digital-to-analog converter (DAC) channels	1	1	1
Real-time counter (RTC)	Yes	Yes	Yes
RTC alarms	1	1	1
RTC compare values	1 × 32-bit value or 2 × 16-bit values	1 × 32-bit value or 2 × 16-bit values	1 × 32-bit value or 2 × 16-bit values
External interrupt lines	16	16	16
Peripheral Touch Controller (PTC) X and Y lines	16x16	12x10	10x6
Maximum CPU frequency	48MHz		
Packages	TQFP	QFN TQFP	QFN TQFP
Clocks	32.768kHz crystal oscillator (XOSC32K) 0.4-32MHz crystal oscillator (XOSC) 32.768kHz internal oscillator (OSC32K) 8MHz high-accuracy internal oscillator (OSC8M) 48MHz digital frequency locked loop (DFLL48M) 96MHz fractional digital phase locked loop (FDPLL96M)		
Event system channels	12	12	12
Software debug interface	Yes	Yes	Yes
Watchdog timer (WDT)	Yes	Yes	Yes

Figure 3-1. Block Diagram



4. Ordering Information

Figure 4-1. Ordering Information



4.1 B-versions

Table 4-1. SAM DA1E

Ordering Code	FLASH (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temperature Grade	PTC, USB, I^2S
ATSAMDA1E14A-ABT	16K	4K	TQFP32	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1E14A-MBT	16K	4K	QFN32	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1E15A-ABT	32K	4K	TQFP32	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1E15A-MBT	32K	4K	QFN32	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1E16A-ABT	64K	8K	TQFP32	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1E16A-MBT	64K	8K	QFN32	Tape and reel	–40°C to +105°C	Yes

Table 4-2. SAM DA1G

Ordering Code	FLASH (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temperature Grade	PTC, USB, I^2S
ATSAMDA1G14A-ABT	16K	4K	TQFP48	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1G14A-MBT	16K	4K	QFN48	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1G15A-ABT	32K	4K	TQFP48	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1G15A-MBT	32K	4K	QFN48	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1G16A-ABT	64K	8K	TQFP48	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1G16A-MBT	64K	8K	QFN48	Tape and reel	–40°C to +105°C	Yes

Table 4-3. SAM DA1J

Ordering Code	FLASH (Bytes)	SRAM (Bytes)	Package	Carrier Type	Temperature Grade	PTC, USB, I^2S
ATSAMDA1J14A-ABT	16K	4K	TQFP64	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1J15A-ABT	32K	4K	TQFP64	Tape and reel	–40°C to +105°C	Yes
ATSAMDA1J16A-ABT	64K	8K	TQFP64	Tape and reel	–40°C to +105°C	Yes

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**