Dual 140V, Rail-to-Rail Output, Picoamp Input Current Op Amp

FEATURES

- **Supply Range: ±4.75V to ±70V (140V)**
- **0.1Hz to 10Hz Noise: 3.5μV_{P-P}**
- **Input Bias Current: 50pA Maximum**
- **Low Offset Voltage: 1.25mV Maximum**
- **Low Offset Drift: ±5μV/°C Maximum**
- **CMRR: 130dB Minimum**
- Rail-to-Rail Output Stage
- Output Sink and Source: 50mA
- 12MHz Gain-Bandwidth Product
- 21V/μs Slew Rate
- 11nV/√Hz Noise Density
- Thermal Shutdown
- 4mm × 6mm 16-Lead QFN Package

APPLICATIONS

- ATE
- Piezo Drivers
- Photodiode Amplifier
- High Voltage Regulators
- Optical Networking

DESCRIPTION

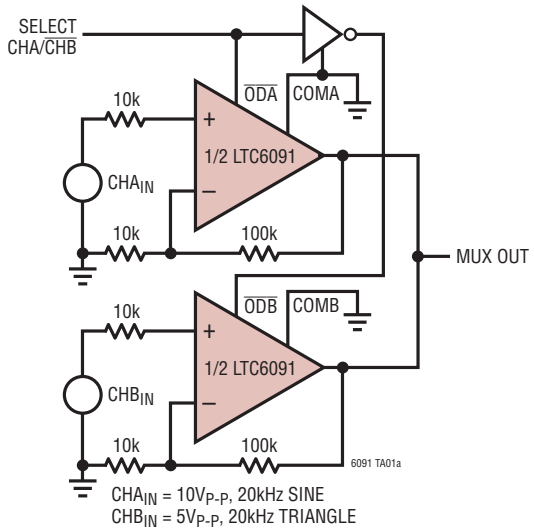
The LTC®6091 is a dual, high voltage precision operational amplifier. The low noise, low bias current input stage is ideal for high gain configurations. The LTC6091 has low input offset voltage, a rail-to-rail output stage, and can be run from a single 140V or split ±70V supplies.

The LTC6091 is internally protected against overtemperature conditions. A thermal warning output, $\overline{TFLAG}$, goes active when the die temperature approaches 150°C. The output stage can be turned off with the output disable pin $\overline{OD}$. By tying the $\overline{OD}$ pin to the thermal warning output, the part will disable the output stage when it is out of the safe operating area. These pins easily interface to any logic family.

The LTC6091 is unity-gain stable with up to a 200pF output capacitor. A wide input and output common mode range along with many features makes the LTC6091 useful for many high voltage applications.

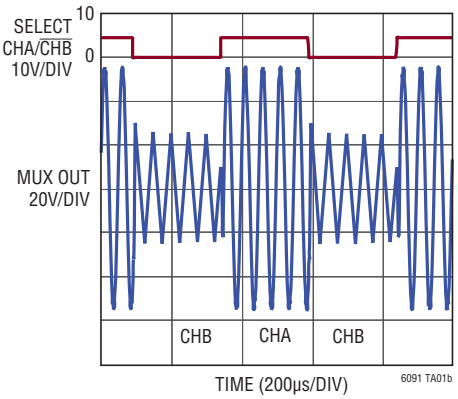
TYPICAL APPLICATION

High Voltage Analog MUX



CHA_{IN} = 10V_{P-P}, 20kHz SINE
CHB_{IN} = 5V_{P-P}, 20kHz TRIANGLE

V_{OUT} vs Time

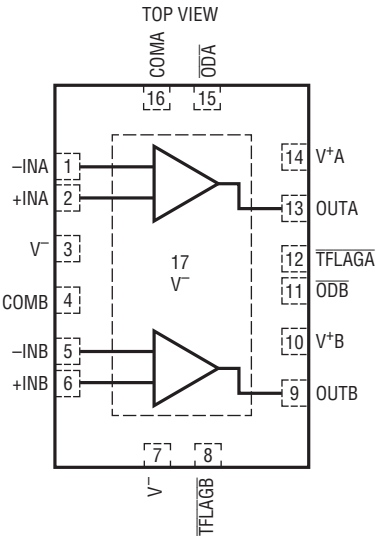


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+A to V^-, or V^+B to V^-) 150V
COMA ..... V^- to V^+A
COMB ..... V^- to V^+B
Input Voltage
  $\overline{ODA}$ ..... V^- to V^+A + 0.3V
  $\overline{ODB}$ ..... V^- to V^+B + 0.3V
  +INA, –INA ..... V^- – 0.3V to V^+A + 0.3V
  +INB, –INB ..... V^- – 0.3V to V^+B + 0.3V
  $\overline{ODA}$ to COMA, $\overline{ODB}$ to COMB ..... –3V to 7V
Input Current
  +INA, –INA, +INB, -INB ..... ±10mA
$\overline{TFLAGA}$, $\overline{TFLAGB}$ Output
  $\overline{TFLAGA}$ ..... V^- – 0.3V to V^+A + 0.3V
  $\overline{TFLAGB}$ ..... V^- – 0.3V to V^+B + 0.3V
  $\overline{TFLAGA}$ to COMA ..... –3V to 7V
  $\overline{TFLAGB}$ to COMB ..... –3V to 7V
Continuous Output Current
  OUTA , OUTB (Note 2) ..... $50mA_{RMS}$
Operating Junction Temperature Range
  (Note 3) ..... –40°C to 125°C
Specified Junction Temperature Range (Note 4)
  LTC6091I ..... –40°C to 85°C
  LTC6091H ..... –40°C to 125°C
Junction Temperature (Note 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10sec) ..... 300°C

PIN CONFIGURATION



UFE PACKAGE
32(16)-LEAD (4mm × 6mm) PLASTIC QFN

θ_{JC} = 15°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ESD Sensitive: The output pins (OUTA and OUTB) are sensitve to ESD. Any ESD greater than 500V may cause permanent damage to the device.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6091IUFE#PBF	LTC6091IUFE#TRPBF	6091	16-Lead Plastic QFN	–40°C to 85°C
LTC6091HUFE#PBF	LTC6091HUFE#TRPBF	6091	16-Lead Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 70V, V^- = –70V, V_{CM} = V_{OUT} = 0V, $V_{\overline{OD}}$ = open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		I-SUFFIX MIN	I-SUFFIX TYP	I-SUFFIX MAX	H-SUFFIX MIN	H-SUFFIX TYP	H-SUFFIX MAX	UNITS
V_{OS}	Input Offset Voltage				±330	±1000		±330	±1000	µV
			●		±330	±1250		±330	±1250	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	T_A = 25°C, ΔT_J = 70°C		–5	±3	5	–5	±3	5	µV/°C
I_B	Input Bias Current (Note 6)	Supply Voltage = ±70V			3			3		pA
		Supply Voltage = ±15V			0.3			0.3		pA
		Supply Voltage = ±15V	●			50			800	pA
I_{OS}	Input Offset Current (Note 6)	Supply Voltage = ±15V			0.5			0.5		pA
			●			30			120	pA
e_n	Input Noise Voltage Density	f = 1kHz			14			14		nV/√Hz
		f = 10kHz			11			11		nV/√Hz
	Input Noise Voltage	0.1Hz to 10Hz			3.5			3.5		μV_{P-P}
i_n	Input Noise Current Density				1			1		fA/√Hz
V_{CM}	Input Common Mode Range	Guaranteed by CMRR			±68			±68		V
			●	V^- + 3V		V^+ – 3V	V^- + 3V		V^+ – 3V	V
C_{IN}	Common Mode Input Capacitance				9			9		pF
C_{DIFF}	Differential Input Capacitance				5			5		pF
CMRR	Common Mode Rejection Ratio	V_{CM} = –67V to 67V		130	>140		130	>140		dB
			●	126			126			dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.75V to ±70V		112	>120		112	>120		dB
			●	106			106			dB
V_{OUT}	Output Voltage Swing High (Referred to V^+) (V_{OH})	No Load	●		10	25		10	25	mV
		I_{SOURCE} = 1mA	●		50	140		50	140	mV
		I_{SOURCE} = 10mA	●		450	1000		450	1000	mV
	Output Voltage Swing Low (Referred to V–) (V_{OL})	No Load	●		10	25		10	25	mV
		I_{SINK} = 1mA	●		30	80		30	80	mV
		I_{SINK} = 10mA	●		250	600		250	600	mV
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k		1000	>10000		1000	>10000		V/mV
		V_{OUT} from –60V to 60V	●	1000			1000			V/mV
I_{SC}	Output Short-Circuit Current (Source and Sink)	Supply Voltage = ±70V			90			90		mA
		Supply Voltage = ±15V	●	50			50			mA
SR	Slew Rate	A_{VCL} = –4, R_L = 10k			21			21		V/µs
			●	10			9			V/µs
GBW	Gain-Bandwidth Product	f_{TEST} = 20kHz, R_L = 10k			12			12		MHz
			●	5.5			5			MHz
ϕ_M	Phase Margin	R_L = 10k, C_L = 50pF			60			60		Deg
FPBW	Full-Power Bandwidth	V_{OUT} = 125V_{P-P}			40			40		kHz
			●	20			18			kHz
t_S	Settling Time 0.1%	V_{STEP} = 1V, A_V = 1, R_L = 10k			2			2		µs
I_S	Supply Current (Per Amplifier)	No Load			2.8	3.9		2.8	3.9	mA
			●			4.3			4.3	mA
V_S	Supply Voltage Range	Guaranteed by the PSRR Test	●	9.5		140	9.5		140	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test conditions are V^+ = 70V, V^- = –70V, V_{CM} = V_{OUT} = 0V, $V_{\overline{OD}}$ = open unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		I-SUFFIX MIN	I-SUFFIX TYP	I-SUFFIX MAX	H-SUFFIX MIN	H-SUFFIX TYP	H-SUFFIX MAX	UNITS
$\overline{ODH}$	$\overline{OD}$ Pin Voltage, Referenced to COM Pin	V_{IH}	●	COM + 1.8V			COM + 1.8V			V
$\overline{ODL}$	$\overline{OD}$ Pin Voltage, Referenced to COM Pin	V_{IL}	●			COM + 0.65V			COM + 0.65V	V
	Amplifier DC Output Impedance, Disabled	DC, $\overline{OD}$ = COM			>10			>10		MΩ
COMCM	COM Pin Voltage Range		●	V^-		V^+ – 5	V^-		V^+ – 5	V
COMV	COM Pin Open-Circuit Voltage		●	17	21	25	17	21	25	V
COMR	COM Pin Resistance		●	500	665	850	500	665	850	kΩ
TEMPF	Die Temperature Where $\overline{TFLAG}$ Is Active				145			145		°C
TEMPHYS	$\overline{TFLAG}$ Output Hysteresis				5			5		°C
I_{TFLAG}	$\overline{TFLAG}$ Pull-Down Current	$\overline{TFLAG}$ Output Voltage = 0V	●	70	200	330	70	200	330	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Either output (OUTA or OUTB) of the LTC6091 is capable of producing peak output currents in excess of 50mA. Current density limitations within the IC require the continuous RMS current supplied by either output (sourcing or sinking) over the operating lifetime of the part to be limited to under 50mA (absolute maximum). Proper heat sinking may be required to keep the junction temperature below the absolute maximum rating. Refer to the Power Dissipation and Thermal Considerations section of the data sheet for more information.

Note 3: The LTC6091I is guaranteed functional over the operating junction temperature range –40°C to 85°C. The LTC6091H is guaranteed functional over the operating junction temperature range –40°C to 125°C. Specifying the junction temperature range as an operating condition is applicable for devices with potentially significant quiescent power dissipation.

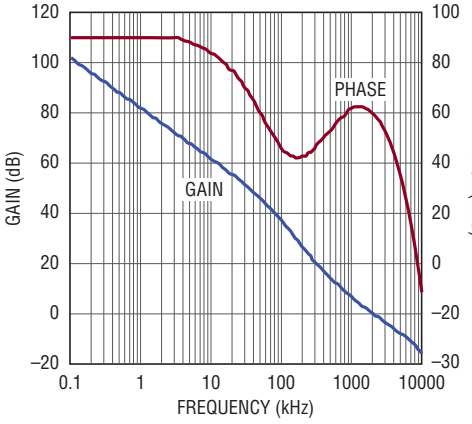
Note 4: The LTC6091I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6091H is guaranteed to meet specified performance from –40°C to 125°C.

Note 5: This device includes overtemperature protection that is intended to protect the device during momentary overload conditions. Operation above the specified maximum operating junction temperature is not recommended.

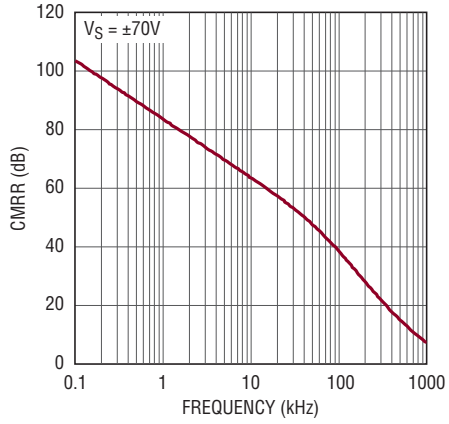
Note 6: Input bias and offset current is production tested with ±15V supplies. See Typical Performance Characteristics curves of actual typical performance over full supply range.

TYPICAL PERFORMANCE CHARACTERISTICS

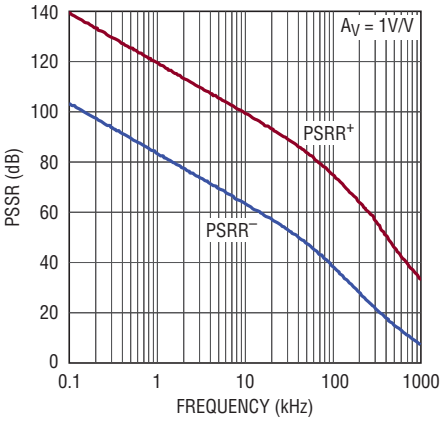
Open-Loop Gain and Phase vs Frequency



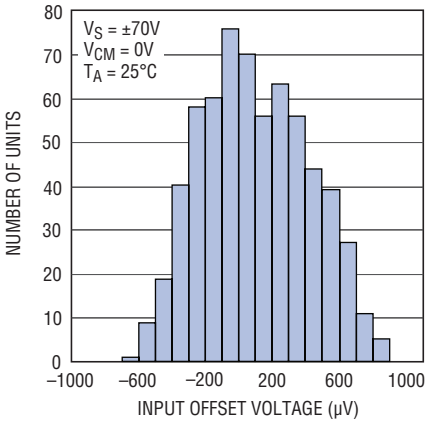
CMRR vs Frequency



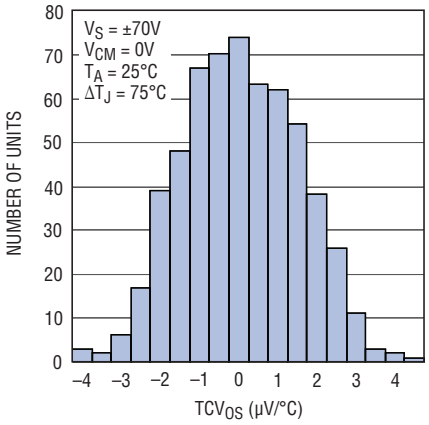
PSRR vs Frequency



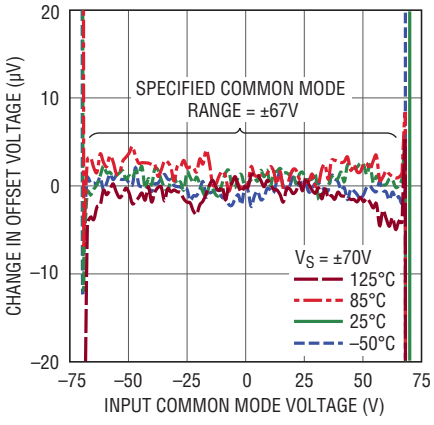
Offset Voltage Distribution



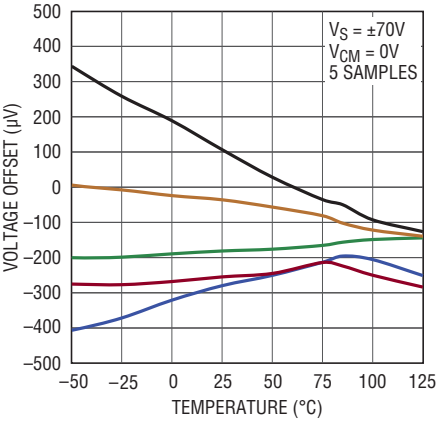
Offset Voltage Drift Distribution



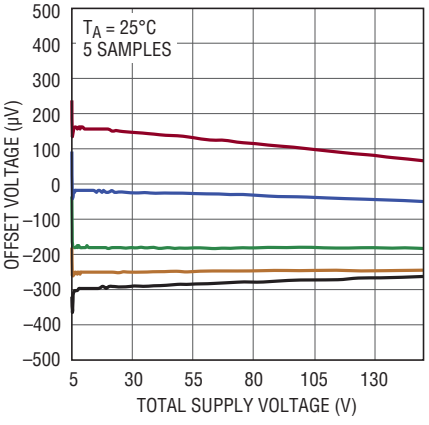
Change in Offset Voltage vs Input Common Mode Voltage



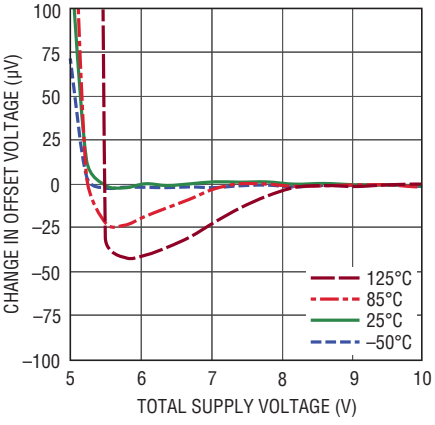
Offset Voltage vs Temperature



Offset Voltage vs Total Supply Voltage

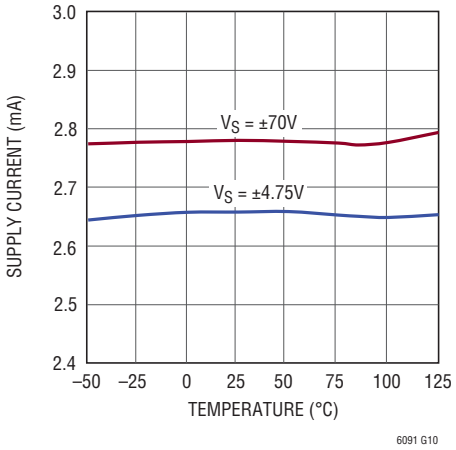


Minimum Supply Voltage

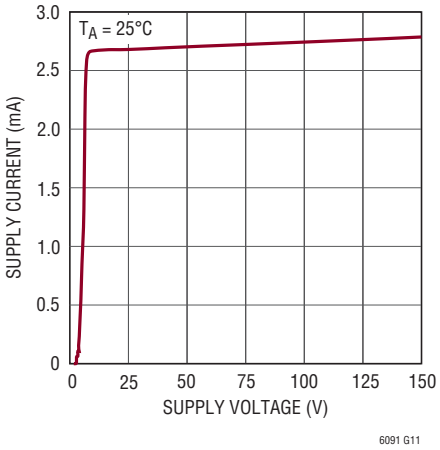


TYPICAL PERFORMANCE CHARACTERISTICS

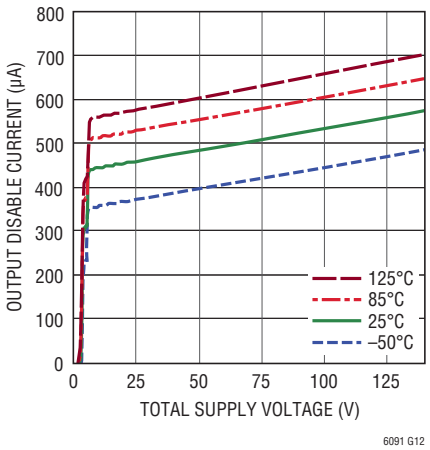
Supply Current vs Temperature



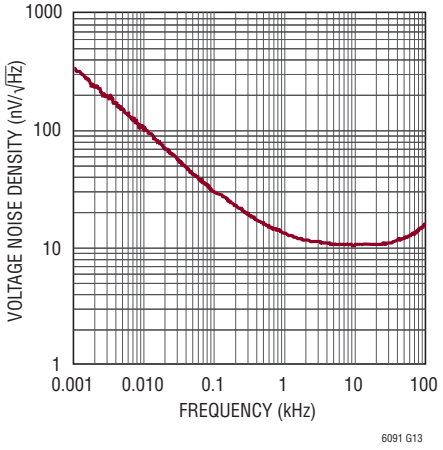
Supply Current vs Supply Voltage



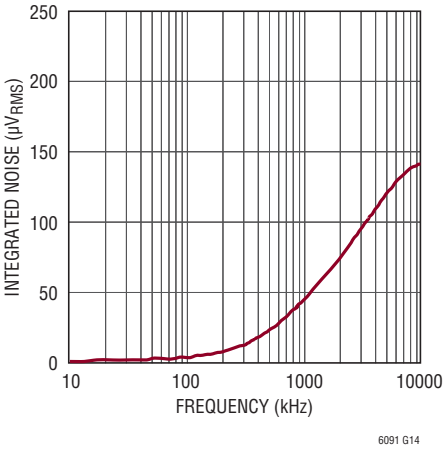
Output Disable Supply Current vs Supply Voltage



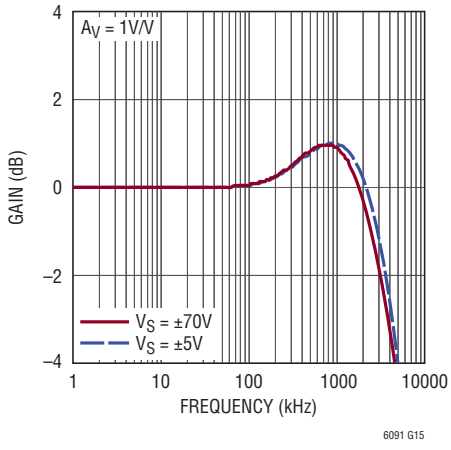
Voltage Noise Density vs Frequency



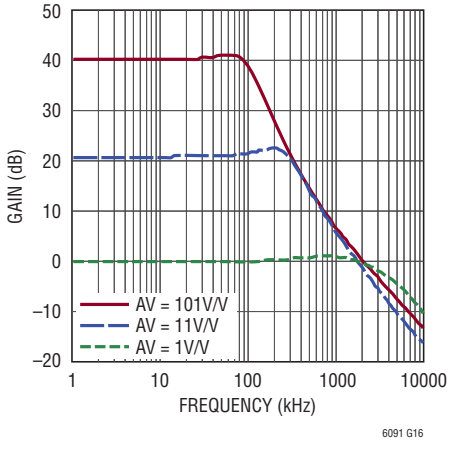
Integrated Noise vs Frequency



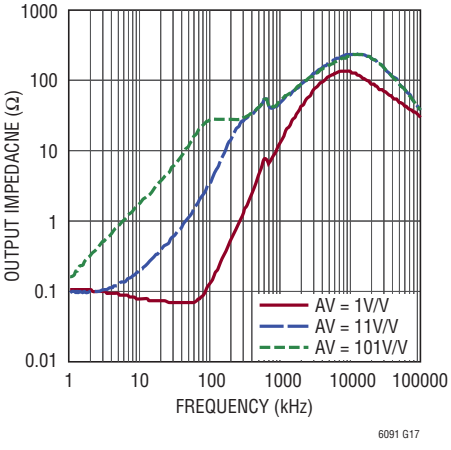
Small-Signal Frequency Response



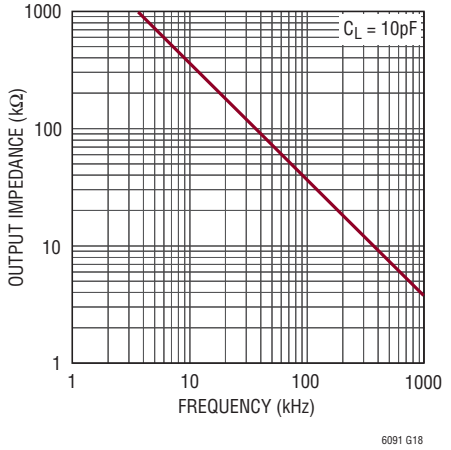
Small-Signal Frequency Response vs Closed-Loop Gain



Output Impedance vs Frequency

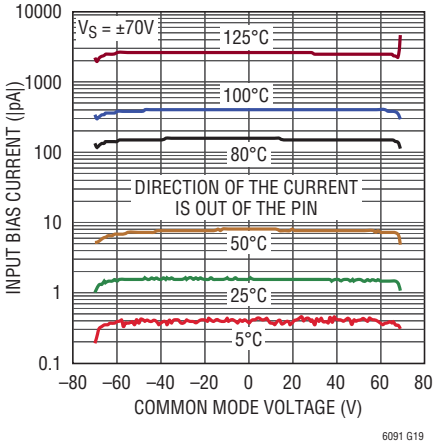


Output Impedance vs Frequency with Output Disabled ($\overline{OD}$ = COM)

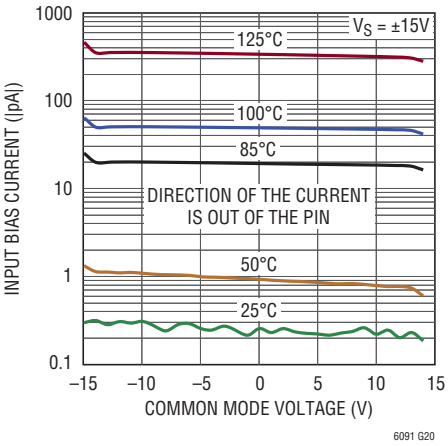


TYPICAL PERFORMANCE CHARACTERISTICS

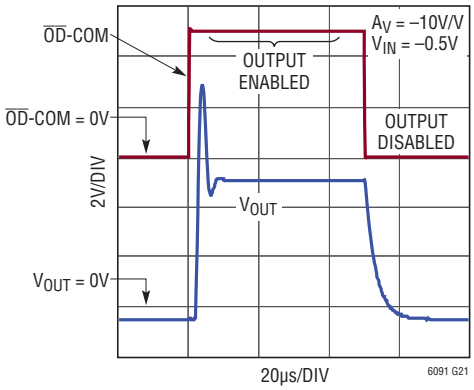
Input Bias Current vs Common Mode Voltage and Temperature (V_S = ±70V)



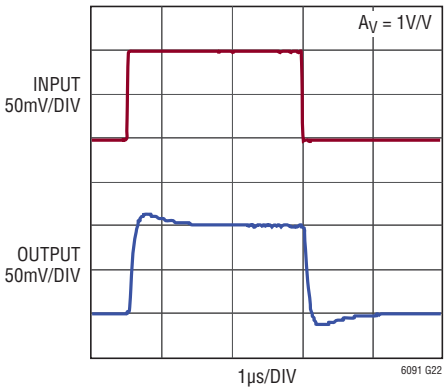
Input Bias Current vs Common Mode Voltage and Temperature (V_S = ±15V)



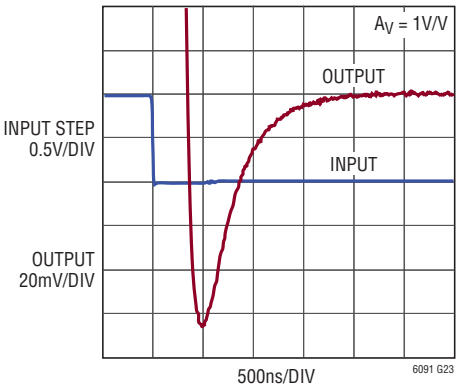
Output Disable ($\overline{OD}$) Response Time



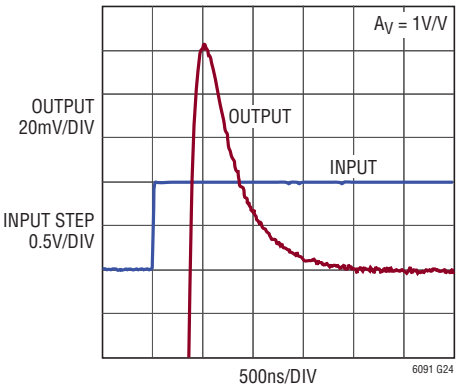
Small-Signal Transient Response



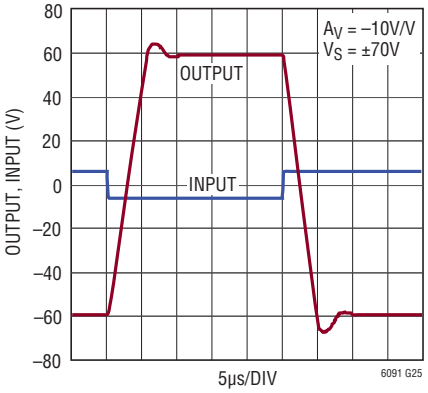
Falling Edge Settling Time



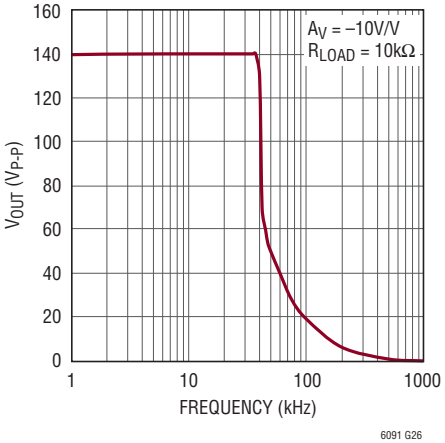
Rising Edge Settling Time



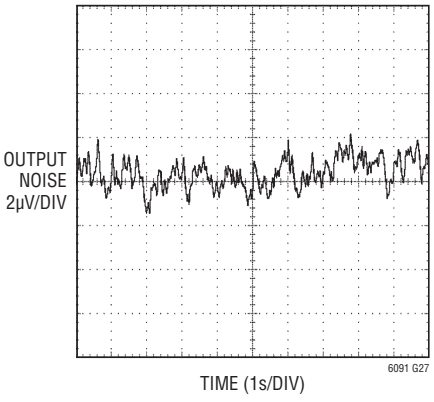
Large-Signal Transient Response



Output Voltage Swing vs Frequency

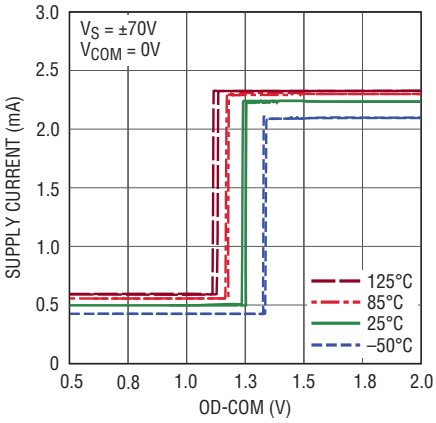


0.1Hz to 10Hz Voltage Noise



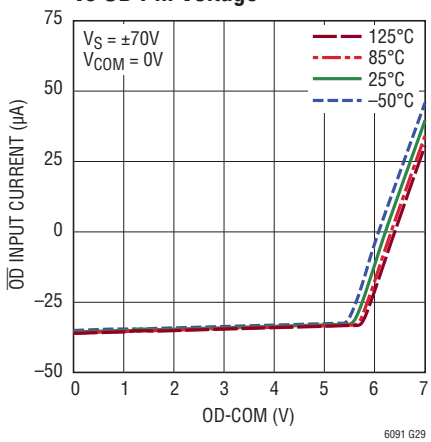
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs $\overline{OD}$ Pin Voltage



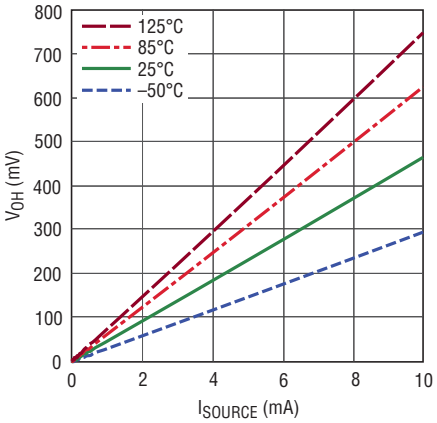
6091 G28

$\overline{OD}$ Pin Input Current vs $\overline{OD}$ Pin Voltage



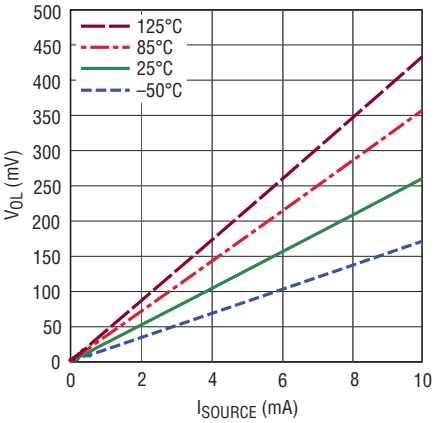
6091 G29

Output Voltage Swing High (V_{OH}) vs Load Current and Temperature



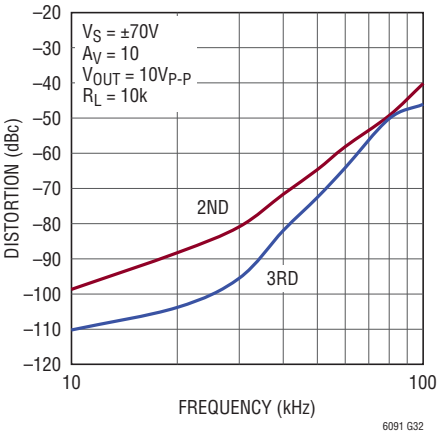
6091 G30

Output Voltage Swing Low (V_{OL}) vs Load Current and Temperature



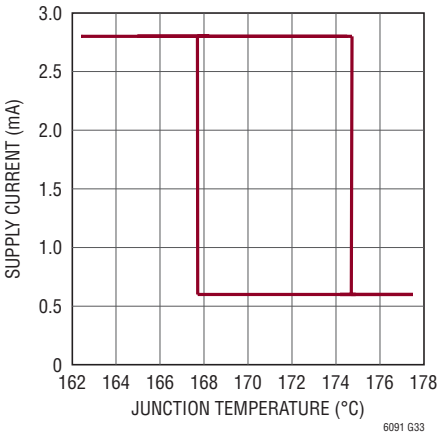
6091 G31

Distortion vs Frequency



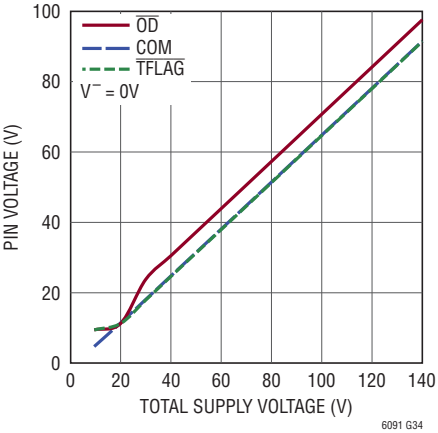
6091 G32

Thermal Shutdown Hysteresis



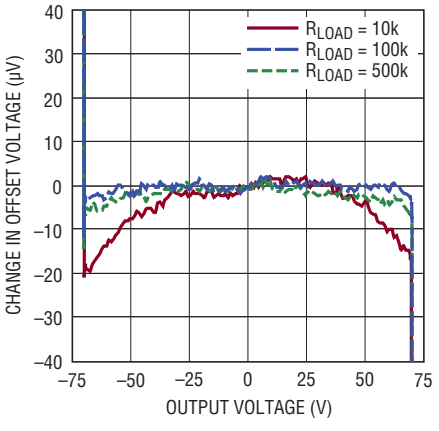
6091 G33

Open-Circuit Voltage of COM, $\overline{OD}$, $\overline{TFLAG}$



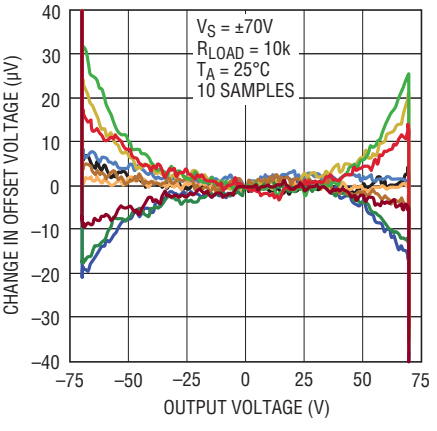
6091 G34

Open-Loop Gain vs Load Resistance



6091 G35

Open-Loop Gain



6091 G36

PIN FUNCTIONS (A Channel/B Channel)

–INA , –INB (Pin 1/Pin 5): Inverting Input Pin. Input common mode range is V^- + 3V to V^+ – 3V. Do not exceed absolute maximum voltage range.

+INA, +INB (Pin 2/Pin 6): Noninverting Input Pin. Input common mode range is V^- + 3V to V^+ – 3V. Do not exceed absolute maximum voltage range.

V^- (Pin 3, Pin 7, Exposed Pad Pin 17): Negative Supply Pin. Connect to a single V^- only. Both amplifiers share a common substrate, and are not isolated from each other. Pins 3, and 7 must be electrically tied to the exposed pad (Pin 17). The exposed pad connection removes heat from the device. To achieve a low thermal resistance, connect the exposed pad to a V^- power plane with as much metal land as possible (see Applications Information).

$\overline{\text{TFLAGA}}$, $\overline{\text{TFLAGB}}$ (Pin 12/ Pin 8): Temperature Flag Pin. The TFLAG pin is an open-drain output that sinks current when the die temperature exceeds 145°C.

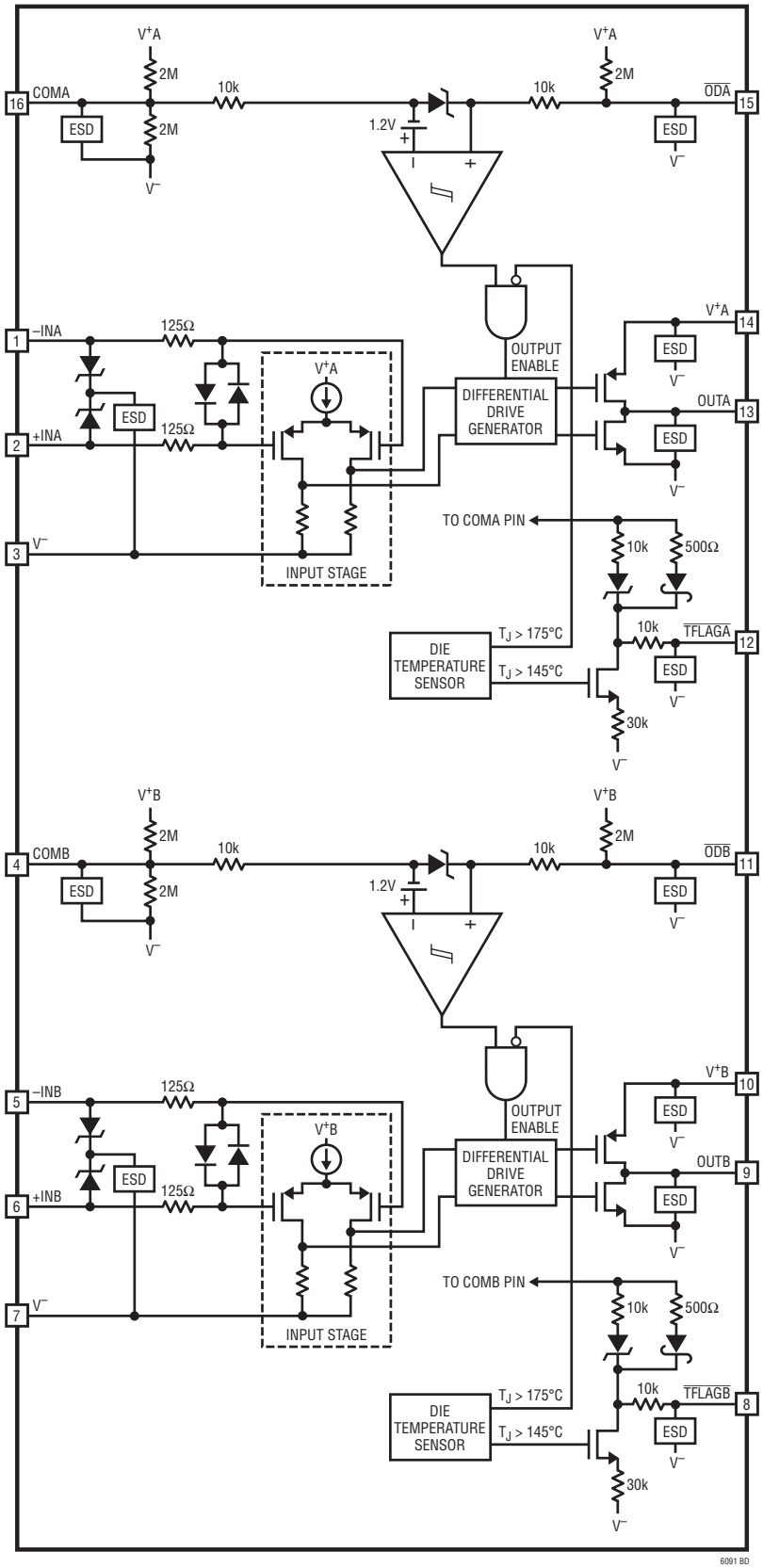
OUTA, OUTB (Pin 13/Pin 9): Output Pin. If this rail-to-rail output goes below V^- , the ESD protection diode will forward bias. If OUT goes above V^+, then output device diodes will forward bias. Avoid forward biasing the diodes on the OUT pin. Excessive current can cause damage.

V^+A, V^+B (Pin 14/Pin 10): Positive Supply Pin. Each amplifier has an independent V^+ supply. But since both amplifiers shares a common substrate, they must share the same V^- supply.

$\overline{\text{ODA}}$, $\overline{\text{ODB}}$ (Pin 15/Pin 11): Output Disable Pin. Active low input disables the output stage. If left open, an internal pull-up resistor enables the amplifier. Input voltage levels are referred to the COM pin.

COMA, COMB (Pin 16/Pin 4): COM Pin is used to interface $\overline{\text{OD}}$ and $\overline{\text{TFLAG}}$ pins to voltage control circuits. Tie this pin to the low voltage ground, or let it float.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

General

The LTC6091 dual high voltage operational amplifier is designed in a Linear Technology proprietary CMOS process enabling a rail-to-rail output stage with a 140V supply while maintaining precision, low offset, low offset drift and low noise.

Power Supply

The LTC6091 consists of single monolithic die containing two LTC6090 amplifiers assembled in a single exposed-pad QFN package. Since both amplifiers share the same substrate, V^- pins (Pin 3 and Pin 7) must be tied together and to the exposed pad underneath. The V^+A (Pin 14) and V^+B (Pin 10) may be supplied independently. The LTC6091 works off single or split supplies. Split supplies can be balanced or unbalanced. For example, two ±70V supplies can be used, or a 100V and –40V supply can be used. The V+ and V– pins should be bypassed with high quality surface mount ceramic capacitors. See Board Layout section for recommendations. When using split supplies, supply sequencing does not cause problems.

Input Protection

As shown in the Block Diagram, the LTC6091 has a comprehensive protection network to prevent damage to the input devices. The current limiting resistors and back-to-back diodes are to keep the inputs from being driven apart. The voltage-current relationship is that of a resistor in series with a diode until the voltage difference between the pins reaches 12V. At that point the Zener diodes turn on. Any additional current into the pins will snap back the input differential voltage to 9V.

In the event of an ESD strike between an input and V^-, the voltage clamps and ESD device fire providing a current path to V^- protecting the input devices. The input pin protection is designed to protect against momentary ESD events. A repetitive large fast input swing (>5.5V and <20ns rise time) will cause repeated stress on the MOSFET input devices. When in such an application, anti-parallel diodes (1N4148) should be connected between the inputs to limit the swing.

Output Disable

Each amplifier of the LTC6091 has its own output disable ($\overline{OD}$) pin (Refer to Figure 1). The $\overline{OD}$ pin is an active low disable with an internal 2M resistor that will pull up the $\overline{OD}$ pin enabling the output stage. The $\overline{OD}$ pin voltage is limited by an internal Zener diode tied between COM and $\overline{OD}$. When the $\overline{OD}$ pin for a particular channel is asserted low with respect to its COM pin, the output stage for that channel is disabled, leaving its bias and input circuits enabled. This results in 580µA (typical) standby current for

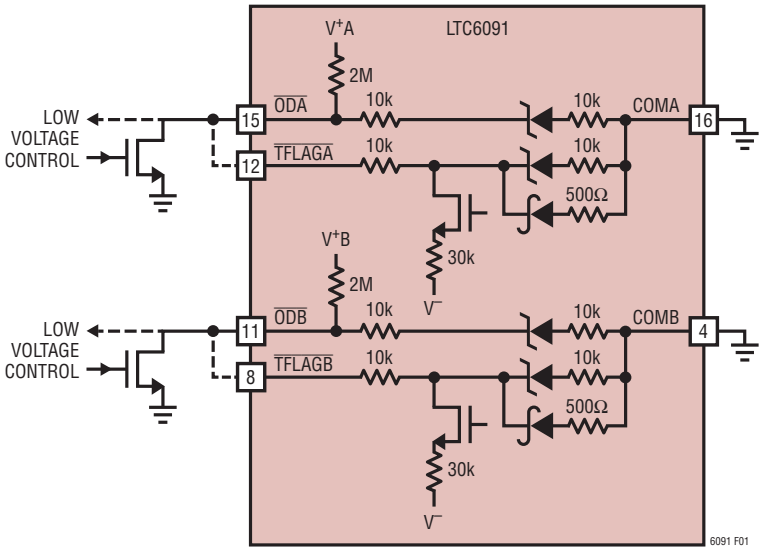


Figure 1. Low Voltage Interface Example for Output Disable

APPLICATIONS INFORMATION

the disabled channel. The $\overline{OD}$ pin can be directly connected to either an open drain NMOS device (as in Figure 1) or connected to low voltage logic circuitry.

Since the $\overline{OD}$ pin is referenced to the COM pin, absolute maximum ratings should be observed for the COM and $\overline{OD}$ pins. When coming out of shutdown the LTC6091 bias circuits and input stage are already powered up leaving only the output stage to turn on and drive to the proper output voltage. Figures 2 and 3 illustrate the part powering on and coming out of shutdown, respectively.

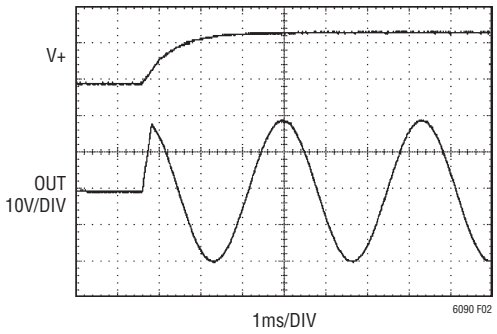


Figure 2. Starting Up

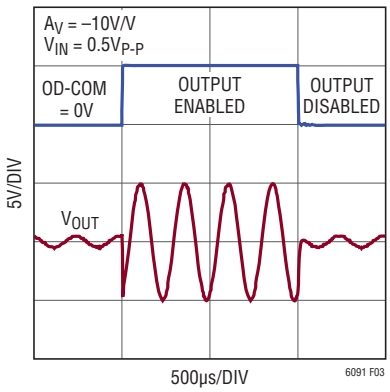


Figure 3. LTC6091 Output Disable Function

Thermal Shutdown

Each amplifier of the LTC6091 has its own trimmed temperature sensing circuit which senses die temperature in close proximity to their respective amplifier's output stage, where most of the on-chip power dissipation occurs. When one of the amplifiers's sensing circuit senses temperatures in excess of approximately 145°C, it will assert the $\overline{TFLAG}$ pin for that amplifier. The $\overline{TFLAG}$ pin is an open-drain output pin that sinks 200µA (typical) when asserted. The temperature sensor itself has approximately 5°C of hysteresis requiring the part to cool to approximately 140°C before disabling $\overline{TFLAG}$.

To guarantee proper operation of thermal shutdown, a few precautions must be followed when interfacing the output disable pin ($\overline{OD}$) to the $\overline{TFLAG}$ pin:

- For simplest operation, float both channel's COM pins (COMA and COMB), and connect $\overline{ODA}$ to $\overline{TFLAGA}$, and $\overline{ODB}$ to $\overline{TFLAGB}$ as shown in Figure 4. Both output stages will be safely disabled should the die temperature reach approximately 145°C. Both COM pins may be tied to ground in this configuration so long as V^- is biased more negatively than –3V with respect to ground for proper thermal shutdown operation.
- In the case where the COM pins are grounded, and the V^- supply is within 0V to –3V of ground, logic buffers must be used to force $\overline{ODA}$ or $\overline{ODB}$ to a logic low as shown in Figure 5. The pull-up resistor (R_{PULLUP}) of Figure 5 must be chosen large enough to guarantee a logic low for the logic buffer. For most CMOS, this requires at least 402k of pull-up resistance. Alternatively, the logic buffer is not needed if you float both COMA and COMB. With COM floating, you may simply tie the respective channel's $\overline{OD}$ directly to $\overline{TFLAG}$ for proper thermal shutdown operation.

Since both amplifiers share a common substrate, thermal cross coupling from one channel to the other will occur. Depending on the average die temperature, and temperature sensing accuracy, it is possible, however unlikely, for heat generated in Channel A's output stage to assert Channel B's $\overline{TFLAGB}$ or visa-versa. Should this condition occur, it should be understood that both amplifiers are operating close to their thermal shutdown limit.

Since the $\overline{TFLAG}$ pin is referenced to the COM pin, absolute maximum ratings should be observed for the COM and $\overline{TFLAG}$ pins.

For safety, a second overtemperature threshold shuts down the output stage if internal die temperatures rise to approximately 175°C. This second overtemperature indicator has approximately 7°C of hysteresis requiring the

APPLICATIONS INFORMATION

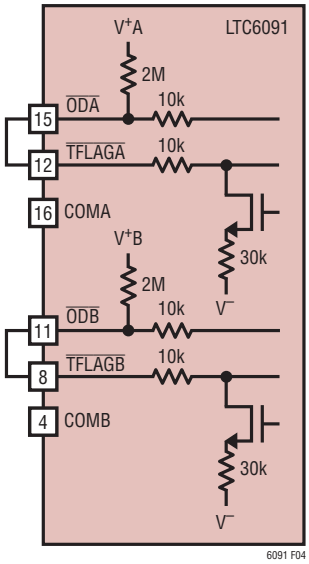


Figure 4. Automatic Thermal Output Disable Using the $\overline{\text{TFLAG}}$ Pins

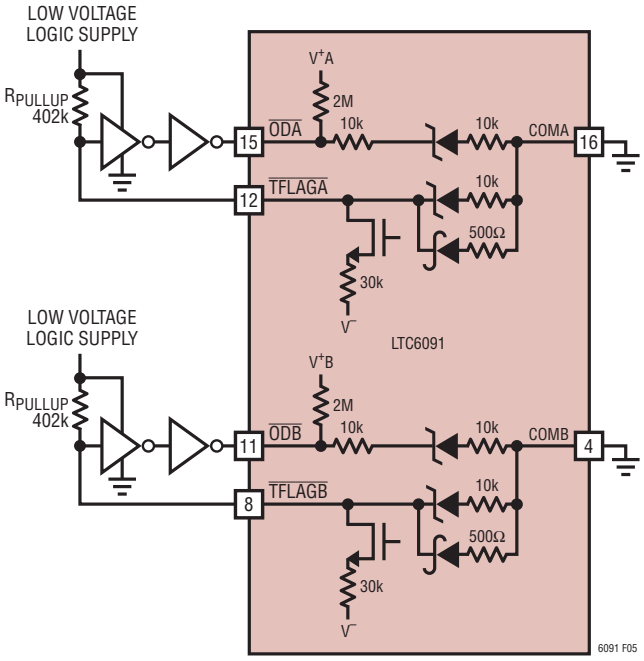


Figure 5. Automatic Thermal Output Disable Using the TFLAG Pin with Unbalanced Split Supply or Single Supply Applications

die temperature to cool 7°C. Once the device has cooled sufficiently, the output stage will enable. **Degradation can occur or reliability may be affected when the junction temperature of the device exceeds 150°C.**

Board Layout

Because the two amplifiers share a common substrate, a single bypass capacitor of 0.1µF can be used to bypass the V^- (as close to the pins as possible) to a low impedance ground plane. Additional bypass capacitance may be required for heavy loads. For the positive supplies, there are two independent positive supply pins (V^+A, V^+B): one for each amplifier. If these two supplies are tied together, they may be bypassed to a low impedance ground plane with a single capacitor (typically 0.1µF) as close to the supply pins as possible. Likewise, when driving heavy loads, additional bypass capacitance may be required.

There are other important considerations for high voltage and high power: trace spacing, humidity and dust. High voltage electric fields between adjacent conductors attract dust. Moisture absorbed by dust can contribute to PCB leakage and electrical breakdown. Vias biased to high voltage should have additional spacing to nearby ground plane.

PCB leakage related errors require special layout and cleaning practices. As little as 1000GΩ of PCB leakage between Pin 2 (+INA) and Pin 3 (V^-) will generate 70pA of leakage with ±70V power supplies! It becomes important to clean the PCB after soldering down the part. Solder flux will accumulate dust and become a leakage hazard. It is recommended to clean the PCB with a solvent, or simply use soap and water to remove residue. Baking the PCB will remove leftover moisture. Depending on the application, a special low leakage board material may be considered. Also guarding sensitive traces as shown in Figures 6 and 7 to the greatest extent possible will also help to mitigate PCB leakage.

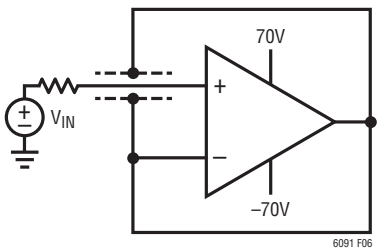


Figure 6. Example of a Noninverting Amplifier Guard Configuration

APPLICATIONS INFORMATION

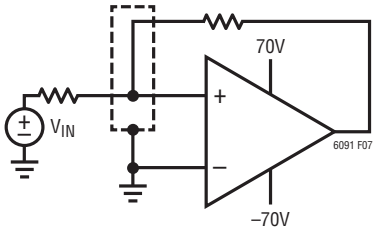


Figure 7. Example of an Inverting Amplifier Guard Configuration

Power Dissipation and Thermal Considerations

In order to avoid damaging the device, the absolute maximum junction temperature of the LTC6091 (T_{JMAX} = 150°C), should not be exceeded. At 5.6mA of quiescent supply current on ±70V supplies, the LTC6091 will consume approximately 0.8W.

In general, the die's junction temperature (T_J) can be estimated from the ambient temperature T_A, and the power dissipated in the device P_D:

$$T_J = T_A + P_D \bullet (\theta_{JC} + \theta_{CA})$$

θ_{JC} is the junction-to-case thermal resistance and is characterized to be approximately 15°C/W. θ_{CA} is the case-to-ambient thermal resistance and depends on circuit board layout, air flow and proximity to other sources of heat. The power dissipated in the IC is a function of supply voltage and the load being driven. Assuming split supplies, and a resistive load, the worst-case power dissipation $P_{D(MAX)}$ occurs when the output is driving the load to half of either supply voltage. $P_{D(MAX)}$, then is the sum of the quiescent power plus the power dissipated in the device due to the load with symmetric supply:

$$P_{D(MAX)} \text{ (per amplifier)} = (V_S \bullet I_S) + (V_S/4)^2/R_{LOAD}$$

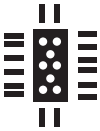
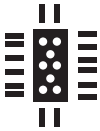
(I_S is the quiescent supply current for a single amplifier)

For example, the resulting peak power dissipation in the LTC6091 for 2 channels driving 5kΩ to ground with a ±70V supply would be approximately 1.3W.

The exposed pad under the LTC6091 is the primary conduit for conducting heat out of the package. Junction-to-ambient thermal resistance is strongly influenced by the number of thermal vias to which the exposed pad is soldered to, the size of the thermal plane connected to these thermal vias, PCB thickness, air-flow, and proximity of other sources of heat. To minimize the amount of temperature rise within the package, the exposed pad must be soldered down to a PCB with multiple thermal vias tied to a thermal plane.

For a 4-layer PCB with the exposed pad of the LTC6091 soldered to a land pattern containing eight 10mil diameter thermal vias which are connected to two 2 inch by 2 inch V^- thermal/power planes, the junction-to-ambient thermal resistance may be as low as 38°C/W in still air. If the density of the PCB layout makes such large thermal

Table 1. Thermal Resistance vs PCB Thermal Plane Area

EXAMPLE A	EXAMPLE B	EXAMPLE C	EXAMPLE D
TOP LAYER A	TOP LAYER B	TOP LAYER C	TOP LAYER D
			
BOTTOM LAYER A	BOTTOM LAYER B	BOTTOM LAYER C	BOTTOM LAYER D
			
θ_{JA} = 90°C/W θ_{JC} = 15°C/W θ_{CA} = 75°C/W	θ_{JA} = 100°C/W θ_{JC} = 15°C/W θ_{CA} = 85°C/W	θ_{JA} = 108°C/W θ_{JC} = 15°C/W θ_{CA} = 93°C/W	θ_{JA} = 115°C/W θ_{JC} = 15°C/W θ_{CA} = 100°C/W

6091 TABLE 1

APPLICATIONS INFORMATION

planes impractical, Table 1 lists the thermal performance achieved of alternative layout examples. A minimally sized single layer thermal land under the device as shown in column D of Table 1 will result in a junction-to-ambient thermal resistance approaching 115°C/W. Since the LTC6091 will dissipate 0.8W on ±70V supplies, there will be approximately 90°C of junction-to-ambient temperature rise due to the device operation alone. This will then limit the specified ambient temperature range of the LTC6091 can operate and/or will limit the load driven to prevent junction temperatures from exceeding T_{JMAX} (150°C).

Stability with Large Resistor Values

A large feedback resistor along with the intrinsic input capacitance will create an additional pole that affects stability and causes peaking in the closed-loop response. To mitigate the peaking a small feedback capacitor placed around the feedback resistor, as shown in Figure 8, will reduce the peaking and overshoot. Figure 9 shows the closed-loop response with various feedback capacitors.

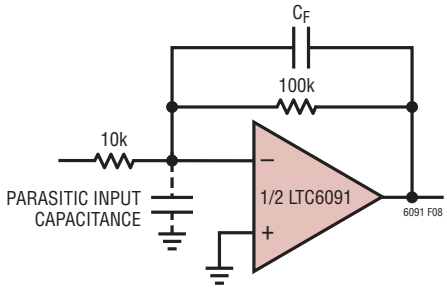


Figure 8. LTC6091 with Feedback Capacitance to Reduce Peaking

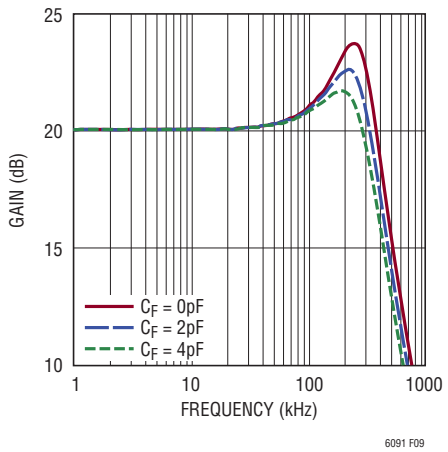


Figure 9. Compensated Closed-Loop Response Reduces Peaking

Additional stray capacitance on the input pins should be kept to a minimum.

Slew Enhancement

The LTC6091 includes a slew enhancement circuit which boosts the slew rate to 21V/µs making the part capable of slewing rail-to-rail across the 140V output range in less than 7µs. To optimize the slew rate and minimize settling time, stray capacitance should be kept to a minimum. A feedback capacitor reduces overshoot and nonlinearities associated with the slew enhancement circuit. The size of the feedback capacitor should be tailored to the specific board, supply voltage and load conditions.

Slewing is a nonlinear behavior and will affect distortion. The relationship between slew rate and full-power bandwidth is given in the relationship below.

$$SR = V_{PEAK} \bullet \omega$$

where V_{PEAK} is the peak output voltage and ω is frequency in radians/sec. The fidelity of a large sine wave output is limited by the slew rate. The graph in Figure 10 shows distortion versus frequency for several output levels.

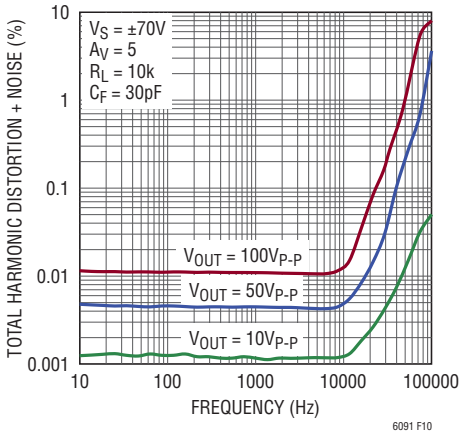


Figure 10. Distortion vs Frequency for Large Output Swings

APPLICATIONS INFORMATION

Multiplexer Application

A single LTC6091 may be arranged to act as a 2-channel high voltage analog multiplexer as shown in Figure 11. When used in this arrangement, it is possible for the output to affect the source on the disabled amplifier's noninverting input. The inverting and noninverting inputs are clamped through resistors and back-to-back diodes. There is a path for current to flow from the multiplexer output through the disabled amplifier's feedback resistor, and through the inputs to the noninverting input's source. For example, if the enabled amplifier has a –70V output, and the disabled amplifier has a 5V input, there is 75V across the two resistors and the input pins. To keep this current below 1mA the combined resistance of the R_{IN} and feedback resistor needs to be about 75k or higher.

The output impedance of the disabled amplifier is > 10MΩ at DC. The AC output impedance is shown in the Typical Performance Characteristics section.

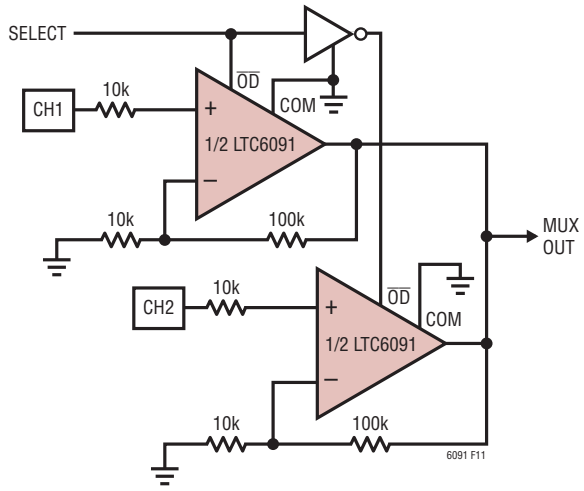


Figure 11. Multiplexer Application

Minimizing Noise

The LTC6091 circuit shown in Figure 12 includes an output filter that reduces noise (and signals) starting at about 150kHz. This filtering reduces out-of-band noise to a relatively insignificant level. Loop compensation is included to provide a well-stabilized overall response. Since the large-signal bandwidth is dictated largely by the op amp slew rate to signals below about 100kHz, the net result is that little is compromised due to the added filtration.

The following table shows the suggested component values for a range of amplification factors.

GAIN	R_G	R_F	C_F
1	N/A	4.99k	330pF
2	50k	50k	33pF
5	20k	80.6k	22pF
10	11k	100k	18pF
20	5.23k	100k	18pF
50	2.05k	100k	18pF
100	1k	100k	18pF

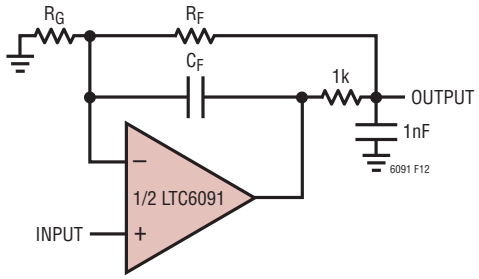
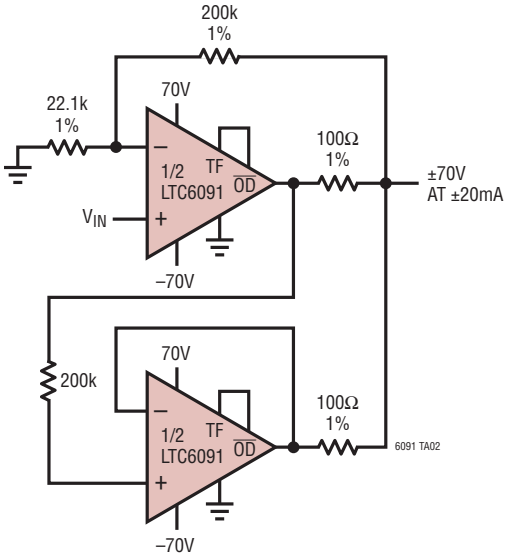


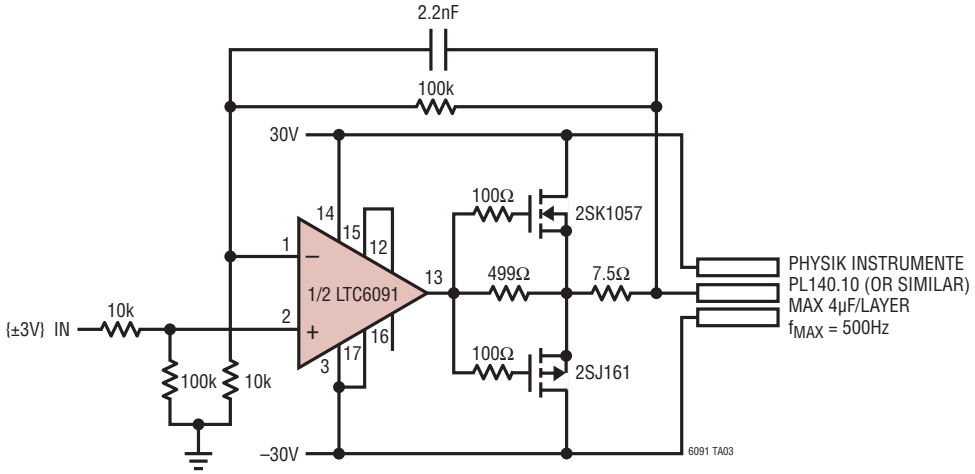
Figure 12. Modified Gain-Block Application That Includes Noise-Reducing Filter

TYPICAL APPLICATIONS

Gain of 10 with Protected Output Current Doubler

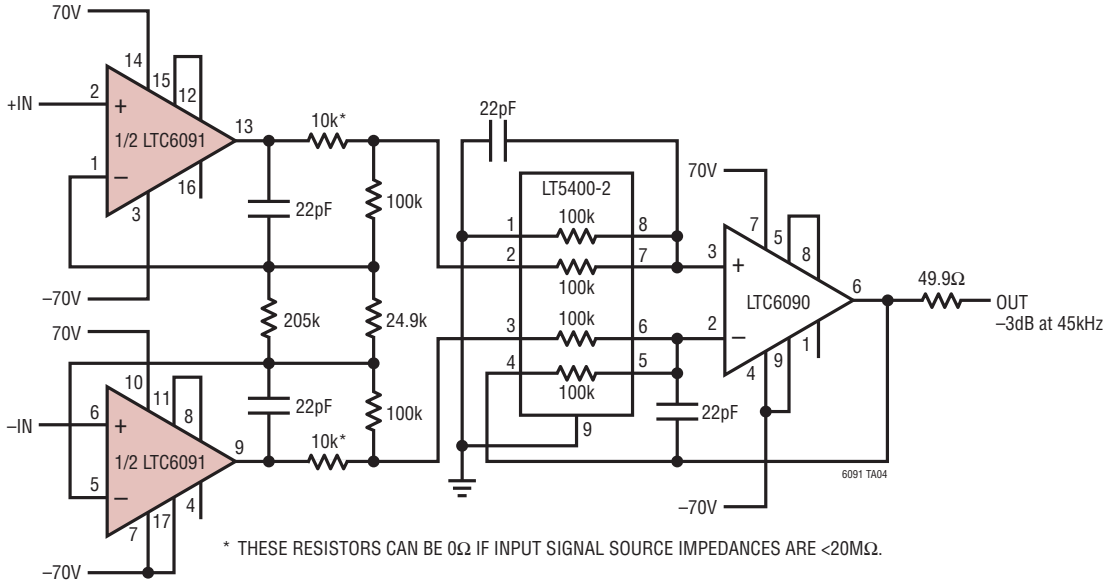


Piezo Bimorph Bender Driver

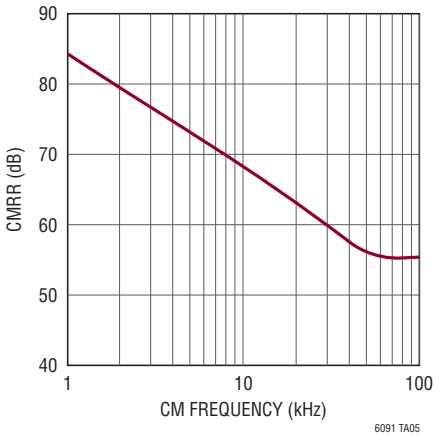


TYPICAL APPLICATIONS

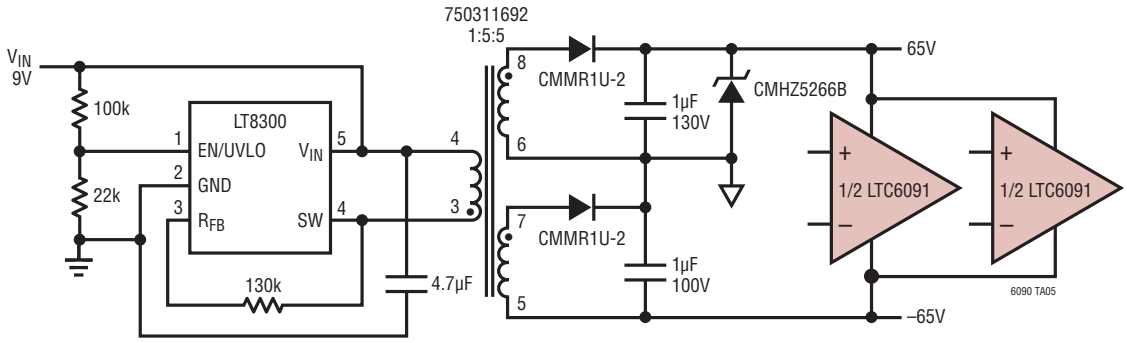
Wide Common Mode Range 10x Gain Instrumentation Amplifier
Typically <1mV Input-Referred Error



* THESE RESISTORS CAN BE 0Ω IF INPUT SIGNAL SOURCE IMPEDANCES ARE <20MΩ.



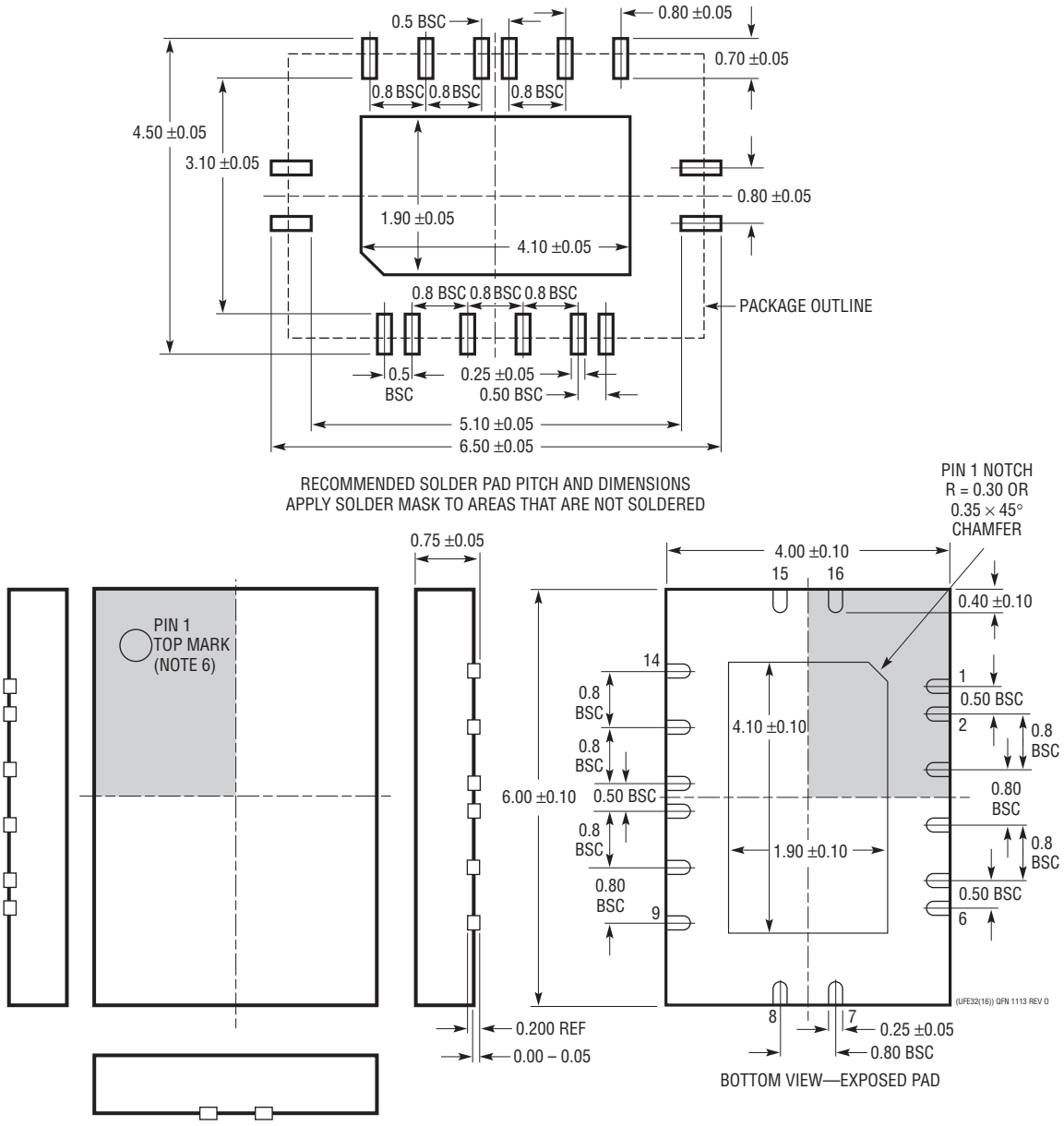
9V to ±65V Isolated Flyback Converter for Amplifier Supply



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

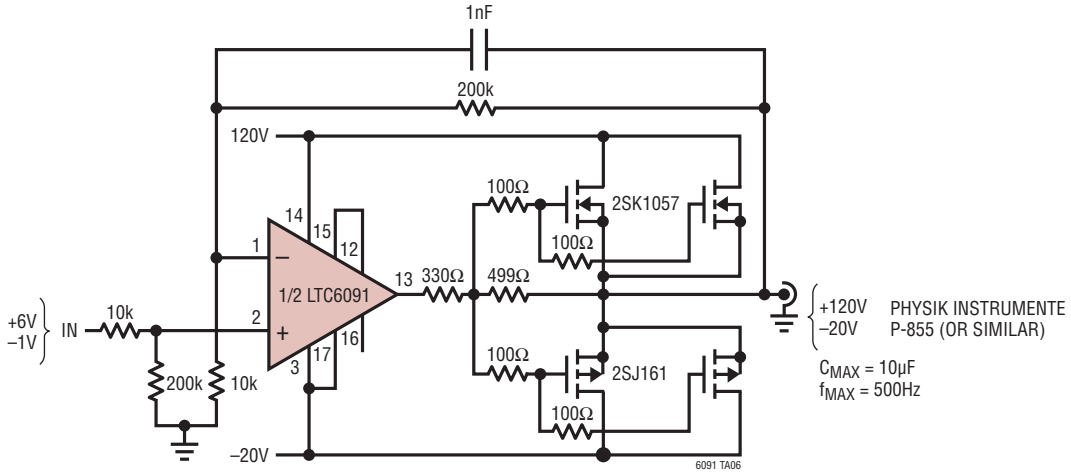
UFE Package
32(16)-Lead Plastic QFN (4mm × 6mm)
(Reference LTC DWG # 05-08-1966 Rev O)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Piezo Micropositioner Driver



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC6090	Single 140V Rail-to-Rail Output pA Input Op Amp	Single Version of LTC6091
LT®1990	250V Input Range G = 1, 10, Micropower, Difference Amplifier	Pin Selectable Gain of 1 or 10
LT1991	Precision, 100µA Gain Selectable Amplifier	Pin Configurable as a Difference Amplifier, Inverting and Noninverting Amplifier
LT6015/LT6016/ LT6017	Single/Dual/Quad 3.2MHz, Low Power, Over-The-Top® Precision Op Amp	76V Common Mode Input Range, 50V Operating Supply Range, 50µV Voltage Offset
LT3511	Monolithic High Voltage Isolated Flyback Converter	4.5V to 100V Input Voltage Range, No Opto-Coupler Required
LT8300	$100V_{IN}$ Micropower Isolated Flyback Converter with 150V/260mA Switch	6V to 100V Input Voltage Range. V_{OUT} Set with a Single External Resistor

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