Kintex UltraScale Architecture Data Sheet: DC and AC Switching Characteristics

DS892 (v1.0) December 10, 2013 **Advance Product Specification**

Summary

The Xilinx® Kintex® UltraScale™ FPGAs are available in -3, -2, -1, and -1L speed grades, with -3 having the highest performance. The -1L devices can operate at either of two V_{CCINT} voltages, 0.95V and 0.90V and are screened for lower maximum static power. When operated at V_{CCINT} = 0.95V, the speed specification of a -1L device is the same as the -1 speed grade. When operated at V_{CCINT} = 0.90V, the -1L performance and static and dynamic power is reduced.

DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the UltraScale architecture-based devices, is available on the Xilinx website at www.xilinx.com/ultrascale.

DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.500	1.100	V
V_{CCINT_IO}(2)	Internal supply voltage for the I/O banks	–0.500	1.100	V
V_{CCAUX}	Auxiliary supply voltage	–0.500	2.000	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.500	1.100	V
V_{CCO}	Output drivers supply voltage for 3.3V HR I/O banks	–0.500	3.400	V
	Output drivers supply voltage for 1.8V HP I/O banks	–0.500	2.000	V
V_{CCAUX_IO}(3)	Auxiliary supply voltage for the I/O banks	–0.500	2.000	V
V_{REF}	Input reference voltage	–0.500	2.000	V
V_{IN}(4)(6)(7)	I/O input voltage for 3.3V HR I/O banks(5)	–0.400	V_{CCO} + 0.550	V
	I/O input voltage for 1.8V HP I/O banks	–0.550	V_{CCO} + 0.550	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8)	–0.400	2.625	V

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{BATT}	Key memory battery backup supply	–0.500	2.000	V
GTH Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTH transmitter and receiver circuits	–0.500	1.100	V
$V_{MGTAVTT}$	Analog supply voltage for the GTH transmitter and receiver termination circuits	–0.500	1.320	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTH transceivers	–0.500	1.935	V
$V_{MGTREFCLK}$	GTH transceiver reference clock absolute input voltage	–0.500	1.320	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTH transceiver column	–0.500	1.320	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.500	1.260	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–		mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–		mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–		mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–		mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–		mA
System Monitor				
V_{CCADC}	System Monitor supply relative to GNDADC	–0.500	2.000	V
V_{REFP}	System Monitor reference input relative to GNDADC	–0.500	2.000	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature(9)	–	260	°C
T_j	Maximum junction temperature(9)	–	125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. V_{CCINT_IO} can be connected to V_{CCINT}.
3. V_{CCAUX_IO} can be connected to V_{CCAUX}.
4. The lower absolute voltage specification always applies.
5. If V_{CCO} is 3.3V, the maximum voltage is 3.4V.
6. For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
7. The maximum limit applied to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
8. See Table 10 for TMDS_33 specifications.
9. For soldering guidelines and thermal considerations, see the *UltraScale Architecture Packaging and Pinout Specifications* (UG575).

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage	0.922	0.950	0.979	V
	For -1L (0.90V) devices: internal supply voltage	0.873	0.900	0.927	V
	For -3 (1.0V only) devices: Internal supply voltage	0.970	1.000	1.030	V
V_{CCINT_IO}(3)	Internal supply voltage for the I/O banks	0.922	0.950	0.979	V
	For -1L (0.90V) devices: internal supply voltage for the I/O banks	0.873	0.900	0.927	V
	For -3 (1.0V only) devices: internal supply voltage for the I/O banks	0.970	1.000	1.030	V
V_{CCBRAM}	Block RAM supply voltage	0.922	0.950	0.979	V
	For -3 (1.0V only) devices: block RAM supply voltage	0.970	1.000	1.030	V
V_{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V
V_{CCO}(4)(5)	Supply voltage for 3.3V HR I/O banks	1.140	–	3.400	V
	Supply voltage for 1.8V HP I/O banks	0.950	–	1.890	V
V_{CCAUX_IO}(6)	Auxiliary I/O supply voltage	1.746	1.800	1.854	V
V_{IN}(7)	I/O input voltage	–0.200	–	V_{CCO} + 0.200	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8).	–	0.400	2.625	V
I_{IN}(9)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10.000	mA
V_{BATT}(10)	Battery voltage	1.000	–	1.890	V
GTH Transceiver					
$V_{MGTAVCC}$(11)	Analog supply voltage for the GTH transceiver	0.970	1.000	1.030	V
$V_{MGTAVTT}$(11)	Analog supply voltage for the GTH transmitter and receiver termination circuits	1.170	1.200	1.230	V
$V_{MGTVCCAUX}$(11)	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V
$V_{MGTAVTTRCAL}$(11)	Analog supply voltage for the resistor calibration circuit of the GTH transceiver column	1.170	1.200	1.230	V
SYSMON					
V_{CCADC}	SYSMON supply relative to GNDADC	1.746	1.800	1.854	V
V_{REFP}	Externally supplied reference voltage	1.200	1.250	1.300	V

Table 2: **Recommended Operating Conditions(1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C

Notes:

1. All voltages are relative to ground.
2. For the design of the power distribution system consult *UltraScale Architecture PCB Design and Pin Planning Guide* (UG583).
3. V_{CCINT_IO} can be connected to V_{CCINT}.
4. Configuration data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HR I/O only) at ±5%, and 3.3V (HR I/O only) at +3/–5%.
6. V_{CCAUX_IO} can be connected to V_{CCAUX}.
7. The lower absolute voltage specification always applies.
8. See Table 10 for TMDS_33 specifications.
9. A total of 200 mA per 52-pin bank should not be exceeded.
10. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.
11. Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)		–	–	V
V_{DRAUX}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)		–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–		µA
I_L	Input or output leakage current per pin (sample-tested)	–	–		µA
C_{IN}(2)	Die input capacitance at the pad	–	–		pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V		–		µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V		–		µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V		–		µA
	Pad pull-down (when selected) at V_{IN} = 1.8V		–		µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–		mA
I_{BATT}(3)	Battery supply current	–	–		nA
R(4)	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 RTT_40				Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 RTT_48				Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 RTT_60				Ω
	Programmable input termination to V_{CCO} RTT_40				Ω
	Programmable input termination to V_{CCO} RTT_48				Ω
	Programmable input termination to V_{CCO} RTT_60				Ω
	Programmable input termination to V_{CCO} RTT_120				Ω
	Programmable input termination to V_{CCO} RTT_240				Ω
n	Temperature diode ideality factor	1.008	1.010	1.012	–
r	Temperature diode series resistance	–	1	2	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. On-die input termination resistance, for more information, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571)

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 3.3V HR I/O Banks(1)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.55			
V_{CCO} + 0.55			
V_{CCO} + 0.55			
V_{CCO} + 0.55			
V_{CCO} + 0.60			
V_{CCO} + 0.65			
V_{CCO} + 0.70			
V_{CCO} + 0.75			
V_{CCO} + 0.80			
V_{CCO} + 0.85			
V_{CCO} + 0.90			
V_{CCO} + 0.95			

Notes:
1. A total of 200 mA per bank should not be exceeded.

Table 5: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for 1.8V HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
V_{CCO} + 0.55			
V_{CCO} + 0.60			
V_{CCO} + 0.65			
V_{CCO} + 0.70			
V_{CCO} + 0.75			
V_{CCO} + 0.80			
V_{CCO} + 0.85			
V_{CCO} + 0.90			
V_{CCO} + 0.95			

Notes:
1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20 µs.

Table 6: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.90V	
			-3	-2	-1/-1L	-1L	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XCKU035					mA
		XCKU040					mA
		XCKU060					mA
		XCKU075					mA
		XCKU100					mA
		XCKU115					mA

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.90V	
			-3	-2	-1 / -1L	-1L	
I_{CCINT_IOQ}	Quiescent current for V_{CCINT_IO} supply	XCKU035					mA
		XCKU040					mA
		XCKU060					mA
		XCKU075					mA
		XCKU100					mA
		XCKU115					mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XCKU035					mA
		XCKU040					mA
		XCKU060					mA
		XCKU075					mA
		XCKU100					mA
		XCKU115					mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XCKU035					mA
		XCKU040					mA
		XCKU060					mA
		XCKU075					mA
		XCKU100					mA
		XCKU115					mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XCKU035					mA
		XCKU040					mA
		XCKU060					mA
		XCKU075					mA
		XCKU100					mA
		XCKU115					mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XCKU035					mA
		XCKU040					mA
		XCKU060					mA
		XCKU075					mA
		XCKU100					mA
		XCKU115					mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. For most designs, operating current exceeds power-on current. The Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) estimates operating current. When the required power-on current exceeds the estimated operating current, XPE can display the power-on current.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCINT_IO}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT}, V_{CCINT_IO}, and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

The recommended power-on sequence to achieve minimum current draw for the GTH transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

When the current minimums are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The device must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

Table 7 shows the power supply ramp time.

Table 7: **Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}	0.2	40	ms
T_{VCCINT_IO}	Ramp time from GND to 90% of V_{CCINT_IO}	0.2	40	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}	0.2	40	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}	0.2	40	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$	0.2	40	ms

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels For HR I/O Banks(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}		
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}		
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450		
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
LVCMOS33	–0.300	0.800	2.000	3.400	0.400	V_{CCO} – 0.400		
LVTTL	–0.300	0.800	2.000	3.400	0.400	2.400		
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150		
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150		
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.150	$V_{CCO}/2$ + 0.150		
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175		
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.175	$V_{CCO}/2$ + 0.175		
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.470	$V_{CCO}/2$ + 0.470		
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	$V_{CCO}/2$ – 0.600	$V_{CCO}/2$ + 0.600		

Notes:

1. Tested according to relevant specifications.
2. For detailed interface specific DC voltage levels, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571)

Table 9: **SelectIO DC Input and Output Levels for HP I/O Banks(1)(2)**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}		
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}		
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400		
LVCMOS15, LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}		
LVCMOS18, LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450		
POD10	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300				
POD12	–0.300	V_{REF} – 0.068	V_{REF} + 0.068	V_{CCO} + 0.300				
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150		
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150		
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175		
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470		

Notes:

1. Tested according to relevant specifications.
2. For detailed interface specific DC voltage levels, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571)

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM} (V)(1)			V_{ID}(V)(2)			V_{OCM}(V)(3)			V_{OD}(V)(4)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
SUB_LVDS_25		0.900		0.070			0.800	0.900	1.000	0.100	0.150	0.200
SUB_LVDS	0.500	0.900	1.300	0.070			0.800	0.900	1.000	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
SLVS_400_18		0.200		0.070			–	–	–	–	–	–
SLVS_400_25		0.200		0.070			–	–	–	–	–	–
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO} – 0.405	V_{CCO} – 0.300	V_{CCO} – 0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 13.
7. LVDS is specified in Table 14.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels for HR I/O Banks**

I/O Standard	V_{ICM} (V)(1)			V_{ID} (V)(2)		V_{OL} (V)(3)	V_{OH} (V)(4)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Max	Min	Max	Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400		
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400		
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400		
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400		
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}		
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150		
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150		
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150		
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175		
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175		
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470		
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600		

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 12: **Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks**

I/O Standard	V_{ICM} (V)(1)			V_{ID} (V)(2)		V_{OL} (V)(3)	V_{OH} (V)(4)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Max	Min	Max	Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400		
DIFF_HSTL_I_12	0.300	0.600	0.850			0.250 x V_{CCO}	0.750 x V_{CCO}		
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400		
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}		
DIFF_POD10									
DIFF_POD12									
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150		
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150		
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175		
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470		

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage.
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 13: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 14: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		1.710	1.800	1.890	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.425	V

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in Table 15.

Table 15: **Speed Specification Version By Device**

2013.4	Device
1.04	XCKU035, XCKU040, XCKU060, XCKU075, XCKU100, XCKU115

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex UltraScale FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 16 correlates the current status of the Kintex UltraScale FPGAs on a per speed grade basis.

Table 16: **Kintex UltraScale FPGAs Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCKU035	-3 (1.0V), -2 (0.95V), -1 (0.95V), -1L (0.95V), and -1L (0.90V)		
XCKU040	-3 (1.0V), -2 (0.95V), -1 (0.95V), -1L (0.95V), and -1L (0.90V)		
XCKU060	-3 (1.0V), -2 (0.95V), -1 (0.95V), -1L (0.95V), and -1L (0.90V)		
XCKU075	-3 (1.0V), -2 (0.95V), -1 (0.95V), -1L (0.95V), and -1L (0.90V)		
XCKU100	-3 (1.0V), -2 (0.95V), -1 (0.95V), -1L (0.95V), and -1L (0.90V)		
XCKU115	-3 (1.0V), -2 (0.95V), -1 (0.95V), -1L (0.95V), and -1L (0.90V)		

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 17 lists the production released Kintex UltraScale FPGAs, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 17: **Kintex UltraScale FPGAs Device Production Software and Speed Specification Release**

Device	Speed Grade Designations			
	1.0V	0.95V		0.90V
	-3E	-2E, -2I	-1C, -1I, -1LI	-1LI
XCKU035				
XCKU040				
XCKU060				
XCKU075				
XCKU100				
XCKU115				

Notes:

1. Blank entries indicate a device and/or speed grade in Advance or Preliminary status.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex UltraScale FPGAs. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 13. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 18: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1/-1L	-1L	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR					Mb/s
	HP					Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR					Mb/s
	HP					Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR					Mb/s
	HP					Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR					Mb/s
	HP					Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 19: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FFV Packages)(1)**

Memory Standard	I/O Bank Type	Speed Grade				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1/-1L	-1L	
4:1 Memory Controllers						
DDR4	HP	2400	2400	2133		Mb/s
DDR3	HP	2133	1866	1866		Mb/s
DDR3L	HP	1866	1866	1600		Mb/s
RLDRAM III	HP	1066	933	933		MHz
2:1 Memory Controllers						
QDR II+(2)	HP	633	600	550		MHz
RLDRAM II	HP	533	515	500		MHz

Notes:

1. V_{REF} tracking is required. For more information, see the *UltraScale Architecture-Based FPGAs Memory Interface Solutions Product Guide* (PG150).
2. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

Table 20: **Maximum Physical Interface (PHY) Rate for Memory Interfaces (FBV Packages)(1)**

Memory Standard	I/O Bank Type	Speed Grade				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1/-1L	-1L	
4:1 Memory Controllers						
DDR4	HP	2133	1866	1866		Mb/s
DDR3	HP	2133	1866	1866		Mb/s
DDR3L	HP	1866	1866	1600		Mb/s
RLDRAM III	HP	1066	933	933		MHz
2:1 Memory Controllers						
QDR II+(2)	HP	633	600	550		MHz
RLDRAM II	HP	533	515	500		MHz

Notes:

1. V_{REF} tracking is required. For more information, see the *UltraScale Architecture-Based FPGAs Memory Interface Solutions Product Guide* (PG150).
2. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

IOB Pad Input, Output, and 3-State

Table 21 (3.3V high-range IOB (HR)) and Table 22 (1.8V high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{INBUF\_DELAY\_PAD\_I}$ is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{OUTBUF\_DELAY\_O\_PAD}$ is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{OUTBUF\_DELAY\_TD\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the on-die termination turn-on time is always faster than $T_{OUTBUF\_DELAY\_TD\_PAD}$ when the INTERMDISABLE pin is used.

Table 21: **3.3V IOB High Range (HR) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1/-1L	-1L	-3	-2	-1/-1L	-1L	-3	-2	-1/-1L	-1L	
BLVDS_25					1.50	1.81	2.09	2.29	1.50	1.81	2.09	2.29	ns
DIFF_HSTL_I_18_F	0.37	0.54	0.56	0.61	0.56	0.66	0.75	0.83	0.82	0.89	0.99	1.09	ns
DIFF_HSTL_I_18_S	0.37	0.54	0.56	0.61	0.61	0.72	0.82	0.90	0.83	0.90	0.99	1.09	ns
DIFF_HSTL_I_F	0.37	0.54	0.56	0.61	0.57	0.68	0.77	0.85	0.75	0.91	1.03	1.13	ns
DIFF_HSTL_I_S	0.37	0.54	0.56	0.61	0.57	0.68	0.77	0.85	0.75	0.91	1.03	1.13	ns
DIFF_HSTL_II_18_F	0.37	0.54	0.56	0.61	0.50	0.59	0.67	0.74	0.87	0.95	1.05	1.15	ns
DIFF_HSTL_II_18_S	0.37	0.54	0.56	0.61	0.56	0.66	0.75	0.82	0.88	0.95	1.05	1.15	ns

Table 21: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
DIFF_HSTL_II_F	0.37	0.54	0.56	0.61	0.57	0.68	0.77	0.85	0.84	0.96	1.03	1.14	ns
DIFF_HSTL_II_S	0.37	0.54	0.56	0.61	0.57	0.68	0.77	0.85	0.84	0.96	1.03	1.14	ns
DIFF_HSUL_12_F	0.37	0.54	0.56	0.61	1.06	1.27	1.46	1.60	0.78	0.84	0.93	1.02	ns
DIFF_HSUL_12_S	0.37	0.54	0.56	0.61	1.06	1.27	1.46	1.60	0.78	0.84	0.93	1.02	ns
DIFF_SSTL12_F	0.37	0.54	0.56	0.61	0.55	0.65	0.75	0.82	0.82	0.97	1.07	1.17	ns
DIFF_SSTL12_S	0.37	0.54	0.56	0.61	0.55	0.65	0.75	0.82	0.82	0.97	1.07	1.17	ns
DIFF_SSTL135_F	0.37	0.54	0.56	0.61	0.51	0.61	0.70	0.77	0.84	0.98	1.07	1.18	ns
DIFF_SSTL135_S	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.86	0.84	0.98	1.07	1.18	ns
DIFF_SSTL135_R_F	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.86	0.84	0.93	0.99	1.09	ns
DIFF_SSTL135_R_S	0.37	0.54	0.56	0.61	0.65	0.77	0.87	0.96	0.83	0.94	1.00	1.11	ns
DIFF_SSTL15_F	0.37	0.54	0.56	0.61	0.51	0.60	0.69	0.76	0.86	0.96	1.04	1.14	ns
DIFF_SSTL15_S	0.37	0.54	0.56	0.61	0.57	0.67	0.77	0.84	0.86	0.96	1.04	1.15	ns
DIFF_SSTL15_R_F	0.37	0.54	0.56	0.61	0.58	0.68	0.77	0.85	0.83	0.90	0.99	1.09	ns
DIFF_SSTL15_R_S	0.37	0.54	0.56	0.61	0.67	0.78	0.89	0.97	0.83	0.90	0.99	1.09	ns
DIFF_SSTL18_I_F	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.85	0.76	0.84	0.90	0.99	ns
DIFF_SSTL18_I_S	0.37	0.54	0.56	0.61	0.95	1.12	1.26	1.38	0.76	0.83	0.94	1.03	ns
DIFF_SSTL18_II_F	0.37	0.54	0.56	0.61	0.50	0.59	0.68	0.74	0.86	0.93	1.02	1.12	ns
DIFF_SSTL18_II_S	0.37	0.54	0.56	0.61	0.50	0.59	0.68	0.74	0.86	0.93	1.02	1.12	ns
HSTL_I_18_F	0.37	0.54	0.56	0.61	0.65	0.77	0.86	0.95	0.77	0.89	0.99	1.09	ns
HSTL_I_18_S	0.37	0.54	0.56	0.61	0.65	0.77	0.86	0.95	0.77	0.89	0.99	1.09	ns
HSTL_I_F	0.37	0.54	0.56	0.61	0.65	0.77	0.86	0.95	0.77	0.89	0.99	1.09	ns
HSTL_I_S	0.37	0.54	0.56	0.61	0.65	0.77	0.86	0.95	0.77	0.89	0.99	1.09	ns
HSTL_II_18_F	0.37	0.54	0.56	0.61	0.50	0.59	0.67	0.74	0.87	0.95	1.05	1.15	ns
HSTL_II_18_S	0.37	0.54	0.56	0.61	0.56	0.66	0.75	0.82	0.88	0.95	1.05	1.15	ns
HSTL_II_F	0.37	0.54	0.56	0.61	0.51	0.60	0.69	0.76	0.85	0.95	1.03	1.13	ns
HSTL_II_S	0.37	0.54	0.56	0.61	0.51	0.60	0.69	0.76	0.85	0.95	1.03	1.13	ns
HSUL_12_F	0.37	0.54	0.56	0.61	0.93	1.12	1.29	1.42	0.77	0.84	0.93	1.02	ns
HSUL_12_S	0.37	0.54	0.56	0.61	0.93	1.12	1.29	1.42	0.77	0.84	0.93	1.02	ns
LVCMOS12_F_12	0.44	0.73	0.75	0.82	0.72	0.86	1.00	1.09	0.82	0.98	1.07	1.18	ns
LVCMOS12_F_4	0.44	0.73	0.75	0.82	1.01	1.21	1.40	1.54	0.72	0.80	0.88	0.97	ns
LVCMOS12_F_8	0.44	0.73	0.75	0.82	0.79	0.95	1.10	1.21	0.77	0.91	0.95	1.05	ns
LVCMOS12_S_12	0.44	0.73	0.75	0.82	0.86	1.03	1.17	1.29	0.82	0.98	1.07	1.18	ns
LVCMOS12_S_4	0.44	0.73	0.75	0.82	1.18	1.40	1.61	1.77	0.72	0.79	0.91	1.00	ns
LVCMOS12_S_8	0.44	0.73	0.75	0.82	0.94	1.11	1.28	1.40	0.77	0.88	0.99	1.09	ns
LVCMOS15_F_12	0.44	0.73	0.75	0.82	0.69	0.82	0.93	1.03	0.85	0.93	1.02	1.12	ns
LVCMOS15_F_16	0.44	0.73	0.75	0.82	0.65	0.78	0.89	0.98	0.87	0.97	1.05	1.15	ns
LVCMOS15_F_4	0.44	0.73	0.75	0.82	0.97	1.14	1.29	1.42	0.72	0.78	0.88	0.97	ns
LVCMOS15_F_8	0.44	0.73	0.75	0.82	0.75	0.89	1.01	1.12	0.84	0.91	1.03	1.13	ns

Table 21: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
LVCMOS15_S_12	0.44	0.73	0.75	0.82	0.81	0.96	1.09	1.20	0.86	0.94	1.02	1.12	ns
LVCMOS15_S_16	0.44	0.73	0.75	0.82	0.77	0.91	1.04	1.15	0.87	0.97	1.05	1.15	ns
LVCMOS15_S_4	0.44	0.73	0.75	0.82	1.09	1.29	1.46	1.60	0.72	0.78	0.89	0.97	ns
LVCMOS15_S_8	0.44	0.73	0.75	0.82	0.87	1.03	1.17	1.28	0.82	0.90	0.99	1.09	ns
LVCMOS18_F_12	0.44	0.73	0.75	0.82	0.71	0.85	0.96	1.06	0.81	0.88	1.00	1.10	ns
LVCMOS18_F_16	0.44	0.73	0.75	0.82	0.68	0.80	0.91	1.01	0.84	0.91	1.01	1.11	ns
LVCMOS18_F_4	0.44	0.73	0.75	0.82	0.96	1.13	1.27	1.40	0.71	0.77	0.84	0.92	ns
LVCMOS18_F_8	0.44	0.73	0.75	0.82	0.83	0.98	1.11	1.22	0.77	0.83	0.94	1.03	ns
LVCMOS18_S_12	0.44	0.73	0.75	0.82	0.81	0.96	1.08	1.19	0.81	0.88	0.97	1.07	ns
LVCMOS18_S_16	0.44	0.73	0.75	0.82	0.78	0.93	1.05	1.16	0.85	0.92	1.01	1.12	ns
LVCMOS18_S_4	0.44	0.73	0.75	0.82	1.05	1.23	1.38	1.52	0.70	0.77	0.84	0.93	ns
LVCMOS18_S_8	0.44	0.73	0.75	0.82	1.05	1.23	1.38	1.52	0.70	0.77	0.84	0.93	ns
LVCMOS25_F_12	0.58	0.80	0.82	0.91	1.24	1.50	1.80	1.98	1.05	1.35	1.55	1.71	ns
LVCMOS25_F_16	0.58	0.80	0.82	0.91	1.19	1.46	1.75	1.92	1.09	1.37	1.57	1.73	ns
LVCMOS25_F_4	0.58	0.80	0.82	0.91	1.88	2.24	2.64	2.91	0.86	1.17	1.38	1.51	ns
LVCMOS25_F_8	0.58	0.80	0.82	0.91	1.45	1.74	2.08	2.28	1.00	1.30	1.52	1.67	ns
LVCMOS25_S_12	0.58	0.80	0.82	0.91	2.01	2.46	2.92	3.21	1.06	1.35	1.55	1.71	ns
LVCMOS25_S_16	0.58	0.80	0.82	0.91	1.74	2.11	2.51	2.76	0.78	1.37	1.57	1.73	ns
LVCMOS25_S_4	0.58	0.80	0.82	0.91	3.07	3.65	4.31	4.74	0.87	1.19	1.38	1.51	ns
LVCMOS25_S_8	0.58	0.80	0.82	0.91	1.97	2.30	2.69	2.96	1.00	1.30	1.52	1.67	ns
LVCMOS33_F_12	0.58	0.80	0.82	0.91	1.31	1.42	1.69	1.86	0.95	1.16	1.35	1.49	ns
LVCMOS33_F_16	0.58	0.80	0.82	0.91	1.23	1.33	1.58	1.74	1.00	1.18	1.33	1.46	ns
LVCMOS33_F_4	0.58	0.80	0.82	0.91	2.01	2.19	2.50	2.75	0.58	0.58	0.58	0.64	ns
LVCMOS33_F_8	0.58	0.80	0.82	0.91	1.42	1.54	1.82	2.00	0.89	1.09	1.25	1.37	ns
LVCMOS33_S_12	0.58	0.80	0.82	0.91	1.68	1.93	2.15	2.37	0.96	1.16	1.32	1.45	ns
LVCMOS33_S_16	0.58	0.80	0.82	0.91	1.78	1.99	2.36	2.60	1.00	1.18	1.33	1.46	ns
LVCMOS33_S_4	0.58	0.80	0.82	0.91	3.24	3.66	4.30	4.73	0.61	0.95	1.07	1.18	ns
LVCMOS33_S_8	0.58	0.80	0.82	0.91	1.67	1.91	2.12	2.34	0.90	1.26	1.26	1.38	ns
LVDS_25					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
LVPECL					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
LVTTL_F_12	0.58	0.80	0.82	0.91	1.42	1.54	1.82	2.00	0.90	1.10	1.28	1.41	ns
LVTTL_F_16	0.58	0.80	0.82	0.91	1.30	1.42	1.67	1.84	0.97	1.13	1.28	1.41	ns
LVTTL_F_4	0.58	0.80	0.82	0.91	1.76	1.91	2.20	2.42	0.75	0.99	1.14	1.26	ns
LVTTL_F_8	0.58	0.80	0.82	0.91	1.76	1.91	2.20	2.42	0.75	0.99	1.14	1.26	ns
LVTTL_S_12	0.58	0.80	0.82	0.91	1.67	1.93	2.15	2.37	0.90	1.10	1.28	1.41	ns
LVTTL_S_16	0.58	0.80	0.82	0.91	2.08	2.37	2.80	3.09	0.97	1.16	1.31	1.44	ns
LVTTL_S_4	0.58	0.80	0.82	0.91	2.19	2.38	2.66	2.93	0.76	0.99	1.10	1.21	ns
LVTTL_S_8	0.58	0.80	0.82	0.91	2.19	2.38	2.66	2.93	0.76	0.99	1.10	1.21	ns

Table 21: **3.3V IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
MINI_LVDS_25					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
PPDS_25					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
RSDS_25					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
SLVS_400					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
SSTL12_F	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL12_S	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL135_F	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.86	0.84	0.98	1.07	1.18	ns
SSTL135_S	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.86	0.84	0.98	1.07	1.18	ns
SSTL135_R_F	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.86	0.84	0.98	1.07	1.18	ns
SSTL135_R_S	0.37	0.54	0.56	0.61	0.58	0.69	0.78	0.86	0.84	0.98	1.07	1.18	ns
SSTL15_F	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL15_S	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL15_R_F	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL15_R_S	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL18_I_F	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL18_I_S	0.37	0.54	0.56	0.61	0.63	0.75	0.85	0.94	0.82	0.98	1.07	1.18	ns
SSTL18_II_F	0.37	0.54	0.56	0.61	0.57	0.67	0.76	0.84	0.84	0.92	1.01	1.11	ns
SSTL18_II_S	0.37	0.54	0.56	0.61	0.57	0.67	0.76	0.84	0.84	0.92	1.01	1.11	ns
SUB_LVDS_25					0.71	0.86	0.89	0.98	110.80	110.80	110.80	121.88	ns
TMDS_33					0.70	0.86	0.89	0.97	110.80	110.80	110.80	121.88	ns

Table 22: **1.8V IOB High Performance (HP) Switching Characteristics**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
DIFF_HSTL_I_12_F	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
DIFF_HSTL_I_12_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
DIFF_HSTL_I_12_S	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
DIFF_HSTL_I_18_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.42	0.48	0.54	0.59	ns
DIFF_HSTL_I_18_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.50	0.46	0.54	0.60	0.66	ns
DIFF_HSTL_I_18_S	0.22	0.26	0.28	0.31	0.39	0.46	0.50	0.55	0.51	0.61	0.68	0.75	ns
DIFF_HSTL_I_DCI_12_F	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
DIFF_HSTL_I_DCI_12_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
DIFF_HSTL_I_DCI_12_S	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
DIFF_HSTL_I_DCI_18_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.42	0.48	0.54	0.59	ns
DIFF_HSTL_I_DCI_18_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.50	0.46	0.54	0.60	0.66	ns
DIFF_HSTL_I_DCI_18_S	0.22	0.26	0.28	0.31	0.39	0.46	0.50	0.55	0.51	0.61	0.68	0.75	ns

Table 22: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
DIFF_HSTL_I_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
DIFF_HSTL_I_DCI_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
DIFF_HSTL_I_DCI_S	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
DIFF_HSTL_I_F	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.41	0.48	0.53	0.58	ns
DIFF_HSTL_I_M	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.60	0.66	ns
DIFF_HSTL_I_S	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.60	0.66	ns
DIFF_HSUL_12_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.45	0.53	0.60	0.66	ns
DIFF_HSUL_12_DCI_M	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.45	0.53	0.60	0.66	ns
DIFF_HSUL_12_DCI_S	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_HSUL_12_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
DIFF_HSUL_12_M	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.51	0.60	0.67	0.74	ns
DIFF_HSUL_12_S	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.51	0.60	0.67	0.74	ns
DIFF_POD10_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.44	0.50	0.56	0.61	ns
DIFF_POD10_DCI_M	0.22	0.26	0.28	0.31	0.37	0.44	0.48	0.53	0.48	0.56	0.62	0.68	ns
DIFF_POD10_DCI_S	0.22	0.26	0.28	0.31	0.37	0.44	0.48	0.53	0.48	0.56	0.62	0.68	ns
DIFF_POD10_F	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.46	0.44	0.50	0.56	0.62	ns
DIFF_POD10_M	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.46	0.44	0.50	0.56	0.62	ns
DIFF_POD10_S	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.46	0.44	0.50	0.56	0.62	ns
DIFF_POD12_DCI_F	0.22	0.26	0.28	0.31	0.34	0.39	0.43	0.47	0.43	0.51	0.56	0.62	ns
DIFF_POD12_DCI_M	0.22	0.26	0.28	0.31	0.34	0.39	0.43	0.47	0.43	0.51	0.56	0.62	ns
DIFF_POD12_DCI_S	0.22	0.26	0.28	0.31	0.34	0.39	0.43	0.47	0.43	0.51	0.56	0.62	ns
DIFF_POD12_F	0.22	0.26	0.28	0.31	0.44	0.52	0.58	0.64	0.54	0.63	0.70	0.77	ns
DIFF_POD12_M	0.22	0.26	0.28	0.31	0.44	0.52	0.58	0.64	0.54	0.63	0.70	0.77	ns
DIFF_POD12_S	0.22	0.26	0.28	0.31	0.44	0.52	0.58	0.64	0.54	0.63	0.70	0.77	ns
DIFF_SSTL12_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL12_DCI_M	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL12_DCI_S	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL12_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL12_M	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL12_S	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL135_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
DIFF_SSTL135_DCI_M	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
DIFF_SSTL135_DCI_S	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
DIFF_SSTL135_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
DIFF_SSTL135_M	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.52	0.60	0.68	0.75	ns
DIFF_SSTL135_S	0.22	0.26	0.28	0.31	0.41	0.47	0.52	0.57	0.52	0.60	0.68	0.75	ns
DIFF_SSTL15_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
DIFF_SSTL15_DCI_M	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns

Table 22: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
DIFF_SSTL15_DCI_S	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
DIFF_SSTL15_F	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
DIFF_SSTL15_M	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
DIFF_SSTL15_S	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
DIFF_SSTL18_I_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
DIFF_SSTL18_I_DCI_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.51	0.46	0.53	0.60	0.67	ns
DIFF_SSTL18_I_DCI_S	0.22	0.26	0.28	0.31	0.40	0.46	0.51	0.56	0.52	0.61	0.69	0.76	ns
DIFF_SSTL18_I_F	0.22	0.26	0.28	0.31	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
DIFF_SSTL18_I_M	0.22	0.26	0.28	0.31	0.36	0.42	0.46	0.51	0.46	0.53	0.60	0.67	ns
DIFF_SSTL18_I_S	0.22	0.26	0.28	0.31	0.40	0.46	0.51	0.56	0.52	0.61	0.69	0.76	ns
HSLVDCI_15_F	0.35	0.44	0.59	0.65	0.34	0.39	0.43	0.47	0.42	0.48	0.53	0.59	ns
HSLVDCI_15_M	0.35	0.44	0.59	0.65	0.38	0.44	0.49	0.54	0.42	0.48	0.53	0.59	ns
HSLVDCI_15_S	0.35	0.44	0.59	0.65	0.43	0.50	0.56	0.61	0.50	0.59	0.66	0.73	ns
HSLVDCI_18_F	0.35	0.44	0.59	0.65	0.33	0.38	0.42	0.46	0.42	0.48	0.54	0.59	ns
HSLVDCI_18_M	0.35	0.44	0.59	0.65	0.37	0.43	0.48	0.53	0.44	0.52	0.58	0.64	ns
HSLVDCI_18_S	0.35	0.44	0.59	0.65	0.37	0.43	0.48	0.53	0.52	0.63	0.69	0.76	ns
HSTL_I_12_F	0.26	0.30	0.33	0.36	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
HSTL_I_12_M	0.26	0.30	0.33	0.36	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
HSTL_I_12_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
HSTL_I_18_F	0.26	0.30	0.33	0.36	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
HSTL_I_18_M	0.26	0.30	0.33	0.36	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
HSTL_I_18_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
HSTL_I_DCI_12_F	0.26	0.30	0.33	0.36	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
HSTL_I_DCI_12_M	0.26	0.30	0.33	0.36	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
HSTL_I_DCI_12_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
HSTL_I_DCI_18_F	0.26	0.30	0.33	0.36	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
HSTL_I_DCI_18_M	0.26	0.30	0.33	0.36	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
HSTL_I_DCI_18_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
HSTL_I_DCI_F	0.26	0.30	0.33	0.36	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
HSTL_I_DCI_M	0.26	0.30	0.33	0.36	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
HSTL_I_DCI_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
HSTL_I_F	0.26	0.30	0.33	0.36	0.33	0.38	0.41	0.45	0.41	0.48	0.53	0.58	ns
HSTL_I_M	0.26	0.30	0.33	0.36	0.36	0.42	0.46	0.50	0.45	0.53	0.60	0.66	ns
HSTL_I_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.52	0.61	0.69	0.76	ns
HSUL_12_DCI_F	0.26	0.30	0.33	0.36	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
HSUL_12_DCI_M	0.26	0.30	0.33	0.36	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
HSUL_12_DCI_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.51	0.60	0.67	0.74	ns
HSUL_12_F	0.26	0.30	0.33	0.36	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns

Table 22: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
HSUL_12_M	0.26	0.30	0.33	0.36	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.59	ns
HSUL_12_S	0.26	0.30	0.33	0.36	0.41	0.47	0.52	0.57	0.51	0.60	0.67	0.74	ns
LVCMOS12_F_2	0.35	0.44	0.59	0.65	0.40	0.46	0.50	0.55	0.42	0.49	0.54	0.59	ns
LVCMOS12_F_4	0.35	0.44	0.59	0.65	0.37	0.43	0.46	0.51	0.41	0.49	0.54	0.59	ns
LVCMOS12_F_6	0.35	0.44	0.59	0.65	0.35	0.40	0.45	0.49	0.42	0.48	0.54	0.59	ns
LVCMOS12_F_8	0.35	0.44	0.59	0.65	0.35	0.40	0.44	0.48	0.42	0.48	0.53	0.59	ns
LVCMOS12_M_2	0.35	0.44	0.59	0.65	0.44	0.52	0.56	0.62	0.45	0.54	0.60	0.66	ns
LVCMOS12_M_4	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.46	0.54	0.60	0.66	ns
LVCMOS12_M_6	0.35	0.44	0.59	0.65	0.40	0.46	0.51	0.56	0.45	0.53	0.59	0.65	ns
LVCMOS12_M_8	0.35	0.44	0.59	0.65	0.39	0.46	0.50	0.55	0.45	0.53	0.59	0.64	ns
LVCMOS12_S_2	0.35	0.44	0.59	0.65	0.52	0.60	0.66	0.72	0.52	0.62	0.67	0.74	ns
LVCMOS12_S_4	0.35	0.44	0.59	0.65	0.48	0.56	0.61	0.68	0.51	0.60	0.69	0.76	ns
LVCMOS12_S_6	0.35	0.44	0.59	0.65	0.46	0.53	0.59	0.65	0.52	0.60	0.67	0.73	ns
LVCMOS12_S_8	0.35	0.44	0.59	0.65	0.45	0.53	0.58	0.64	0.51	0.59	0.66	0.73	ns
LVCMOS15_F_12	0.35	0.44	0.59	0.65	0.34	0.39	0.43	0.47	0.42	0.48	0.53	0.59	ns
LVCMOS15_F_2	0.35	0.44	0.59	0.65	0.39	0.45	0.49	0.53	0.41	0.49	0.54	0.59	ns
LVCMOS15_F_4	0.35	0.44	0.59	0.65	0.36	0.42	0.46	0.50	0.41	0.49	0.54	0.59	ns
LVCMOS15_F_6	0.35	0.44	0.59	0.65	0.35	0.40	0.44	0.48	0.41	0.48	0.53	0.58	ns
LVCMOS15_F_8	0.35	0.44	0.59	0.65	0.34	0.40	0.43	0.48	0.41	0.48	0.53	0.58	ns
LVCMOS15_M_12	0.35	0.44	0.59	0.65	0.38	0.44	0.49	0.54	0.42	0.48	0.53	0.59	ns
LVCMOS15_M_2	0.35	0.44	0.59	0.65	0.45	0.52	0.57	0.62	0.46	0.55	0.60	0.66	ns
LVCMOS15_M_4	0.35	0.44	0.59	0.65	0.45	0.52	0.57	0.62	0.45	0.54	0.60	0.66	ns
LVCMOS15_M_6	0.35	0.44	0.59	0.65	0.39	0.45	0.50	0.55	0.45	0.54	0.60	0.66	ns
LVCMOS15_M_8	0.35	0.44	0.59	0.65	0.38	0.44	0.49	0.54	0.45	0.53	0.59	0.65	ns
LVCMOS15_S_12	0.35	0.44	0.59	0.65	0.43	0.50	0.56	0.61	0.50	0.59	0.66	0.73	ns
LVCMOS15_S_2	0.35	0.44	0.59	0.65	0.45	0.52	0.57	0.62	0.51	0.61	0.68	0.75	ns
LVCMOS15_S_4	0.35	0.44	0.59	0.65	0.48	0.56	0.62	0.68	0.51	0.61	0.68	0.75	ns
LVCMOS15_S_6	0.35	0.44	0.59	0.65	0.45	0.54	0.59	0.65	0.51	0.60	0.67	0.74	ns
LVCMOS15_S_8	0.35	0.44	0.59	0.65	0.44	0.52	0.57	0.63	0.50	0.60	0.67	0.74	ns
LVCMOS18_F_12	0.35	0.44	0.59	0.65	0.33	0.38	0.42	0.46	0.42	0.48	0.54	0.59	ns
LVCMOS18_F_2	0.35	0.44	0.59	0.65	0.39	0.45	0.49	0.53	0.42	0.49	0.54	0.59	ns
LVCMOS18_F_4	0.35	0.44	0.59	0.65	0.36	0.42	0.45	0.50	0.41	0.49	0.54	0.59	ns
LVCMOS18_F_6	0.35	0.44	0.59	0.65	0.35	0.40	0.43	0.48	0.42	0.48	0.53	0.59	ns
LVCMOS18_F_8	0.35	0.44	0.59	0.65	0.34	0.39	0.43	0.47	0.42	0.48	0.54	0.59	ns
LVCMOS18_M_12	0.35	0.44	0.59	0.65	0.37	0.43	0.48	0.53	0.44	0.52	0.58	0.64	ns
LVCMOS18_M_2	0.35	0.44	0.59	0.65	0.36	0.42	0.45	0.50	0.45	0.55	0.61	0.67	ns
LVCMOS18_M_4	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.45	0.55	0.61	0.67	ns
LVCMOS18_M_6	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.45	0.55	0.61	0.67	ns

Table 22: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
LVCMOS18_M_8	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.45	0.55	0.61	0.67	ns
LVCMOS18_S_12	0.35	0.44	0.59	0.65	0.37	0.43	0.48	0.53	0.52	0.63	0.69	0.76	ns
LVCMOS18_S_2	0.35	0.44	0.59	0.65	0.52	0.61	0.66	0.73	0.52	0.63	0.69	0.76	ns
LVCMOS18_S_4	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.52	0.63	0.69	0.76	ns
LVCMOS18_S_6	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.52	0.63	0.69	0.76	ns
LVCMOS18_S_8	0.35	0.44	0.59	0.65	0.41	0.48	0.53	0.58	0.52	0.63	0.69	0.76	ns
LVDCI_15_F	0.35	0.44	0.59	0.65	0.34	0.39	0.43	0.47	0.42	0.48	0.53	0.59	ns
LVDCI_15_M	0.35	0.44	0.59	0.65	0.38	0.44	0.49	0.54	0.42	0.48	0.53	0.59	ns
LVDCI_15_S	0.35	0.44	0.59	0.65	0.43	0.50	0.56	0.61	0.50	0.59	0.66	0.73	ns
LVDCI_18_F	0.35	0.44	0.59	0.65	0.33	0.38	0.42	0.46	0.42	0.48	0.54	0.59	ns
LVDCI_18_M	0.35	0.44	0.59	0.65	0.37	0.43	0.48	0.53	0.44	0.52	0.58	0.64	ns
LVDCI_18_S	0.35	0.44	0.59	0.65	0.37	0.43	0.48	0.53	0.52	0.63	0.69	0.76	ns
LVDS					0.39	0.48	0.50	0.55	933.04	933.04	933.04	1026.34	ns
POD10_DCI_F	0.22	0.26	0.28	0.31	0.47	0.55	0.62	0.68	0.53	0.62	0.71	0.78	ns
POD10_DCI_M	0.22	0.26	0.28	0.31	0.47	0.55	0.62	0.68	0.53	0.62	0.71	0.78	ns
POD10_DCI_S	0.22	0.26	0.28	0.31	0.47	0.55	0.62	0.68	0.53	0.62	0.71	0.78	ns
POD10_F	0.22	0.26	0.28	0.31	0.45	0.53	0.60	0.65	0.54	0.63	0.70	0.77	ns
POD10_M	0.22	0.26	0.28	0.31	0.45	0.53	0.60	0.65	0.54	0.63	0.70	0.77	ns
POD10_S	0.22	0.26	0.28	0.31	0.45	0.53	0.60	0.65	0.54	0.63	0.70	0.77	ns
POD12_DCI_F	0.22	0.26	0.28	0.31	0.45	0.53	0.60	0.65	0.54	0.63	0.70	0.77	ns
POD12_DCI_M	0.22	0.26	0.28	0.31	0.45	0.53	0.60	0.65	0.54	0.63	0.70	0.77	ns
POD12_DCI_S	0.22	0.26	0.28	0.31	0.45	0.53	0.60	0.65	0.54	0.63	0.70	0.77	ns
POD12_F	0.22	0.26	0.28	0.31	0.44	0.52	0.58	0.64	0.54	0.63	0.70	0.77	ns
POD12_M	0.22	0.26	0.28	0.31	0.44	0.52	0.58	0.64	0.54	0.63	0.70	0.77	ns
POD12_S	0.22	0.26	0.28	0.31	0.44	0.52	0.58	0.64	0.54	0.63	0.70	0.77	ns
SLVS_400_18													ns
SSTL12_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL12_DCI_M	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL12_DCI_S	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL12_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL12_M	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL12_S	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL135_DCI_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL135_DCI_M	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.46	0.54	0.60	0.66	ns
SSTL135_DCI_S	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.46	0.54	0.60	0.66	ns
SSTL135_F	0.22	0.26	0.28	0.31	0.33	0.38	0.42	0.46	0.41	0.48	0.53	0.58	ns
SSTL135_M	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.46	0.54	0.60	0.66	ns
SSTL135_S	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.46	0.54	0.60	0.66	ns

Table 22: **1.8V IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	1.0V	0.95V		0.9V	
	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	-3	-2	-1 / -1L	-1L	
SSTL15_DCI_F	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
SSTL15_DCI_M	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
SSTL15_DCI_S	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
SSTL15_F	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
SSTL15_M	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
SSTL15_S	0.22	0.26	0.28	0.31	0.37	0.42	0.46	0.51	0.45	0.53	0.59	0.65	ns
SSTL18_I_DCI_F	0.22	0.26	0.28	0.31	0.32	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
SSTL18_I_DCI_M	0.22	0.26	0.28	0.31	0.32	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
SSTL18_I_DCI_S	0.22	0.26	0.28	0.31	0.32	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
SSTL18_I_F	0.22	0.26	0.28	0.31	0.32	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
SSTL18_I_M	0.22	0.26	0.28	0.31	0.32	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
SSTL18_I_S	0.22	0.26	0.28	0.31	0.32	0.38	0.41	0.45	0.41	0.48	0.53	0.59	ns
SUB_LVDS					0.39	0.48	0.50	0.55	933.04	933.04	933.04	1026.34	ns

Table 23 specifies the values of $T_{OUTBUF\_DELAY\_TE\_PAD}$ and $T_{INBUF\_DELAY\_IBUFDIS\_O}$. $T_{OUTBUF\_DELAY\_TE\_PAD}$ is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{INBUF\_DELAY\_IBUFDIS\_O}$ is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{OUTBUF\_DELAY\_TE\_PAD}$ when the INTERMDISABLE pin is used.

Table 23: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1 / -1L	-1L	
$T_{OUTBUF\_DELAY\_TE\_PAD}$	T input to pad high-impedance	1.56	1.89	2.17	2.38	ns
$T_{INBUF\_DELAY\_IBUFDIS\_O}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	0.46	0.66	0.70	0.77	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.05	1.26	1.55	1.70	ns

CLB Switching Characteristics

Table 24: **CLB Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1 / -1L	-1L	
F_{TOG}	Toggle frequency (for export control)					MHz

Block RAM and FIFO Switching Characteristics

Table 25: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
Maximum Frequency						
$F_{MAX\_WF\_NC}$	Block RAM (Write First and No Change modes)	660	585	525	458	MHz
F_{MAX_RF}	Block RAM (Read First mode)	575	510	460	400	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	660	585	525	458	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration without PIPELINE	530	450	390	350	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in Write First or No Change mode.	660	585	525	458	MHz
	Block RAM in ECC configuration in Read First mode with PIPELINE	575	510	460	400	MHz
$F_{MAX\_ADDREN\_RDADDRCHANGE}$	Block RAM with address enable and read address change compare turned on.	575	510	460	400	MHz

Input/Output Delay Switching Characteristics

Table 26: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
F_{REFCLK}	REFCLK frequency	200.00	200.00	200.00	200.00	MHz
$T_{DELAY\_RST\_RDY}$	Reset to ready for IDELAYCTRL	0.50	0.61	0.70	0.77	ns
T_{MINPER_RST}	Minimum precision reset	52.00	52.00	52.00	52.00	ns
F_{MAX_IDELAY}	Maximum IDELAY frequency	364.96	364.96	316.46	316.46	MHz
F_{MAX_ODELAY}	Maximum ODELAY frequency	364.96	364.96	316.46	316.46	MHz
$T_{IDELAY\_RESOLUTION}$/ $T_{ODELAY\_RESOLUTION}$	IDELAY/ODELAY chain resolution	$1/(40 \times 8 \times F_{REF})$				

DSP48 Slice Switching Characteristics

Table 27: **DSP48 Slice Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
Maximum Frequency						
F_{MAX}	With all registers used	741	661	594	547	MHz
F_{MAX_PATDET}	With pattern detector	687	581	512	463	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	462	429	361	303	MHz

Table 27: **DSP48 Slice Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	428	387	326	276	MHz
$F_{MAX\_PREADD\_NOADREG}$	Without ADREG	468	429	358	342	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	335	312	260	255	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	316	286	238	209	MHz

Clock Buffers and Networks

Table 28: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
$T_{DELAY\_I\_O}$	BUFGCTRL delay from I0/I1 to O	0.12	0.15	0.17	0.19	ns
Maximum Frequency						
F_{MAX}	Global clock tree (BUFG)	850	725	630	630	MHz

Table 29: **Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
$T_{DELAY\_I\_O}$	Propagation delay from I to O	0.24	0.29	0.34	0.37	ns
$T_{DELAY\_CLR\_O}$	Propagation delay from CLR to O	0.22	0.27	0.31	0.34	ns
Maximum Frequency						
F_{MAX}	Global clock buffer with input divide capability (BUFGCE_DIV)	850	725	630	630	MHz

Table 30: **Global Clock Buffer with Clock Enable (BUFGCE)**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
$T_{DELAY\_I\_O}$	BUFGCE delay from I to O	0.06	0.07	0.08	0.09	ns
$T_{DELAY\_CE\_O}$	BUFGCE delay from CE to O	0.14	0.17	0.19	0.21	ns
Maximum Frequency						
F_{MAX}	Global clock buffer with clock enable (BUFGCE)	850	725	630	630	MHz

Table 31: **Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
$T_{DELAY\_I\_O}$	BUFCE_LEAF delay from I to O	0.043	0.054	0.062	0.068	ns
Maximum Frequency						
F_{MAX}	Leaf clock buffer with clock enable (BUFCE_LEAF)	850	725	630	630	MHz

Table 32: **GT Clock Buffer with Clock Enable and Clock Input Divide Capability**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
$T_{DELAY\_I\_O}$	BUFG_GT Delay from I to O	0.21	0.26	0.30	0.33	ns
Maximum Frequency						
F_{MAX}	GT clock buffer with clock enable and clock input divide capability	512	512	391	323	MHz

MMCM Switching Characteristics

Table 33: **MMCM Specification**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
MMCM_F_{INMAX}	Maximum input clock frequency	850	725	630	630	MHz
MMCM_F_{INMIN}	Minimum input clock frequency	10	10	10	10	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz	25	25	25	25	%
	Allowable input duty cycle: 50—199 MHz	30	30	30	30	%
	Allowable input duty cycle: 200—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase shift clock frequency	550	500	450	450	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency	600	600	600	600	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency	1600	1440	1200	1200	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical(1)	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical(1)	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs(2)	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter	Note 3				
MMCM_$T_{OUTDUTY}$	MMCM output clock duty cycle precision(4)	0.165	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time	100	100	100	100	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency	850	725	630	630	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency(4)(5)	4.69	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector with bandwidth set to High or optimized.	550	500	450	450	MHz
	Maximum frequency at the phase frequency detector with bandwidth set to Low.	550	500	450	450	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector	10	10	10	10	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path	3 ns Max or one CLKIN cycle				

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

PLL Switching Characteristics

Table 34: **PLL Specification(1)**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1/-1L	-1L	
PLL_F_{INMAX}	Maximum input clock frequency	850	725	630	630	MHz
PLL_F_{INMIN}	Minimum input clock frequency	70	70	70	70	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F_{INDUTY}	Allowable input duty cycle: 70—399 MHz	35	35	35	35	%
	Allowable input duty cycle: 400—499 MHz	40	40	40	40	%
	Allowable input duty cycle: >500 MHz	45	45	45	45	%
PLL_F_{VCOMIN}	Minimum TXPLL VCO frequency	600	600	600	600	MHz
PLL_F_{VCOMAX}	Maximum TXPLL VCO frequency	1335	1335	1200	1200	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the TXPLL outputs(2)	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	TXPLL output jitter	Note 3				
PLL_$T_{OUTDUTY}$	TXPLL CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B duty-cycle precision(4)	0.165	0.20	0.20	0.20	ns
	TXPLL CLKOUTPHY output clock duty-cycle precision at 2 x VCO	±5% of 2 x VCO period				
	TXPLL CLKOUTPHY output clock duty-cycle precision at 1 x VCO or 0.5 x VCO	0.060	0.060	0.060	0.060	ns
PLL_$T_{LOCKMAX}$	TXPLL maximum lock time	100				µs
PLL_F_{OUTMAX}	TXPLL maximum output frequency at CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B	850	725	630	630	MHz
	TXPLL maximum output frequency at CLKOUTPHY	2670	2670	2400	2400	MHz
PLL_F_{OUTMIN}	TXPLL minimum output frequency at CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B(5)	4.69	4.69	4.69	4.69	MHz
	TXPLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1200 1 x VCO mode: 600 0.5 x VCO mode: 300				MHz
PLL_$RST_{MINPULSE}$	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector with bandwidth set to High or optimized	667.5	667.5	600	600	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector	70	70	70	70	MHz

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 35: **Global Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.9V	
			-3	-2	-1/-1L	-1L	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF}	Global clock input and output flip-flop *without* MMCM/PLL (near clock region)	XCKU035					ns
		XCKU040	3.90	4.39	4.68	4.84	ns
		XCKU060	4.32	4.89	5.23	5.42	ns
		XCKU075	4.40	5.01	5.37	5.53	ns
		XCKU100					ns
		XCKU115					ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 36: **Global Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.9V	
			-3	-2	-1/-1L	-1L	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.							
T_{ICKOF_FAR}	Global clock input and output flip-flop *without* MMCM/PLL (far clock region)	XCKU035					ns
		XCKU040	4.30	4.89	5.23	5.40	ns
		XCKU060	4.73	5.41	5.80	6.01	ns
		XCKU075	4.84	5.55	5.96	6.16	ns
		XCKU100					ns
		XCKU115					ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.

Table 37: **Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.9V	
			-3	-2	-1/-1L	-1L	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.							
$T_{ICKOFMMCMCC}$	Global clock input and output flip-flop *with* MMCM	XCKU035					ns
		XCKU040	0.93	1.40	1.68	1.85	ns
		XCKU060	1.36	1.92	2.25	2.46	ns
		XCKU075	1.37	1.94	2.28	2.47	ns
		XCKU100					ns
		XCKU115					ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

Table 38: **Global Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.9V	
			-3	-2	-1/-1L	-1L	
SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with PLL.							
$T_{ICKOF\_PLL\_CC}$	Global clock input and output flip-flop *with* PLL	XCKU035					ns
		XCKU040	3.75	4.19	4.46	4.62	ns
		XCKU060	4.18	4.71	5.02	5.23	ns
		XCKU075	4.19	4.73	5.05	5.25	ns
		XCKU100					ns
		XCKU115					ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
2. PLL output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

Table 39: **Global Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.9V	
			-3	-2	-1/-1L	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)							
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	Global clock input and input flip-flop (or latch) with MMCM	XCKU035					ns
		XCKU040	2.37/–1.61	2.37/–1.40	2.37/–1.28	2.30/–1.25	ns
		XCKU060	2.36/–1.62	2.36/–1.44	2.36/–1.33	2.29/–1.26	ns
		XCKU075	2.17/–1.32	2.17/–1.04	2.17/–0.88	2.07/–0.84	ns
		XCKU100					ns
		XCKU115					ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 40: **Global Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade				Units
			1.0V	0.95V		0.9V	
			-3	-2	-1/-1L	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard.(1)(2)							
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	Global clock input and input flip-flop (or latch) with PLL	XCKU035					ns
		XCKU040	–0.37/1.21	–0.37/1.40	–0.37/1.49	–0.43/1.53	ns
		XCKU060	–0.38/1.20	–0.38/1.35	–0.38/1.44	–0.45/1.51	ns
		XCKU075	–0.57/1.50	–0.57/1.76	–0.57/1.90	–0.67/1.94	ns
		XCKU100					ns
		XCKU115					ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 41: **Sample Window**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.9V	
		-3	-2	-1 / -1L	-1L	
	Sampling error at receiver pins(1)					ns

Notes:

1. This parameter indicates the total sampling error of the DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.

Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

Table 42: **Package Skew**

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package Skew	XCKU035	FBVA676		ps
			FBVA900		ps
			FFVA1156		ps
		XCKU040	FBVA676	173	ps
			FBVA900	162	ps
			FFVA1156	168	ps
		XCKU060	FFVA1156		ps
			FFVA1517		ps
		XCKU075	FFVA1156		ps
			FFVA1517		ps
			FFVA1760		ps
		XCKU100	FLVA1517		ps
			FLVB1517		ps
			FLVA1760		ps
			FLVD1924		ps
			FLVF1924		ps
		XCKU115	FLVA1517		ps
			FLVB1517		ps
			FLVA1760		ps
			FLVD1924		ps
			FLVF1924		ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTH Transceiver Specifications

GTH Transceiver DC Input and Output Levels

Table 43 summarizes the DC specifications of the GTH transceivers in Kintex UltraScale FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 43: **GTH Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Absolute input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–400	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
D_{VPPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to 1010	–	–	800	mV
$V_{CMOUTDC}$	Common mode output voltage: DC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/4$			mV
$V_{CMOUTAC}$	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R_{IN}	Differential input resistance		–	100	–	W
R_{OUT}	Differential output resistance		–	100	–	W
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	10	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		–	100	–	nF

Notes:

1. The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide* (UG576), and can result in values lower than reported in this table.
2. Other values can be used as appropriate to conform to specific protocols and standards.

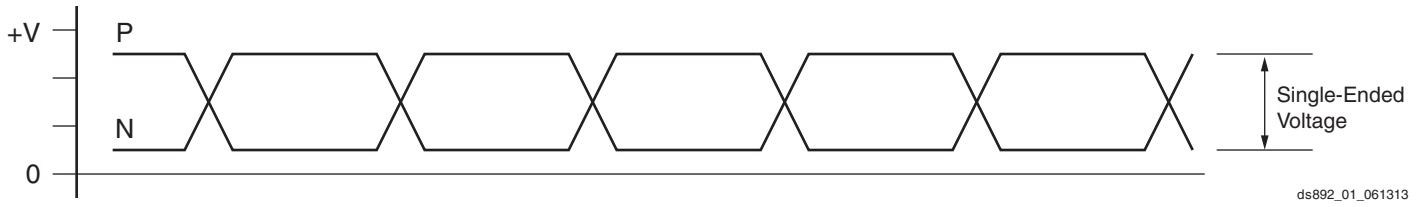

Figure 1: **Single-Ended Peak-to-Peak Voltage**

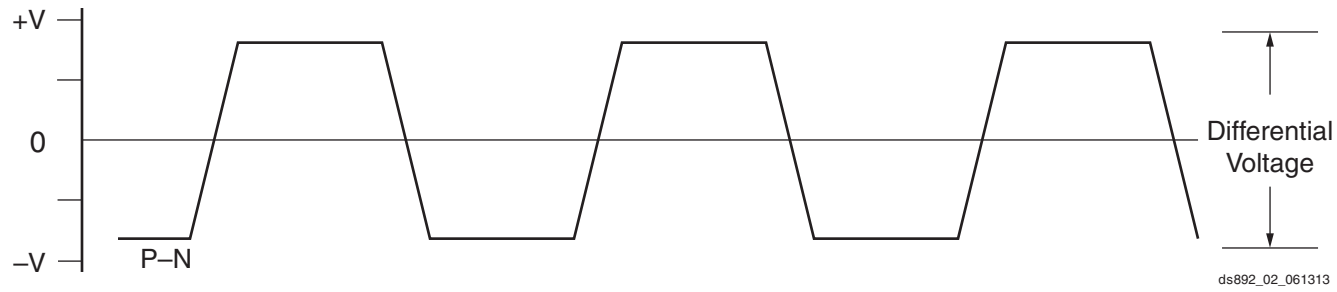

Figure 2: **Differential Peak-to-Peak Voltage**

Table 44 summarizes the DC specifications of the clock input of the GTH transceivers in Kintex UltraScale FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 44: **GTH Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further information.

Table 45: **GTH Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V		0.95V				0.90V		
			-3E		-2E, -2I		-1C,-1I,-1LI		-1LI		
F_{GTHMAX}	GTH maximum line rate		16.375		16.375		12.5		10.3125		Gb/s
F_{GTHMIN}	GTH minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHCRANGE}$	CPLL line rate range	1	4.0	12.5	4.0	12.5	4.0	8.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	4.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	2.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.0625	0.5	1.0625	Gb/s
		16	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE1}$	QPLL0 line rate range	1	9.8	16.375	9.8	16.375	9.8	12.5	9.8	10.3125	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.15	4.9	8.15	Gb/s
		4	2.45	4.09375	2.45	4.09375	2.45	4.075	2.45	4.075	Gb/s
		8	1.225	2.046875	1.225	2.046875	1.225	2.0375	1.225	2.0375	Gb/s
		16	0.6125	1.0234375	0.6125	1.0234375	0.6125	1.01875	0.6125	1.01875	Gb/s

Table 45: **GTH Transceiver Performance *(Cont'd)***

Symbol	Description	Output Divider	Speed Grade								Units
			1.0V		0.95V				0.90V		
			-3E		-2E, -2I		-1C,-1I,-1LI		-1LI		
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{GTHQRANGE2}$	QPLL1 line rate range	1	8.0	13.0	8.0	13.0	8.0	12.5	8.0	10.3125	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.6250	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
$F_{CPLLRANGE}$	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	4.25	2.0	4.25	GHz
$F_{QPLL0RANGE}$	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
$F_{QPLL1RANGE}$	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

Table 46: **GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	All Speed Grades	Units
$F_{GTHDRPCLK}$	GTHDRPCLK maximum frequency	200	MHz

Table 47: **GTH Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range		60	–	820	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

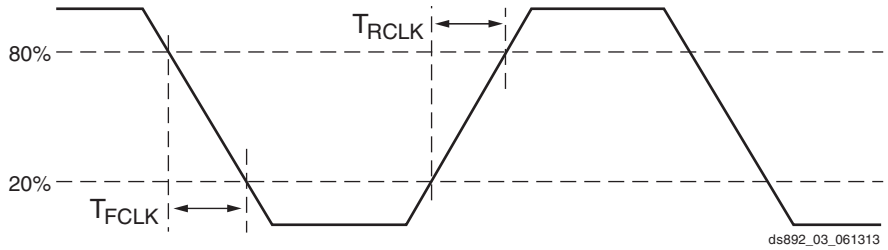

Figure 3: **Reference Clock Timing Parameters**

Table 48: **GTH Transceiver PLL/Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms

Table 48: **GTH Transceiver PLL/Lock Time Adaptation *(Cont'd)***

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10^6	UI

Table 49: **GTH Transceiver User Clock Switching Characteristics(1)**

Symbol	Description	Data Width Conditions (Bit)		Speed Grade				Units
				1.0V	0.95V		0.90V	
		Internal Logic	Interconnect Logic	-3E(2)	-2E, -2I(2)	-1C, -1I(3), -1LI(4)	-1LI(4)	
F_{TXOUT}	TXOUTCLK maximum frequency			511.719	511.719	390.625	322.266	MHz
F_{RXOUT}	RXOUTCLK maximum frequency			511.719	511.719	390.625	322.266	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	257.813	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16	16, 32	511.719	511.719	390.625	322.266	MHz
		32	32, 64	511.719	511.719	390.625	322.266	MHz
		20	20, 40	409.375	409.375	312.500	257.813	MHz
		40	40, 80	409.375	409.375	312.500	257.813	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16	16	511.719	511.719	390.625	322.266	MHz
		16, 32	32	511.719	511.719	390.625	322.266	MHz
		32	64	255.860	255.860	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	257.813	MHz
		20, 40	40	409.375	409.375	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	128.907	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16	16	511.719	511.719	390.625	322.266	MHz
		16, 32	32	511.719	511.719	390.625	322.266	MHz
		32	64	255.860	255.860	195.313	161.133	MHz
		20	20	409.375	409.375	312.500	257.813	MHz
		20, 40	40	409.375	409.375	312.500	257.813	MHz
		40	80	204.688	204.688	156.250	128.907	MHz

Notes:

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide* (UG576).
2. For speed grades -3 and -2, a 16-bit and 20-bit internal data path can only be used for line rates less than 8.1875 Gb/s.
3. For speed grade -1, a 16-bit and 20-bit internal path can only be used for line rates less than 6.25 Gb/s.
4. For speed grade -1L, a 16-bit and 20-bit data path can only be used for speeds less than 5.15625 Gb/s.

Table 50: **GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHTX}	Serial data rate range		0.500	–	F_{GTHMAX}	Gb/s
T_{RTX}	TX rise time	20%–80%	–	40	–	ps
T_{FTX}	TX fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	17	UI
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$T_{J16.375}$	Total jitter(2)(4)	16.375 Gb/s	–	–		UI
$D_{J16.375}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J12.5}$	Total jitter(2)(4)	12.5 Gb/s	–	–		UI
$D_{J12.5}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J11.3}$	Total jitter(2)(4)	11.3 Gb/s	–	–		UI
$D_{J11.3}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J10.3125\_QPLL}$	Total jitter(2)(4)	10.3125 Gb/s	–	–		UI
$D_{J10.3125\_QPLL}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J10.3125\_CPLL}$	Total jitter(3)(4)	10.3125 Gb/s	–	–		UI
$D_{J10.3125\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J9.953}$	Total jitter(2)(4)	9.953 Gb/s	–	–		UI
$D_{J9.953}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J9.8}$	Total jitter(2)(4)	9.8 Gb/s	–	–		UI
$D_{J9.8}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J8.0\_QPLL}$	Total jitter(2)(4)	8.0 Gb/s	–	–		UI
$D_{J8.0\_QPLL}$	Deterministic jitter(2)(4)		–	–		UI
$T_{J8.0\_CPLL}$	Total jitter(3)(4)	8.0 Gb/s	–	–		UI
$D_{J8.0\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J6.6\_CPLL}$	Total jitter(3)(4)	6.6 Gb/s	–	–		UI
$D_{J6.6\_CPLL}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J5.0}$	Total jitter(3)(4)	5.0 Gb/s	–	–		UI
$D_{J5.0}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J4.25}$	Total jitter(3)(4)	4.25 Gb/s	–	–		UI
$D_{J4.25}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.75}$	Total jitter(3)(4)	3.75 Gb/s	–	–		UI
$D_{J3.75}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.20}$	Total jitter(3)(4)	3.20 Gb/s(5)	–	–		UI
$D_{J3.20}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J3.20L}$	Total jitter(3)(4)	3.20 Gb/s(6)	–	–		UI
$D_{J3.20L}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J2.5}$	Total jitter(3)(4)	2.5 Gb/s(7)	–	–		UI
$D_{J2.5}$	Deterministic jitter(3)(4)		–	–		UI
$T_{J1.25}$	Total jitter(3)(4)	1.25 Gb/s(8)	–	–		UI
$D_{J1.25}$	Deterministic jitter(3)(4)		–	–		UI

Table 50: **GTH Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
T_{J500}	Total jitter(3)(4)	500 Mb/s	–	–		UI
D_{J500}	Deterministic jitter(3)(4)		–	–		UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTH Quad) at maximum line rate.
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of 10^{-12}.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 51: **GTH Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTHRX}	Serial data rate		0.500	–	F_{GTHMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated at 33 KHz	–5000	–	0	ppm
R_{XRL}	Run length (CID)		–	–	256	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$J_{T\_SJ16.375}$	Sinusoidal jitter (QPLL)(3)	16.375 Gb/s		–	–	UI
$J_{T\_SJ12.5}$	Sinusoidal jitter (QPLL)(3)	12.5 Gb/s		–	–	UI
$J_{T\_SJ11.3}$	Sinusoidal jitter (QPLL)(3)	11.3 Gb/s		–	–	UI
$J_{T\_SJ10.32\_QPLL}$	Sinusoidal jitter (QPLL)(3)	10.32 Gb/s		–	–	UI
$J_{T\_SJ10.32\_CPLL}$	Sinusoidal jitter (CPLL)(3)	10.32 Gb/s		–	–	UI
$J_{T\_SJ9.8}$	Sinusoidal jitter (QPLL)(3)	9.8 Gb/s		–	–	UI
$J_{T\_SJ8.0\_QPLL}$	Sinusoidal jitter (QPLL)(3)	8.0 Gb/s		–	–	UI
$J_{T\_SJ8.0\_CPLL}$	Sinusoidal jitter (CPLL)(3)	8.0 Gb/s		–	–	UI
$J_{T\_SJ6.6\_CPLL}$	Sinusoidal jitter (CPLL)(3)	6.6 Gb/s		–	–	UI
$J_{T\_SJ5.0}$	Sinusoidal jitter (CPLL)(3)	5.0 Gb/s		–	–	UI
$J_{T\_SJ4.25}$	Sinusoidal jitter (CPLL)(3)	4.25 Gb/s		–	–	UI
$J_{T\_SJ3.75}$	Sinusoidal jitter (CPLL)(3)	3.75 Gb/s		–	–	UI
$J_{T\_SJ3.2}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(4)		–	–	UI
$J_{T\_SJ3.2L}$	Sinusoidal jitter (CPLL)(3)	3.2 Gb/s(5)		–	–	UI
$J_{T\_SJ2.5}$	Sinusoidal jitter (CPLL)(3)	2.5 Gb/s(6)		–	–	UI
$J_{T\_SJ1.25}$	Sinusoidal jitter (CPLL)(3)	1.25 Gb/s(7)		–	–	UI

Table 51: **GTH Transceiver Receiver Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
J_{T_SJ500}	Sinusoidal jitter (CPLL)(3)	500 Mb/s		–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$J_{T\_TJSE3.2}$	Total jitter with stressed eye(8)	3.2 Gb/s		–	–	UI
$J_{T\_TJSE6.6}$		6.6 Gb/s		–	–	UI
$J_{T\_SJSE3.2}$	Sinusoidal jitter with stressed eye(8)	3.2 Gb/s		–	–	UI
$J_{T\_SJSE6.6}$		6.6 Gb/s		–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of 10^{-12}.
3. The frequency of the injected sinusoidal jitter is 80 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX equalizer enabled. DFE disabled.

GTH Transceiver Protocol Jitter Characteristics

For Table 52 through Table 57, the *UltraScale Architecture GTH Transceiver User Guide* (UG576) contains recommended settings for optimal usage of protocol specific characteristics.

Table 52: **Gigabit Ethernet Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 53: **XAUI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 54: **PCI Express Protocol Characteristics (GTH Transceivers)(1)**

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

Table 55: **CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 56: **SFP+ Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:
1. Line rated used for CPRI over SFP+ applications.

Table 57: **CPRI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:
1. Tested per SFP+ specification, see Table 56.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at: www.xilinx.com/technology/protocols/pciexpress.htm.

Table 58: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1/-1L	-1L	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
$F_{CORECLK}$	Core clock maximum frequency	500.00(1)	500.00(1)	250.00	250.00	MHz
$F_{USERCLK}$	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

Notes:
1. PCI Express x8 Gen 3 operation is only supported in -2 and -3 speed grades.

System Monitor Specifications

Table 59: **SYSMON Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ±3%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_j = –40°C to 100°C, typical values at T_j = 40°C						
System Monitor Accuracy(1)						
Resolution			10	–	–	Bits
Integral nonlinearity(2)	INL		–	–	±1	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	2	LSBs
Gain error		Gain calibration enabled	–	–	±0.4	%
Sample rate			0.1	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
Accuracy Across (–55°C to 125°C) Temperature Range						
Resolution			10	–	–	Bits
Integral nonlinearity	INL		–	–	±1	LSB
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	

Table 59: **SYSMON Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog Inputs[2]						
SYSMON input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
On-Chip Sensors						
Temperature sensor error		T_j = –40°C to 100°C (with external REF)	–	–	±4	°C
		T_j = –55°C to 125°C (with external REF)	–	–	±6	°C
		T_j = –40°C to 100°C (with internal REF)	–	–	±4	°C
		T_j = –55°C to 125°C (with internal REF)	–	–	±6	°C
Supply sensor error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to 100°C (with external REF)	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to 125°C (with external REF)	–	–	±2	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to 100°C (with internal REF)	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to 125°C (with internal REF)	–	–	±2	%
Conversion Rate[3]						
Conversion time—continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t_{CONV}	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
SYSMON Reference[4]						
External reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V_{REFP} pin to AGND, T_j = –55°C to 125°C	1.225	1.25	1.275	V

Notes:

1. Offset and gain errors are removed by enabling the SYSMON automatic gain calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide* (UG580)
3. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide* (UG580)
4. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

I2C Interfaces

Table 60: **I2C Fast Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
T_{DCFCLK}	SCL duty cycle	–	50	–	%
T_{FCKO}	SDAO clock-to-out delay	–	–	900	ns
T_{FDCK}	SDAI setup time	100	–	–	ns
F_{FCLK}	SCL clock frequency	–	–	400	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

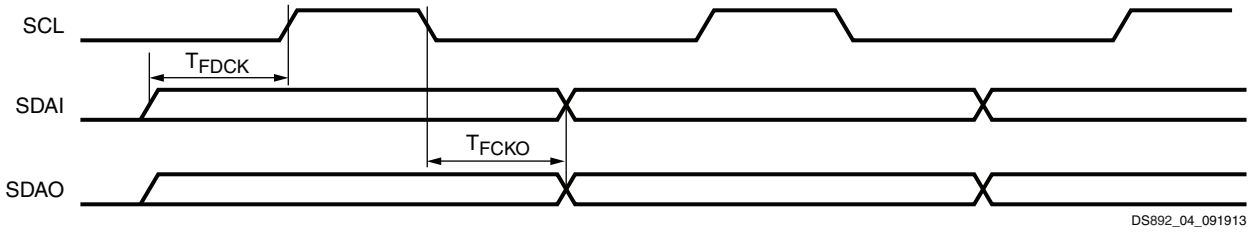

Figure 4: **I2C Fast Mode Interface Timing Diagram**

Table 61: **I2C Standard Mode Interface Switching Characteristics(1)**

Symbol	Description	Min	Typ	Max	Units
T_{DCSCLK}	SCL duty cycle	–	50	–	%
T_{SCKO}	SDAO clock-to-out delay	–	–	3450	ns
T_{SDCK}	SDAI setup time	250	–	–	ns
F_{SCLK}	SCL clock frequency	–	–	100	KHz

Notes:

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.

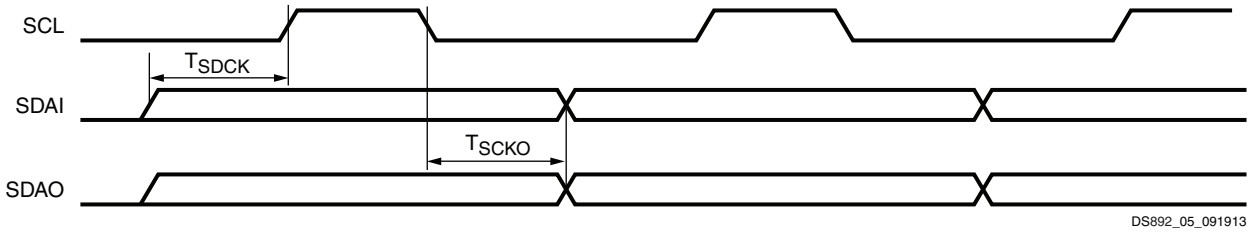

Figure 5: **I2C Standard Mode Interface Timing Diagram**

Configuration Switching Characteristics

Table 62: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1/-1L	-1L	
Power-up Timing Characteristics						
T_{PL}	Program latency	5	5	5	5	ms, Max
T_{POR}	Power-on reset (50 ms ramp rate time)	50	50	50	50	ms, Min/Max
	Power-on reset with POR override	29	29	29	29	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	ns, Min
CCLK Output (Master Mode)						
T_{ICCK}	Master CCLK output delay					ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle					%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle					%, Min/Max
F_{MCCK}	Master CCLK frequency	150.00	150.00	150.00	150.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±15	±15	±15	±15	%, Max
CCLK Input (Slave Modes)						
T_{SCCKL}	Slave CCLK clock minimum Low time					ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time					ns, Min
F_{SCCK}	Slave CCLK frequency	150.00	150.00	150.00	150.00	MHz, Max
EMCCLK Input (Master Mode)						
T_{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency	150.00	150.00	150.00	150.00	MHz, Max
Internal Configuration Access Port						
F_{ICAPCK}	Internal configuration access port (ICAPE2)	200.00	200.00	200.00	175.00	MHz, Max
Master/Slave Serial Mode Programming Switching						
T_{DCCK}/T_{CCKD}	D_{IN} Setup/Hold					ns, Min
T_{CCO}	D_{OUT} clock to out					ns, Max
SelectMAP Mode Programming Switching						
T_{SMDCCK}/T_{SMCCKD}	D[31:00] Setup/Hold					ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CSI_B Setup/Hold					ns, Min
T_{SMWCCK}/T_{SMCCKW}	RDWR_B Setup/Hold					ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)					ns, Max

Table 62: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade				Units
		1.0V	0.95V		0.90V	
		-3	-2	-1/-1L	-1L	
T_{SMCO}	D[31:00] clock to out in readback					ns, Max
F_{RBCCK}	Readback frequency	125.00	125.00	125.00	125.00	MHz, Max
Boundary-Scan Port Timing Specifications						
T_{TAPTCK}/T_{TCKTAP}	TMS and TDI Setup/Hold					ns, Min
T_{TCKTDO}	TCK falling edge to TDO output					ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	66.00	MHz, Max
BPI Master Flash Mode Programming Switching						
T_{BPICCO}	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out					ns, Max
T_{BPIDCC}/T_{BPICCD}	D[15:00] Setup/Hold					ns, Min
SPI Master Flash Mode Programming Switching						
T_{SPIDCC}/T_{SPICCD}	D[03:00] Setup/Hold					ns, Min
T_{SPIDCC}/T_{SPICCD}	D[07:04] Setup/Hold					ns, Min
T_{SPICCM}	MOSI clock to out					ns, Max
$T_{SPICCFC}$	FCS_B clock to out					ns, Max
DNA Port Switching						
F_{DNACK}	DNA port frequency	200.00	200.00	200.00	175.00	MHz, Max
USRCCLK Output						
$T_{USRCCLKO}$	STARTUPE2 USRCCLKO input to CCLK output					ns, Min/Max

eFUSE Programming Conditions

Table 63: **eFUSE Programming Conditions**(1)

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	–40	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
12/10/2013	1.0	Initial Xilinx release.

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