TAIWAN SEMICONDUCTOR

TESDB5V0A
5V, 2-Channels ESD Protection Array

Small Signal Diode

Features

✧Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
✧Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
✧Protects two directional I/O lines
✧Working Voltage : 5V
✧Pb free version, RoHS compliant, and Halogen free

Mechanical Data

✧Case :SOT-143 package, molded plastic
✧Terminal: Matte tin plated, lead free.
✧High temperature soldering guaranteed: 260°C/10s
✧Molding Compound Flammability Rating : UL 94V-0
✧Weight : 10mg (approximately)
✧Marking Code : SL3

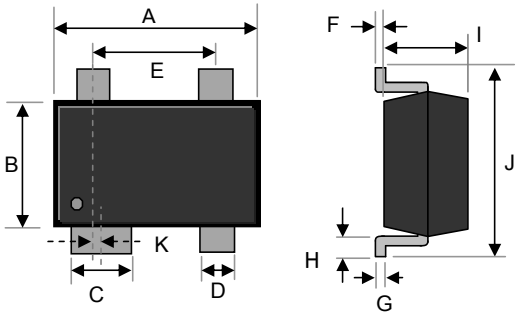
Applications

✧USB Power & Data Line Protection
✧I^2C Bus Protection
✧Video Line Protection
✧Microcontroller Input Protectionrs
✧T1/E1 secondary IC side Protection
✧ISDN S/T Interface
✧WAN/LAN Equipment
✧Ethernet 10BaseT

Ordering Information

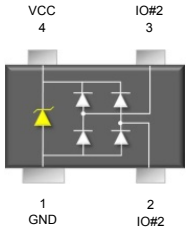
Part No.	Package	Packing	Packing Code	Marking
TESDB5V0A	SOT-143	3K / 7" Reel	RBG	SL3

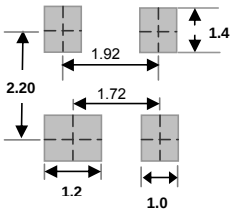
SOT-143



Dimensions	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.800	3.040	0.110	0.120
B	1.200	1.400	0.047	0.055
C	0.760	0.940	0.030	0.037
D	0.300	0.510	0.012	0.020
E	2.100	2.640	0.083	0.104
F	0.013	0.015	0.001	0.001
G	0.080	0.200	0.003	0.008
H	0.400	0.600	0.016	0.024
I	0.750	1.070	0.030	0.042
J	2.100	2.640	0.083	0.104
K	0.2 (BSC)		0.008(BSC)	

Pin Configutation & PAD Layout





Unit : mm

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.

Maximum Ratings

Type Number	Symbol	Value	Units
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	200	W
Peak Pulse Current (tp = 8/20μs)	I_{PP}	10	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ± 8	KV
Junction Temperature Range	T_J	-55 to + 150	°C
Storage Temperature Range	T_{STG}	-55 to + 150	°C

Electrical Characteristics

Type Number		Symbol	Min	Max	Units
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Voltage	I_R= 1mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R= 5V	I_R	-	5	uA
Clamping Voltage	I_{PP}= 1A	Vc	-	9.8	V
	I_{PP}= 3A		-	17	
Junction Capacitance	V_R=0V, f=1.0MHz	C_J	3 (Typ.)		pF

Notes: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary despending on application.

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Rating and Characteristic Curves

FIG 1. Admissible Power Dissipation Curve

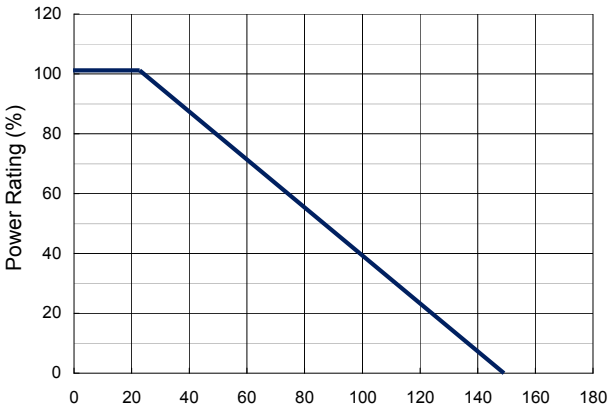


FIG 2. Pulse Waveform

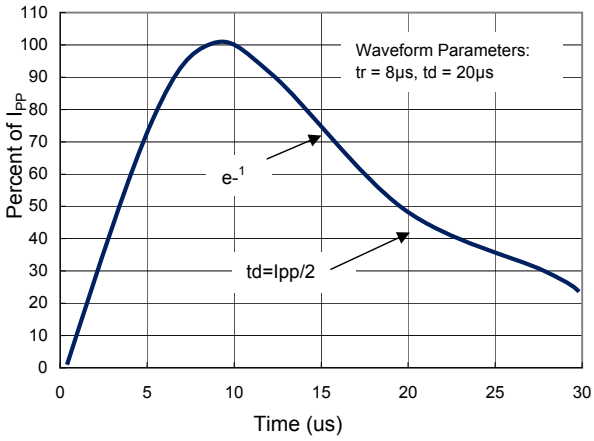


FIG 3. Clamping Voltage vs. Peak Pulse Current

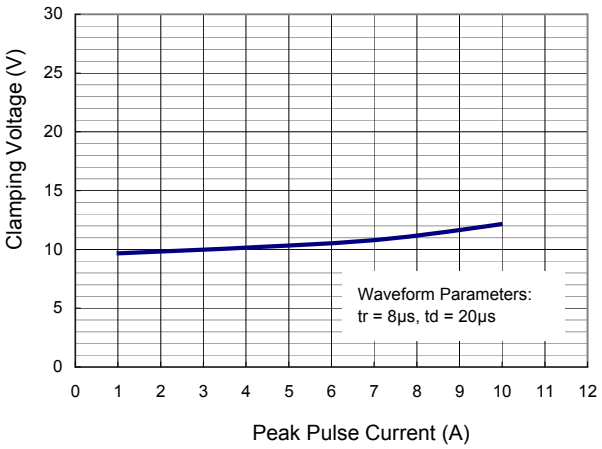
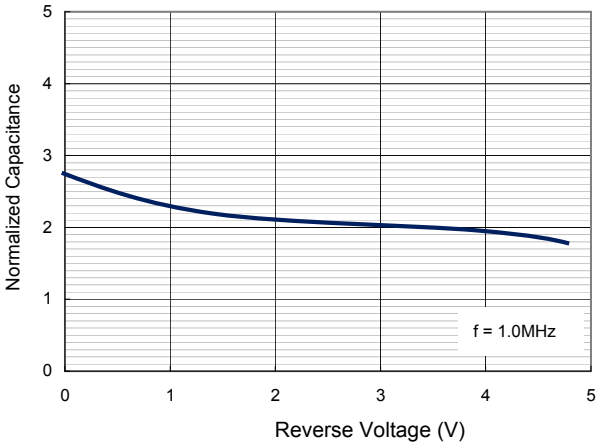


FIG 4. Typical Junction Capacitance



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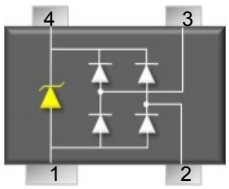
Applications Information

✧Designed for the protect two data lines from transient over-voltages by clamping them to afixed reference.

✧Data lines are connected at pins 2 and 3.

✧The negative reference (REF1) is connected at pin1 and which should be connected directly to a ground plane on the board for best results.

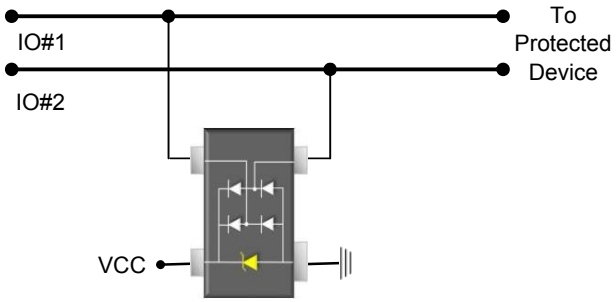
✧The positive reference (REF2) is connected at pin 4.



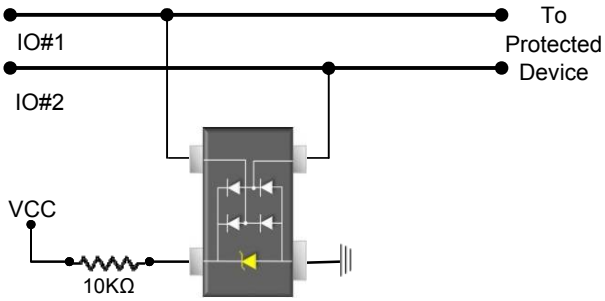
Pin	Definition
2, 3	I/O Lines
1	Ground
4	VCC

Typical Application

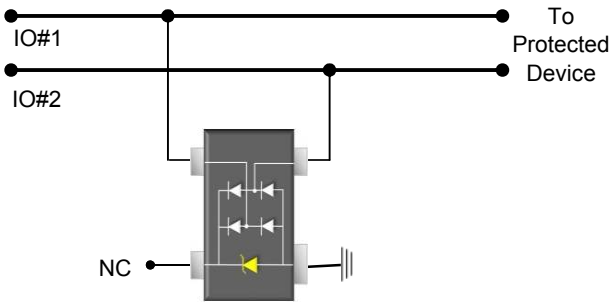
Schematic Diagram for Gigabit Ethernet ESD Protection



✧Data Line and Power Supply Protection Using VCC



✧Data Line Protection with Bias and Power Supply Isolation Resistor



✧Data Line Protection Using Internal ESD Diode

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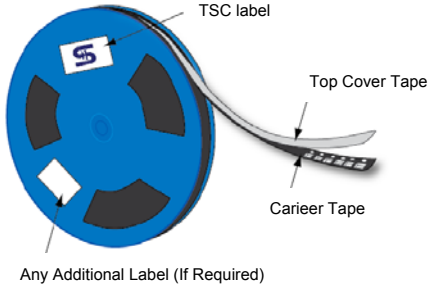
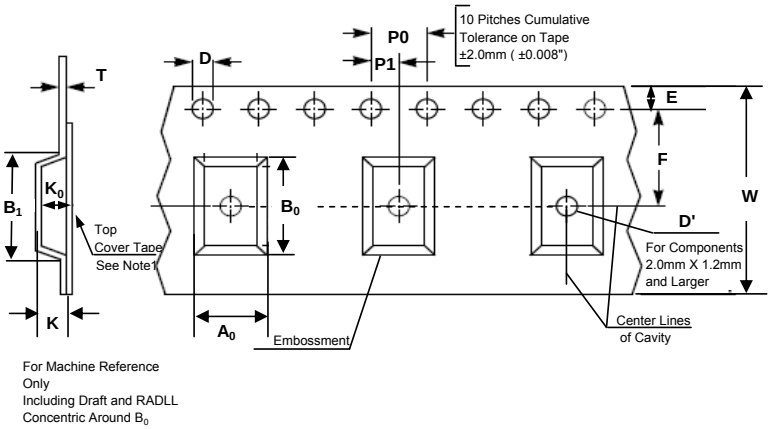
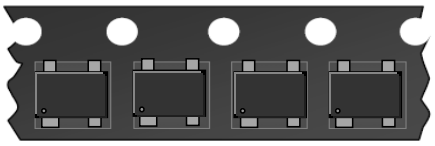
Carrier & Reel specification

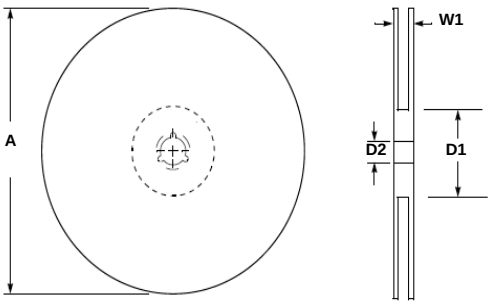


Item	Symbol	Dimension(mm)
Carrier depth	K	1.22 Max.
Sprocket hole	D	1.50 +0.10
Reel outside diameter	A	180 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocke hole position	E	1.75 ±0.10
Sprocke hole pitch	P0	4.00 ±0.10
Embossment center	P1	2.00 ±0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.





Direction of Feed



Note 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max. The component cannot rote more than 10 ^{o} within the determined cavity.

Note 2: If B1 exceeds 4.2 mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape feeders.