TPL5100 Nano Power Programmable Timer with MOS driver

Check for Samples: TPL5100

FEATURES

- **Supply Voltage from 1.8V to 5.0V**
- **Selectable Timer Intervals, 16s to 1024s**
- **Current Consumption 30nA (typ, at 2.5V)**

APPLICATIONS

- **Battery-Powered Systems**
- **Energy Harvesting Systems**
- **Remote Data-Logger**
- **Sensor Node**
- **Power-gating applications**
- **Building automation**
- **Low power wireless**
- **Consumer electronics**

DESCRIPTION

The TPL5100 is a long-term timer IC optimized for low power applications. The TPL5100 can replace a micro controller's (µC) internal timer, allowing the µC to stay completely off instead of running a timer, providing a total power consumption reduction of 60 to 80%.The TPL5100 is designed for use in power cycled applications and provides selectable timing from 16 seconds to 1024 seconds. The TPL5100 can also monitor a battery management IC via a power-good digital input and power on the µC only when a good supply voltage is present. The device is packaged in a 10-pin VSSOP package.

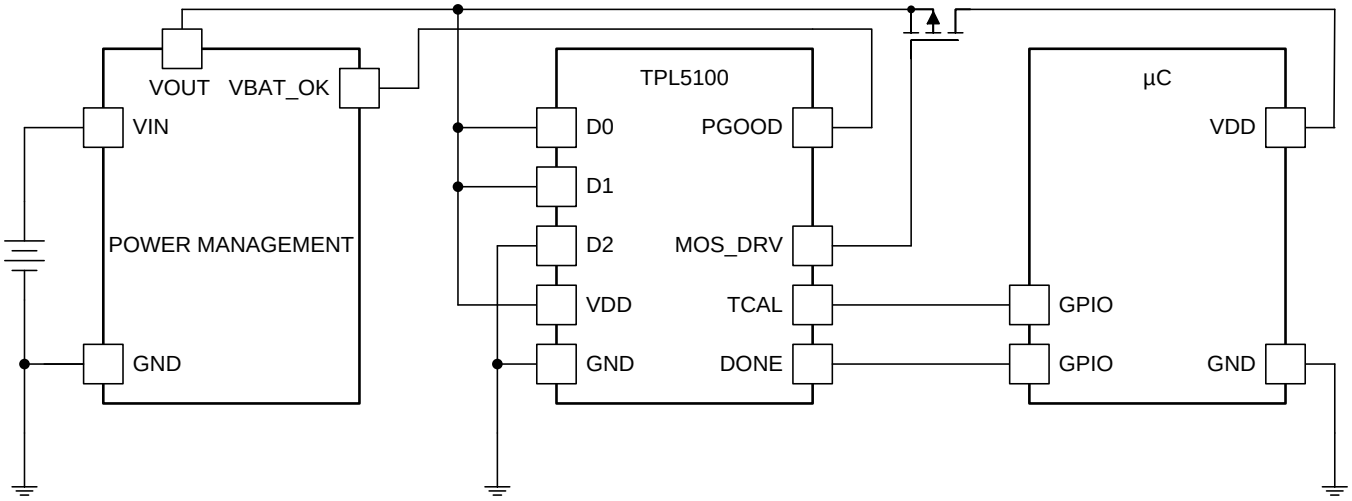


Figure 1. Simplified Application Schematic

Block Diagram

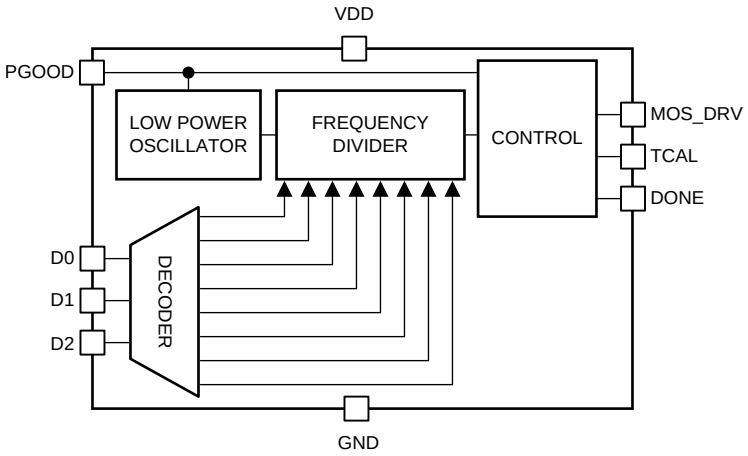


Figure 2. Block Diagram

Connection Diagram

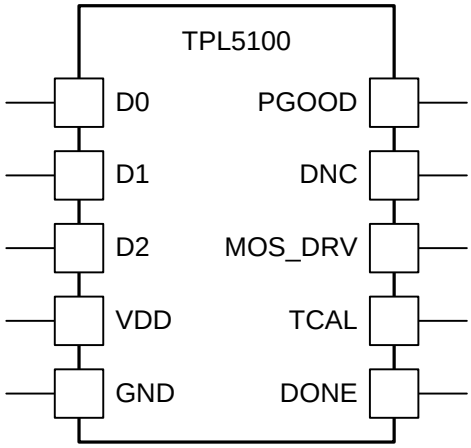


Figure 3. Top View
10-Lead VSSOP

Pin Descriptions

Pin(s)	Name	Description	Application Information
1	D0	Logic Input to set period delay (t_{DP})	Connect to GND (low logic value) or to VDD (high logic value)
2	D1	Logic Input to set period delay (t_{DP})	Connect to GND (low logic value) or to VDD (high logic value)
3	D2	Logic Input to set period delay (t_{DP})	Connect to GND (low logic value) or to VDD (high logic value)
4	VDD	Supply voltage	
5	GND	Ground	
6	DONE	Logic input for Watchdog functionality	
7	TCAL	Short duration pulse output for estimation of TPL5100 timer delay.	
8	MOS_DRV	Drives external MOSFET to power cycle the remaining system.	
9	DNC	Do Not Connect	Leave this pin floating
10	PGOOD	Digital power good input	

Absolute Maximum Ratings(1)(2)

		MIN	MAX	UNIT
Supply Voltage (VDD-GND)		-0.3	6	V
Input voltage		-0.3	VDD+0.3	V
Voltage between any two pins(3)		-0.3	VDD+0.3	V
Input Current on any pin		-5	+5	mA
Operating Temperature, TA		-40	105	°C
Storage Temperature, T_{stg}		-65	150	°C
Junction Temperature, TJ(4)			150	°C
ESD Rating	Human Body Model(5)		1000	V
	Charged Device Model		250	V

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) All voltages referenced to ground unless otherwise noted.
(3) When the input voltage (VIN) at any pin exceeds the power supply (VDD), the current on that pin must not exceed 5mA and the voltage must also not exceed 6.0V.
(4) The maximum power dissipation is a function of TJ(MAX), Î¸JA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ Î¸JA. All numbers apply for packages soldered directly onto a PC board.
(5) The human body model is a 100pF capacitor discharged through a 1.5k resistor into each pin.

Thermal Characteristics

			UNIT
$Î¸_{JA}$	Package thermal impedance(1)(2)	196.8	°C/W

(1) The maximum power dissipation is a function of TJ(MAX), Î¸JA, and the ambient temperature, TA. The maximum allowable power dissipation at any ambient temperature is PDMAX = (TJ(MAX) - TA)/ Î¸JA. All numbers apply for packages soldered directly onto a PC board.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.0	V
Temperature Range	-40	105	°C

Electrical Characteristics (1)

Specifications with standard typeface are for $T_A = T_J$ = 25°C, VDD-GND=2.5V, unless otherwise stated.

Symbol	Parameter	Conditions	Min (2)	Typ (3)	Max (2)	Units
POWER SUPPLY						
IVDD	Supply current (4)	PGOOD=VDD		30	50	nA
		PGOOD=GND		12		nA
TIMER						
t_{DP}	Timer Delay Period			16, 32, 64, 100, 128, 256, 512, 1024		s
	Timer Delay Period drift over life time (5)			0.06		%
	Timer Delay Period drift over temperature			400		ppm/°C
t_{CAL}	Calibration pulse width		14.063	15.625	17.188	ms
	t_{DP} to t_{CAL} matching error (6)	VDD<=3.0V			0.1	%
t_{DONE}	DONE Pulse width (6)		100			ns
t_{MOS_DRV}	MOS_DRV Pulse width			31.25		ms
DIGITAL LOGIC LEVELS						
VIH	Logic High Threshold	PGOOD, DONE	0.7xVDD			V
VIL	Logic Low Threshold	PGOOD, DONE			0.3xVDD	V
VOH	Logic output High Level	MOS_DRV, TCAL Iout = 100uA	VDD-0.3			V
		MOS_DRV, TCAL Iout = 1mA	VDD-0.7			V
VOL	Logic output Low Level	MOS_DRV, TCAL Iout = -100uA			0.3	V
		MOS_DRV, TCAL Iout = -1mA			0.7	V
TIMING TCAL, MOS_DRV, DONE, PGOOD - Refer to Timing Diagram						
tr_{TCAL}	Rise Time TCAL	Capacitve load 15pF		50		ns
tf_{TCAL}	Fall Time TCAL	Capacitve load 15pF		50		ns
tr_{MOS_DRV}	Rise Time MOS_DRV	Capacitve load 50pF		4		ns
tf_{MOS_DRV}	Fall Time MOS_DRV	Capacitve load 50pF		50		ns
tD_{DONE}	DONE to MOS_DRV delay	Min delay		100		ns
		Max delay		t_{DP}-5*t_{CAL}		ms
tD_{TCAL}	TCAL to MOS_DRV delay			t_{CAL}/2		ms

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) The supply current doesn't take in account load and pull-up resistor current. Input pins are at GND or VDD.
(5) Operational life time test procedure equivalent to 10 years.
(6) Guaranteed by design.

Timing Diagram

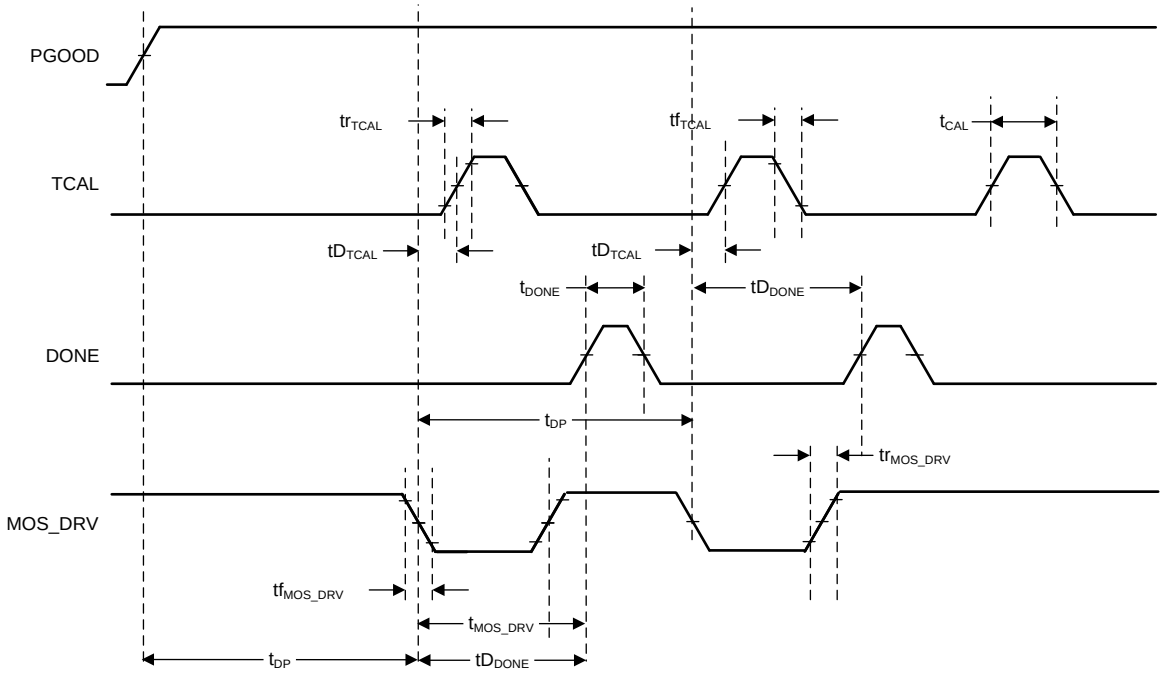
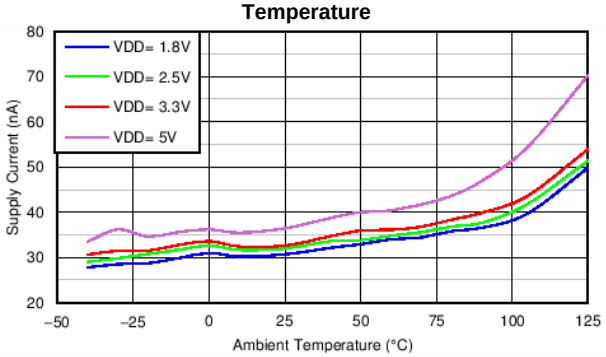


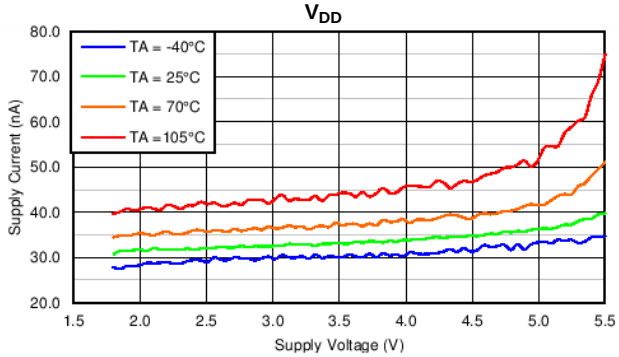
Figure 4. Timing characteristics

Typical Performance Characteristics

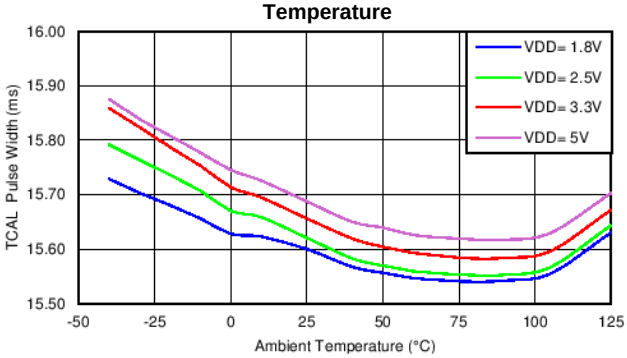
I_{DD} vs Temperature



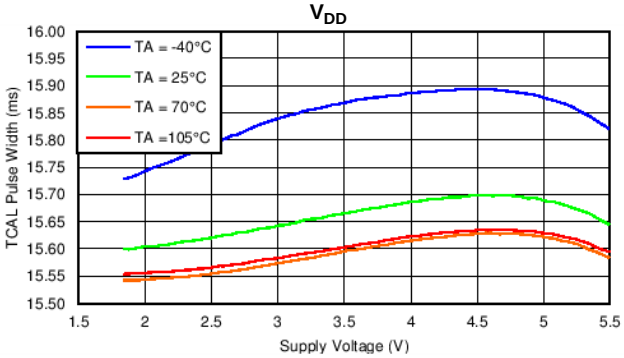
I_{DD} vs V_{DD}



TCAL Pulse Width vs Temperature



TCAL Pulse Width vs V_{DD}



APPLICATION INFORMATION

The TPL5100 is a long-term timer for low power applications. The TPL5100 is designed for use in power cycled applications and provides selectable timing from 16 seconds to 1024 seconds. An additional supervisor feature is achieved through interfacing the TPL5100 to a power management IC.

Configuration and Interface

The time interval between 2 adjacent pulses is selectable through 3 digital input pins (D0, D1, D2) that can be strapped to either VDD (1) or GND (0). Eight possible time delays can be selected, as shown in Table 1.

Table 1. Timer Delay Period

D2	D1	D0	Time (s)	Factor N
0	0	0	16	2^{10}
0	0	1	32	2^{11}
0	1	0	64	2^{12}
0	1	1	100	$100*2^{6}$
1	0	0	128	2^{13}
1	0	1	256	2^{14}
1	1	0	512	2^{15}
1	1	1	1024	2^{16}

Overview of the Timing Signals MOS_DRV, TCAL and DONE

Figure 5 shows the timing of PGOOD, MOS_DRV, and TCAL with respect to DONE. The frame, A, shows a typical sequence after the PGOOD, low to high, transition. As soon as PGOOD is high, the internal oscillator is powered ON. At the end of the delay period (t_{DP}), a MOS enable signal (MOS_DRV), followed by a calibration pulse, TCAL, is sent out. The calibration pulse starts after a half period of the internal oscillator from the falling edge of the MOS_DRV signal, and lasts one internal oscillator period. A "DONE" signal is received before the end of the MOS_DRV pulse. As soon as the TPL5100 receives the DONE signal, the counter resets and MOS_DRV and TCAL return to default conditions (MOS_DRV signal high and TCAL signal low).

The frame, B, shows a non-standard sequence. A "DONE" signal has not been received before the end of the MOS_DRV pulse. The MOS_DRV signal stays low for 2 internal oscillator periods. The calibration pulse starts after a half period of the internal oscillator from the falling edge of the MOS_DRV signal, and lasts one internal oscillator period. The external power gating MOS stays ON for 2 internal oscillator periods.

The frame, C, shows a standard sequence, but in this case, the TPL5100 receives the DONE signal when MOS_DRV is high and TCAL pulse is still high. As soon as the TPL5100 recognizes the DONE signal, the counter resets and MOS_DRV and TCAL return to default conditions (MOS_DRV signal high and TCAL signal low).The external power gating MOS stays ON for the execution time of the program of the connected µC.

The frame, D, shows a typical PGOOD, high to low transition. As soon as PGOOD is low, the internal oscillator is powered OFF and the digital output pins, TCAL and MOS_DRV, are asynchronously reset by the falling edge of the PGOOD signal, such that TCAL resets at low logical values, while MOS_DRV resets at a high logical value. The external power gating MOS stays ON less than the execution time of the program of the connected µC.

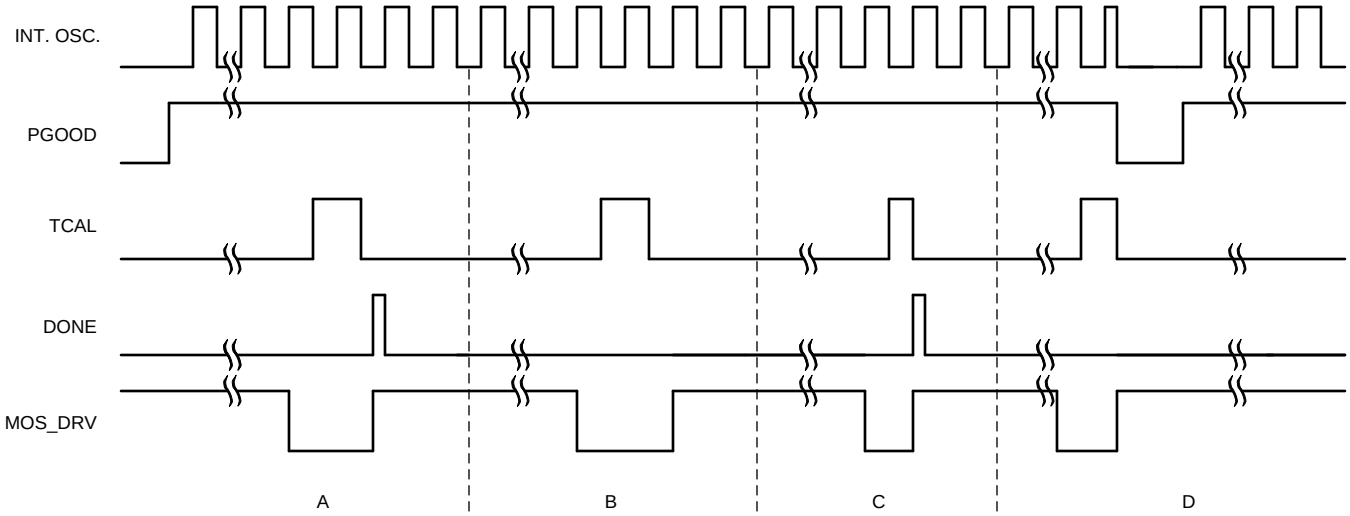


Figure 5. Timing MOS_DRV, TCAL

Supervisor Feature

A critical event that can corrupt the memory of a µC is a voltage supply drop (supply lower than minimum operating range), and a reset of the µC is mandatory if this occurs. Since the TPL5100 is the right choice in systems which stay most of the time in deep sleep or completely OFF, due to its ultra low power consumption, it is fundamental that it takes into account the voltage drop events. The TPL5100 implements the supervisor feature when working with some power management ICs, which indicate the status of the supply voltage with a power good or battery good output. The supervisory functionality is enabled by simply connecting the Battery management power good output to the TPL5100 PGOOD pin. If this feature is not used connect the PGOOD pin to VDD.

In case the power management IC detects a voltage drop while the µC is OFF, consequently lowering the PGOOD line, the TPL5100 resets its internal counter and does not allow the micro to turn ON until the PGOOD is high again. This series of events allows the µC to avoid working in an unsafe voltage supply condition. If the PGOOD signal is lowered while the µC is ON, the TPL51000 turns the µC OFF. The micro will be turned ON when PGOOD is high again and the selected delay is elapsed.

Calibration Pulse

The TPL5100 is based on an ultra-low power oscillator, which has a relatively low frequency and low accuracy; however, it shows very good cycle to cycle repeatability and very low temperature drift. In most of the applications, the accuracy of the oscillator is enough, but if a more accurate measure of the delay period is required, it is possible to measure the base period of the internal oscillator. A single pulse, which has the same duration as the base period of the internal oscillator, is present at the TCAL pin of the TPL5100. This pulse starts after a half period of the internal oscillator, from the falling edge of the MOS_DRV pulse.

A µC connected to the TPL5100 can routinely measure the width of the TCAL pulse, using a counter and an external crystal. Once the base period of the TPL5100 is measured, the actual time delay is calculated by multiplying the measured period by a factor, N (see Table 1), dependent upon the nominal selected time delay.

The resolution and the accuracy of the measurement depend upon the external crystal. Since the frequency of the internal oscillator of the TPL5100 is very stable, the measurement of the calibration pulse is suggested only when a high gradient of ambient temperature is observed. The measurement of the TCAL pulse is useful in battery-powered applications that implement a precise battery life counter in the µC.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5100DGSR	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	ASAA	Samples
TPL5100DGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 105	ASAA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

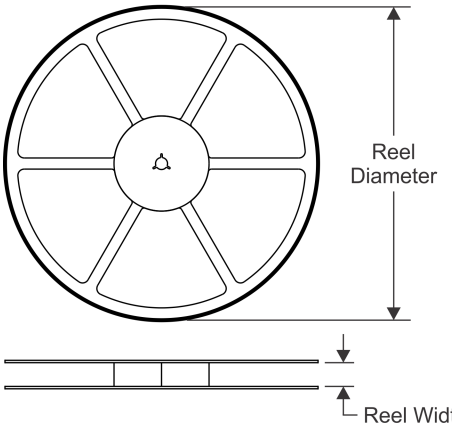
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

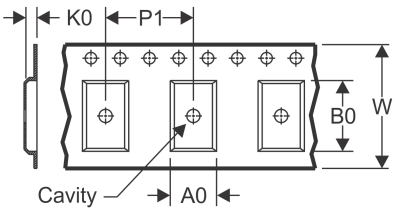
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

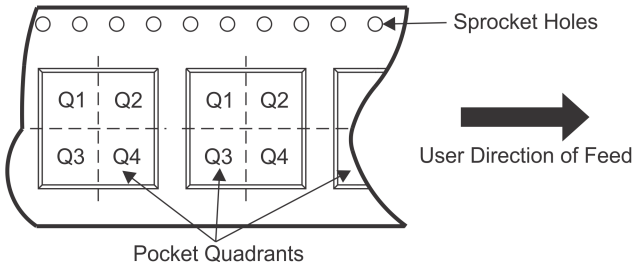


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

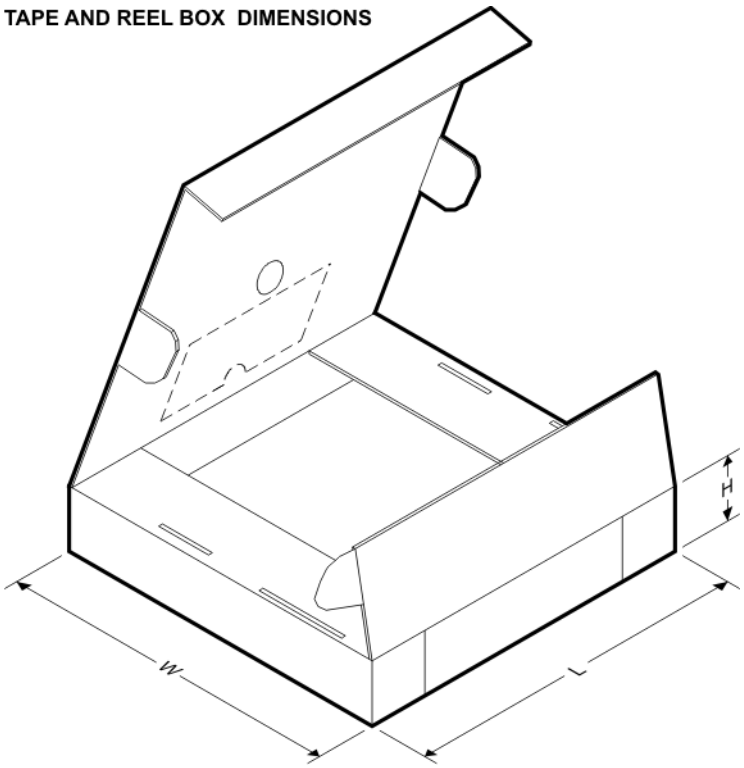
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5100DGST	VSSOP	DGS	10	250	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

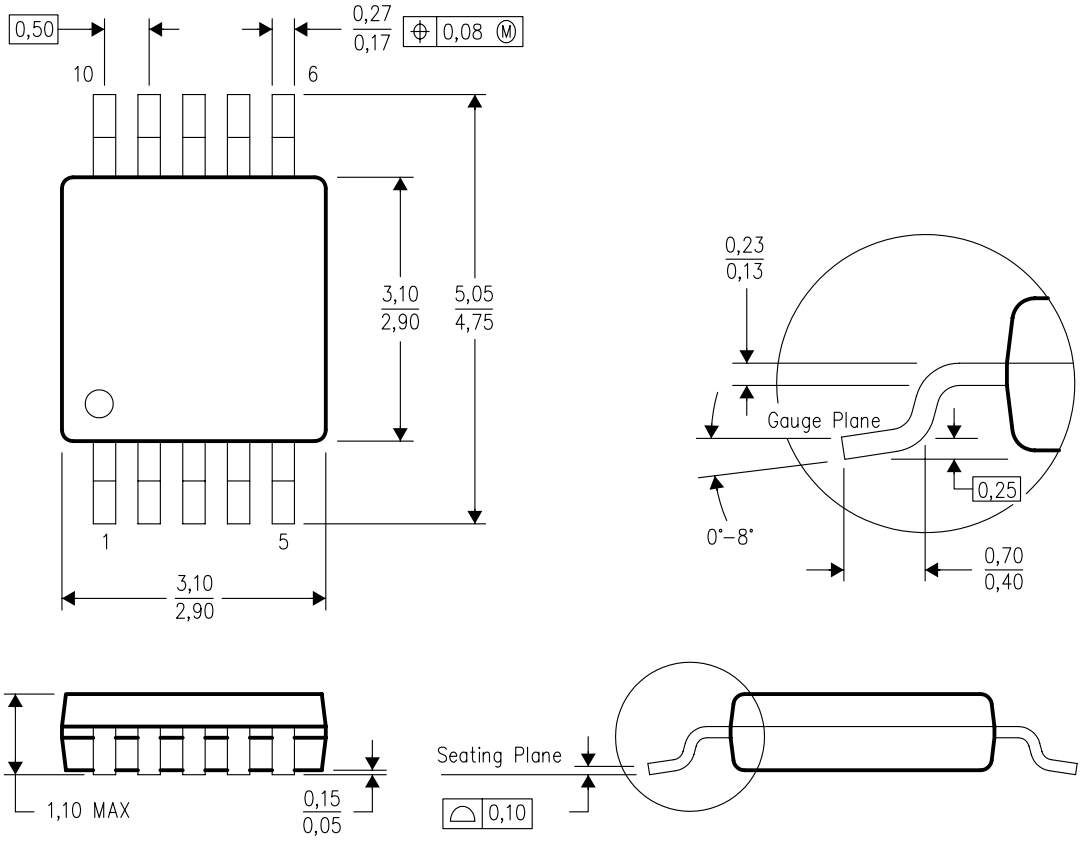
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5100DGST	VSSOP	DGS	10	250	210.0	185.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265