Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB2.6	Standard I/O	29	B13	XBR1	✓	AD11m/ A3		Yes	INT0.6 INT1.6	
PB2.7	Standard I/O	28	A17	XBR1	✓	AD10m/ A2		Yes	INT0.7 INT1.7	
PB2.8	Standard I/O	27	B12	XBR1	✓	AD9m/ A1		Yes		
PB2.9	Standard I/O	26	A16	XBR1	✓	AD8m/ A0		Yes		
PB2.10	Standard I/O	25	B11	XBR1	✓	AD7m/ D7		Yes		
PB2.11	Standard I/O	24	A15	XBR1	✓	AD6m/ D6		Yes		CMP0P.0 CMP1P.0
PB2.12	Standard I/O	23	A14	XBR1	✓	AD5m/ D5		Yes		CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.13	Standard I/O	22	A13	XBR1	✓	AD4m/ D4		Yes		CMP0P.1 CMP1P.1
PB2.14	Standard I/O	21	D2	XBR1	✓	AD3m/ D3		Yes		CMP0N.1 CMP1N.1
PB3.0	5 V Tolerant I/O	20	A12	XBR1	✓	AD2m/ D2				CMP0P.2 CMP1P.2
PB3.1	5 V Tolerant I/O	19	A11	XBR1	✓	AD1m/ D1				CMP0N.2 CMP1N.2
PB3.2	5 V Tolerant I/O	18	A10	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0	CMP0P.3 CMP1P.3
PB3.3	5 V Tolerant I/O	17	B8	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.8 INT1.8	CMP0N.3 CMP1N.3

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.4	5 V Tolerant I/O	16	A9	XBR1	✓	$\overline{OE}$			INT0.9 INT1.9 WAKE.8	CMP0P.4 CMP1P.4
PB3.5	5 V Tolerant I/O	15	B7	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.10 INT1.10 WAKE.9	CMP0N.4 CMP1N.4
PB3.6	5 V Tolerant I/O	14	A8	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.11 INT1.11 WAKE.10	CMP0P.5 CMP1P.5
PB3.7	5 V Tolerant I/O	13	B6	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 LPT0T1 INT0.12 INT1.12 WAKE.11	CMP0N.5 CMP1N.5
PB3.8	5 V Tolerant I/O	12	A7	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T2 INT0.13 INT1.13 WAKE.12	CMP0P.6 CMP1P.6 EXREGSP
PB3.9	5 V Tolerant I/O	11	B5	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 INT0.14 INT1.14 WAKE.13	CMP0N.6 CMP1N.6 EXREGSN
PB3.10	5 V Tolerant I/O	10	B4	XBR1	✓				INT0.15 INT1.15 WAKE.14	CMP0P.7 CMP1P.7 EXREGOUT
PB3.11	5 V Tolerant I/O	9	B3	XBR1	✓				WAKE.15	CMP0N.7 CMP1N.7 EXREGBD

Table 6.1. Pin Definitions and alternate functions for SiM3C1x7 (Continued)

Pin Name	Type	Pin Numbers TQFP-80	Pin Numbers LGA-92	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB4.0	High Drive I/O	8	A6				LSO0			
PB4.1	High Drive I/O	7	A5				LSO1			
PB4.2	High Drive I/O	6	A4				LSO2			
PB4.3	High Drive I/O	3	A2				LSO3			
PB4.4	High Drive I/O	2	A1				LSO4			
PB4.5	High Drive I/O	1	D1				LSO5			

Note: All unnamed pins on the LGA-92 package are no-connect pins. They should be soldered to the PCB for mechanical stability, but have no internal connections to the device.

6.2. SiM3C1x6 Pin Definitions

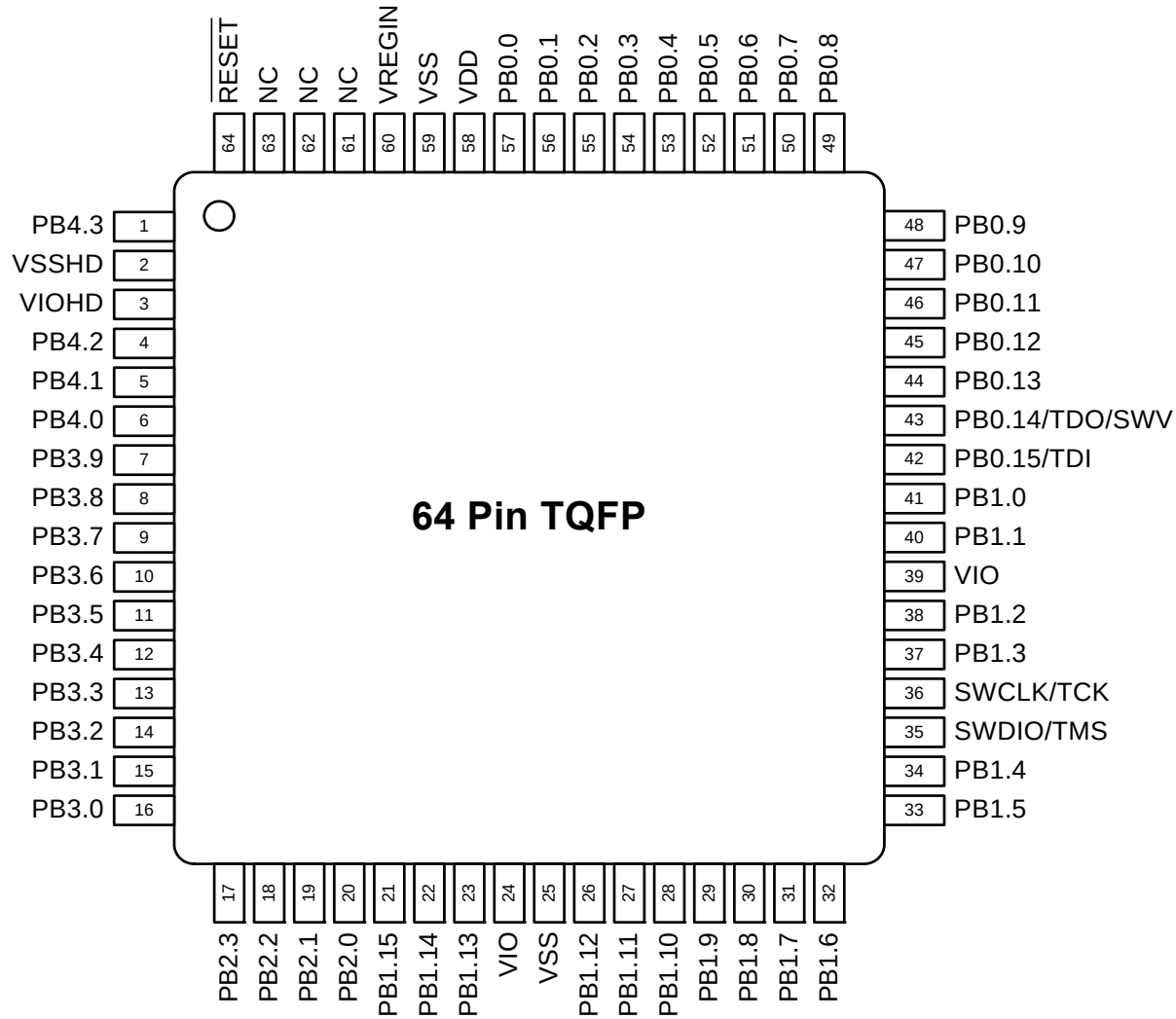

Figure 6.3. SiM3C1x6-GQ Pinout

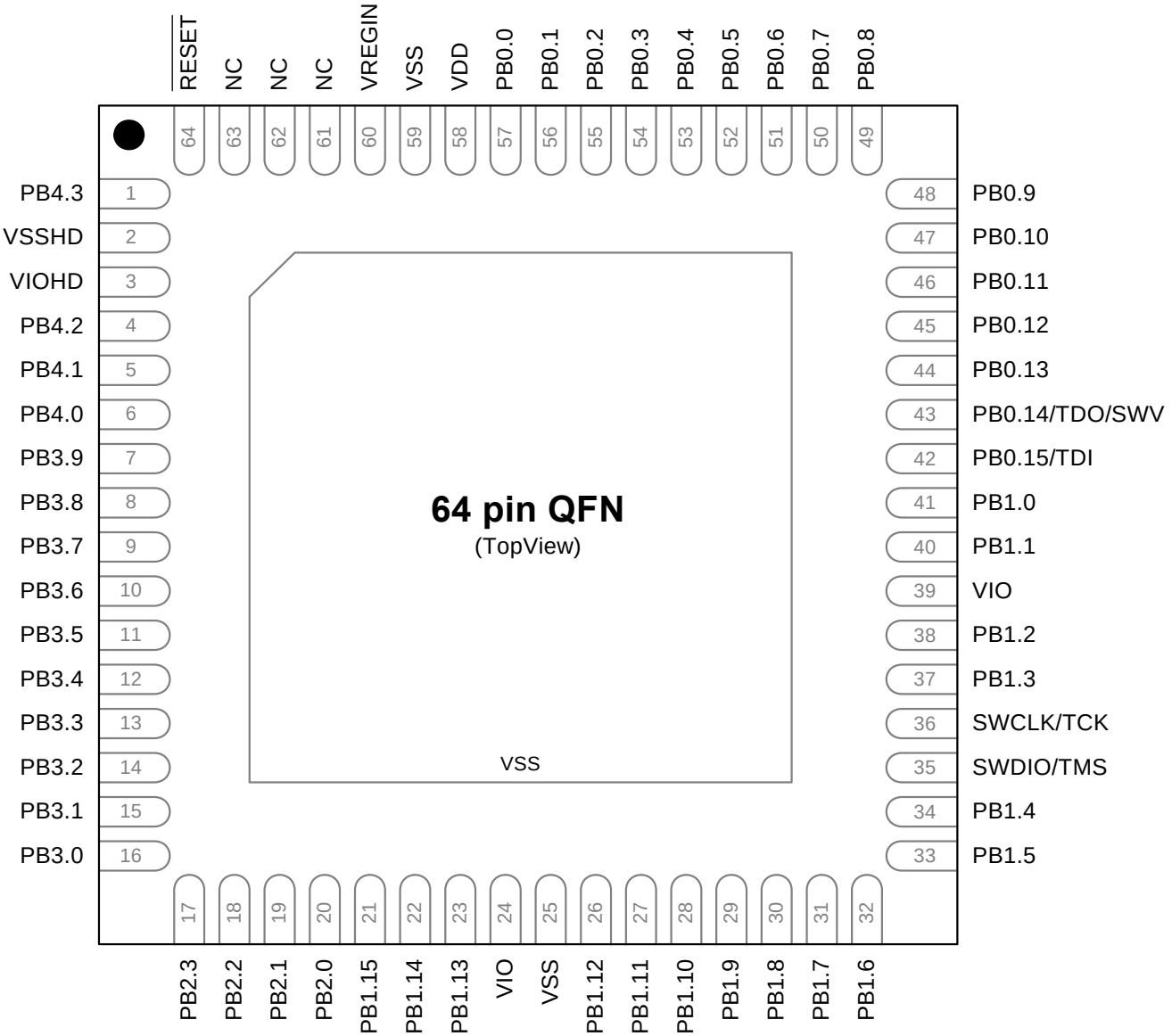

Figure 6.4. SiM3C1x6-GM Pinout

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	25 59							
VDD	Power (Core)	58							
VIO	Power (I/O)	24 39							
VREGIN	Power (Regulator)	60							
VSSHD	Ground (High Drive)	2							
VIOHD	Power (High Drive)	3							
$\overline{\text{RESET}}$	Active-low Reset	64							
SWCLK/TCK	Serial Wire / JTAG	36							
SWDIO/TMS	Serial Wire / JTAG	35							
PB0.0	Standard I/O	57	XBR0	✓					ADC0.2 CS0.1
PB0.1	Standard I/O	56	XBR0	✓					ADC0.3 CS0.2
PB0.2	Standard I/O	55	XBR0	✓					ADC0.4 CS0.3
PB0.3	Standard I/O	54	XBR0	✓					ADC0.5 CS0.4
PB0.4	Standard I/O	53	XBR0	✓					ADC0.6 CS0.5 IVC0.0
PB0.5	Standard I/O	52	XBR0	✓					ADC0.7 CS0.6 IVC0.1
PB0.6	Standard I/O	51	XBR0	✓					ADC0.8 CS0.7 RTC1

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.7	Standard I/O	50	XBR0	✓					RTC2
PB0.8	Standard I/O	49	XBR0	✓					ADC0.9 VREFGND
PB0.9	Standard I/O	48	XBR0	✓					ADC0.10 VREF
PB0.10	Standard I/O	47	XBR0	✓					ADC1.6 IDAC0
PB0.11	Standard I/O	46	XBR0	✓					IDAC1
PB0.12	Standard I/O	45	XBR0	✓					XTAL1
PB0.13	Standard I/O	44	XBR0	✓					XTAL2
PB0.14/TDO/ SWV	Standard I/O / JTAG / Serial Wire Viewer	43	XBR0	✓					ADC0.12 ADC1.12
PB0.15/TDI	Standard I/O / JTAG	42	XBR0	✓					ADC0.13 ADC1.13
PB1.0	Standard I/O	41	XBR0	✓					ADC0.14 ADC1.14
PB1.1	Standard I/O	40	XBR0	✓					ADC0.15 ADC1.15
PB1.2	Standard I/O	38	XBR0	✓					ADC1.11 CS0.8
PB1.3	Standard I/O	37	XBR0	✓					ADC1.10 CS0.9
PB1.4	Standard I/O	34	XBR0	✓					ADC1.8
PB1.5	Standard I/O	33	XBR0	✓					ADC1.7
PB1.6	Standard I/O	32	XBR0	✓				ADC0T15 WAKE.0	ADC1.5 CS0.10
PB1.7	Standard I/O	31	XBR0	✓	AD15m/ A7			ADC1T15 WAKE.1	ADC1.4 CS0.11

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB1.8	Standard I/O	30	XBR0	✓	AD14m/ A6			WAKE.2	ADC1.3 CS0.12
PB1.9	Standard I/O	29	XBR0	✓	AD13m/ A5			WAKE.3	ADC1.2 CS0.13
PB1.10	Standard I/O	28	XBR0	✓	AD12m/ A4			DMA0T1 WAKE.4	ADC1.1 CS0.14
PB1.11	Standard I/O	27	XBR0	✓	AD11m/ A3			DMA0T0 WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.12	Standard I/O	26	XBR0	✓	AD10m/ A2			WAKE.6	
PB1.13	Standard I/O	23	XBR0	✓	AD9m/ A1				
PB1.14	Standard I/O	22	XBR0	✓	AD8m/ A0				
PB1.15	Standard I/O	21	XBR0	✓	AD7m/ D7				
PB2.0	Standard I/O	20	XBR1	✓	AD6m/ D6	LSI0	Yes	INT0.0 INT1.0	
PB2.1	Standard I/O	19	XBR1	✓	AD5m/ D5	LSI1	Yes	INT0.1 INT1.1	
PB2.2	Standard I/O	18	XBR1	✓	AD4m/ D4	LSI2	Yes	INT0.2 INT1.2	CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB2.3	Standard I/O	17	XBR1	✓	AD3m/ D3	LSI3	Yes	INT0.3 INT1.3	CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	16	XBR1	✓	AD2m/ D2				CMP0P.1 CMP1P.1
PB3.1	5 V Tolerant I/O	15	XBR1	✓	AD1m/ D1				CMP0N.1 CMP1N.1

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.2	5 V Tolerant I/O	14	XBR1	✓	AD0m/ D0			DAC0T0 DAC1T0 LPT0T0 WAKE.8	CMP0P.2 CMP1P.2
PB3.3	5 V Tolerant I/O	13	XBR1	✓	$\overline{WR}$			DAC0T1 DAC1T1 INT0.4 INT1.4 WAKE.9	CMP0N.2 CMP1N.2
PB3.4	5 V Tolerant I/O	12	XBR1	✓	$\overline{OE}$			INT0.5 INT1.5 WAKE.10	CMP0P.3 CMP1P.3
PB3.5	5 V Tolerant I/O	11	XBR1	✓	ALEm			DAC0T2 DAC1T2 INT0.6 INT1.6 WAKE.11	CMP0N.3 CMP1N.3
PB3.6	5 V Tolerant I/O	10	XBR1	✓	CS0			DAC0T3 DAC1T3 INT0.7 INT1.7 WAKE.12	CMP0P.4 CMP1P.4 EXREGSP
PB3.7	5 V Tolerant I/O	9	XBR1	✓	$\overline{BE1}$			DAC0T4 DAC1T4 INT0.8 INT1.8 WAKE.13	CMP0N.4 CMP1N.4 EXREGSN
PB3.8	5 V Tolerant I/O	8	XBR1	✓	CS1			DAC0T5 DAC1T5 LPT0T1 INT0.9 INT1.9 WAKE.14	CMP0P.5 CMP1P.5 EXREGOUT

Table 6.2. Pin Definitions and alternate functions for SiM3C1x6 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	External Memory Interface (m = muxed mode)	Port-Mapped Level Shifter	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.9	5 V Tolerant I/O	7	XBR1	✓	$\overline{BE0}$			DAC0T6 DAC1T6 LPT0T2 INT0.10 INT1.10 WAKE.15	CMP0N.5 CMP1N.5 EXREGBD
PB4.0	High Drive I/O	6				LSO0			
PB4.1	High Drive I/O	5				LSO1			
PB4.2	High Drive I/O	4				LSO2			
PB4.3	High Drive I/O	1				LSO3			

6.3. SiM3C1x4 Pin Definitions

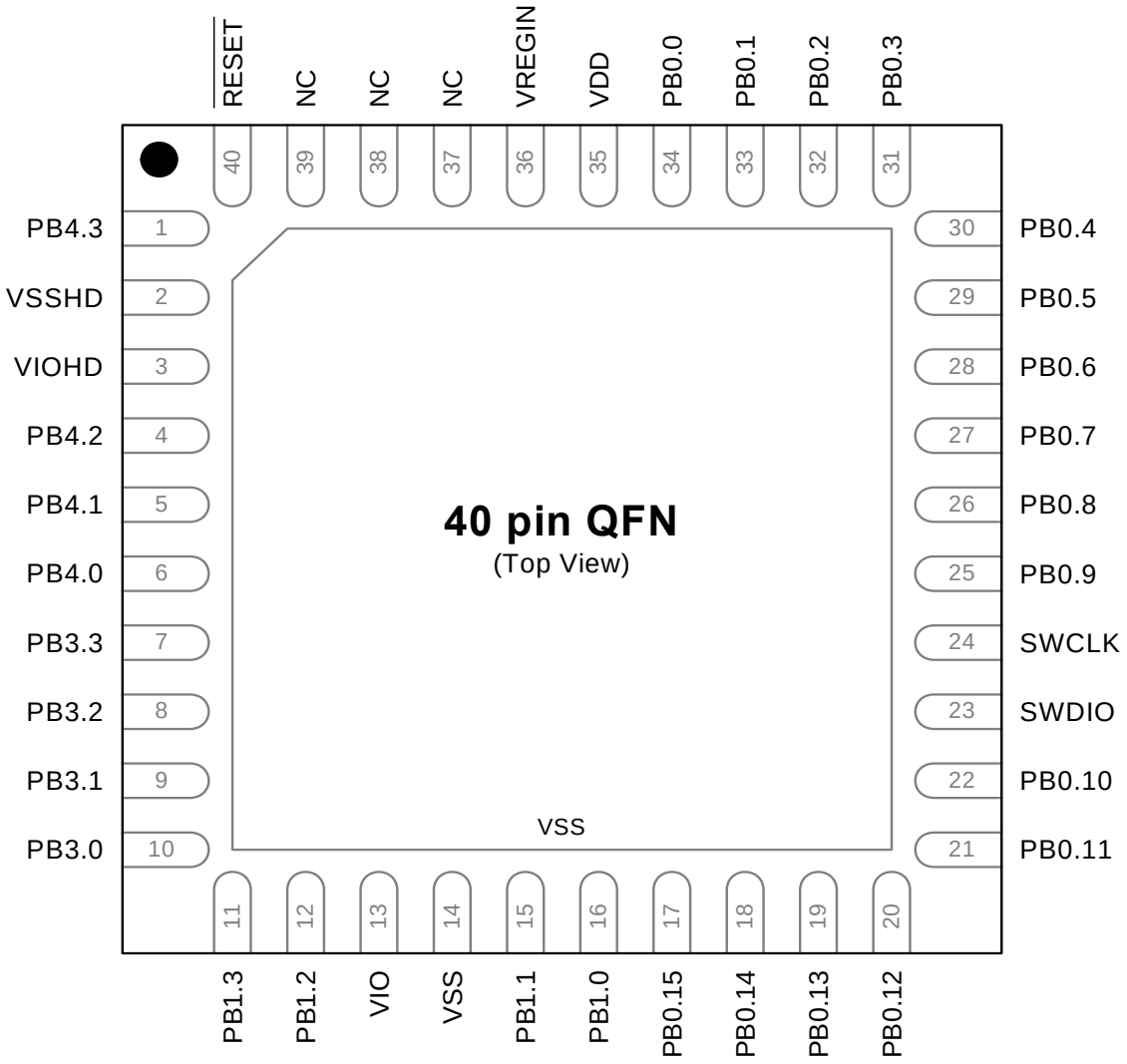

Figure 6.5. SiM3C1x4-GM Pinout

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
VSS	Ground	14					
VDD	Power (Core)	35					
VIO	Power (I/O)	13					
VREGIN	Power (Regulator)	36					
VSSHD	Ground (High Drive)	2					
VIOHD	Power (High Drive)	3					
$\overline{\text{RESET}}$	Active-low Reset	40					
SWCLK	Serial Wire	24					
SWDIO	Serial Wire	23					
PB0.0	Standard I/O	34	XBR0	✓			ADC0.8 CS0.7 RTC1
PB0.1	Standard I/O	33	XBR0	✓			RTC2
PB0.2	Standard I/O	32	XBR0	✓			ADC0.9 CS0.0 VREFGND
PB0.3	Standard I/O	31	XBR0	✓			ADC0.10 CS0.1 VREF
PB0.4	Standard I/O	30	XBR0	✓			ADC1.6 CS0.2 IDAC0
PB0.5	Standard I/O	29					IDAC1
PB0.6	Standard I/O	28	XBR0	✓			ADC0.0 CS0.3 XTAL1
PB0.7	Standard I/O	27	XBR0	✓			ADC0.1 CS0.4 XTAL2

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB0.8	Standard I/O	26	XBR0	✓			ADC0.14 ADC1.14
PB0.9	Standard I/O	25	XBR0	✓			ADC0.15 ADC1.15
PB0.10	Standard I/O	22	XBR0	✓		DMA0T1	ADC1.8
PB0.11	Standard I/O	21	XBR0	✓		DMA0T0	ADC1.7
PB0.12	Standard I/O	20	XBR0	✓		ADC0T15 WAKE.0	ADC1.5 CS0.10
PB0.13	Standard I/O	19	XBR0	✓		ADC1T15 WAKE.1	ADC1.4 CS0.11
PB0.14	Standard I/O	18	XBR0	✓		WAKE.2	ADC1.3 CS0.12
PB0.15	Standard I/O	17	XBR0	✓		WAKE.3	ADC1.2 CS0.13
PB1.0	Standard I/O	16	XBR0	✓		WAKE.4	ADC1.1 CS0.14
PB1.1	Standard I/O	15	XBR0	✓		WAKE.5	ADC1.0 CS0.15 PMU_Asleep
PB1.2	Standard I/O	12	XBR0	✓			CMP0N.0 CMP1N.0 RTC0TCLK_OUT
PB1.3	Standard I/O	11	XBR0	✓			CMP0P.0 CMP1P.0
PB3.0	5 V Tolerant I/O	10	XBR1	✓		DAC0T0 DAC1T0 LPT0T0 INT0.0 INT1.0 WAKE.12	CMP0P.1 CMP1P.1 EXREGSP

Table 6.3. Pin Definitions and Alternate Functions for SiM3C1x4 (Continued)

Pin Name	Type	Pin Numbers	Crossbar Capability (see Port Config Section)	Port Match	Output Toggle Logic	External Trigger Inputs	Analog or Additional Functions
PB3.1	5 V Tolerant I/O	9	XBR1	✓		DAC0T1 DAC1T1 LPT0T1 INT0.1 INT1.1 WAKE.13	CMP0N.1 CMP1N.1 EXREGSN
PB3.2	5 V Tolerant I/O	8	XBR1	✓		DAC0T2 DAC1T2 LPT0T2 INT0.2 INT1.3 WAKE.14	CMP0P.2 CMP1P.2 EXREGOUT
PB3.3	5 V Tolerant I/O	7	XBR1	✓		DAC0T3 DAC1T3 INT0.3 INT1.3 WAKE.15	CMP0N.2 CMP1N.2 EXREGBD
PB4.0	High Drive I/O	6					
PB4.1	High Drive I/O	5					
PB4.2	High Drive I/O	4					
PB4.3	High Drive I/O	1					

6.4. LGA-92 Package Specifications

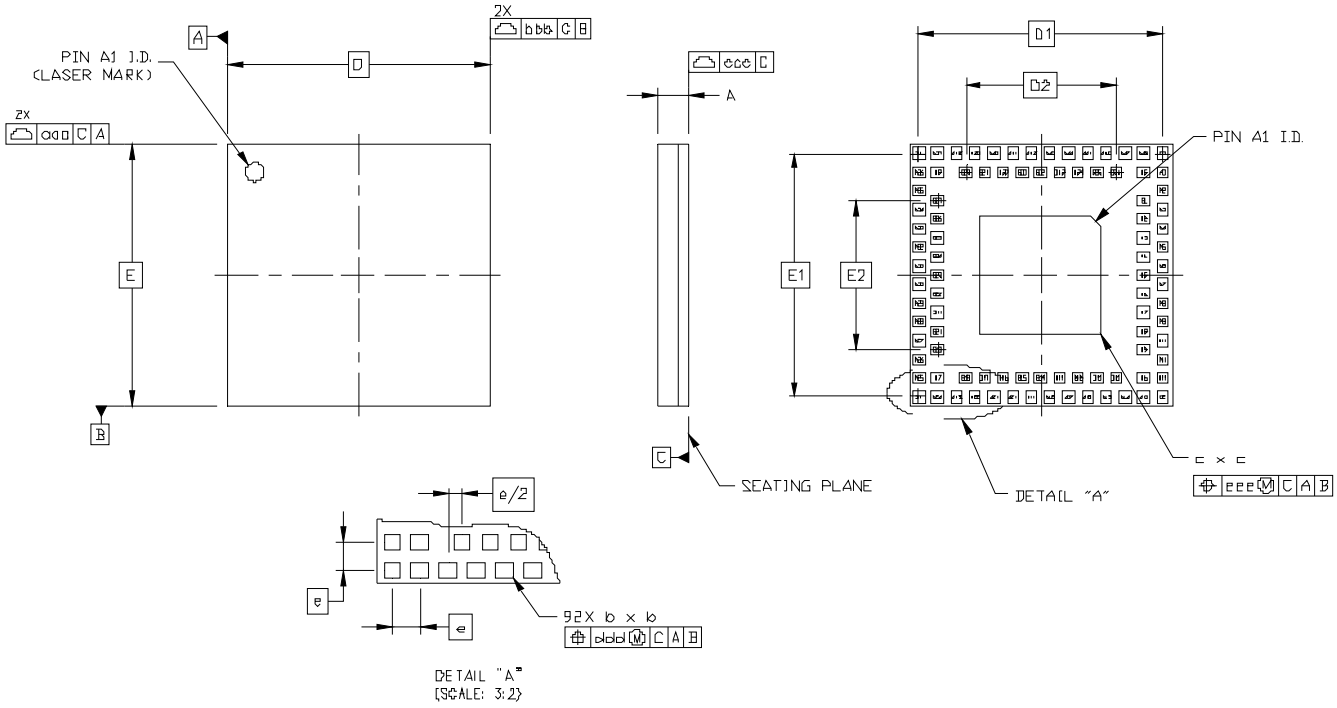

Figure 6.6. LGA-92 Package Drawing

Table 6.4. LGA-92 Package Dimensions

Dimension	Min	Nominal	Max
A	0.74	0.84	0.94
b	0.25	0.30	0.35
c	3.15	3.20	3.25
D		7.00 BSC	
D1		6.50 BSC	
D2		4.00 BSC	
e		0.50 BSC	
E		7.00 BSC	
E1		6.50 BSC	
E2		4.00 BSC	
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

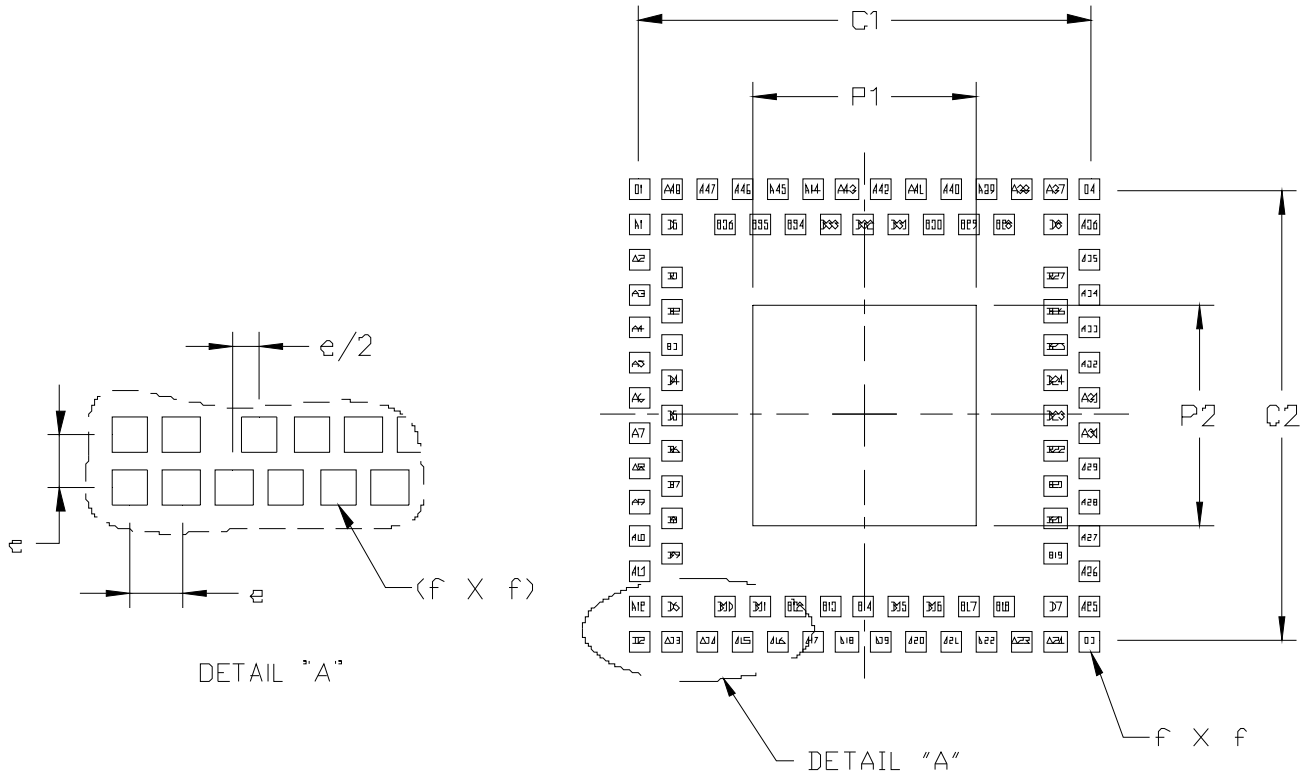

Figure 6.7. LGA-92 Landing Diagram

Table 6.5. LGA-92 Landing Diagram Dimensions

Dimension	Typical	Max
C1	6.50	—
C2	6.50	—
e	0.50	—
f	—	0.35
P1	—	3.20
P2	—	3.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
3. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
4. This land pattern design is based on the IPC-7351 guidelines.

6.4.1. LGA-92 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.4.2. LGA-92 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
4. A 2 x 2 array of 1.25 mm square openings on 1.60 mm pitch should be used for the center ground pad.

6.4.3. LGA-92 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.5. TQFP-80 Package Specifications

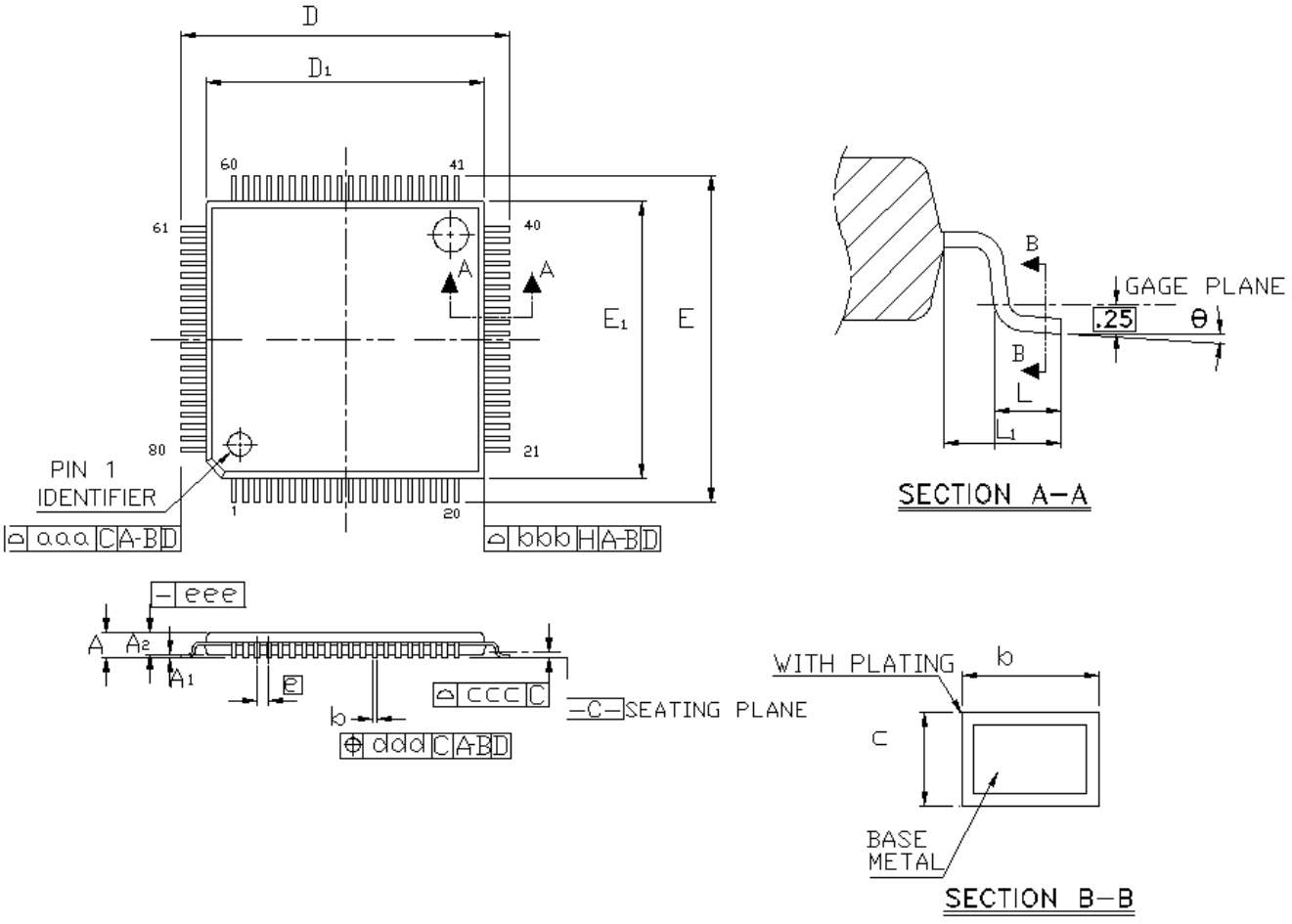

Figure 6.8. TQFP-80 Package Drawing

Table 6.6. TQFP-80 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.20	0.27
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.50 BSC		
E	14.00 BSC		
E1	12.00 BSC		

Table 6.6. TQFP-80 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
L	0.45	0.60	0.75
L1		1.00 Ref	
Θ	0°	3.5°	7°
aaa		0.20	
bbb		0.20	
ccc		0.08	
ddd		0.08	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ADD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

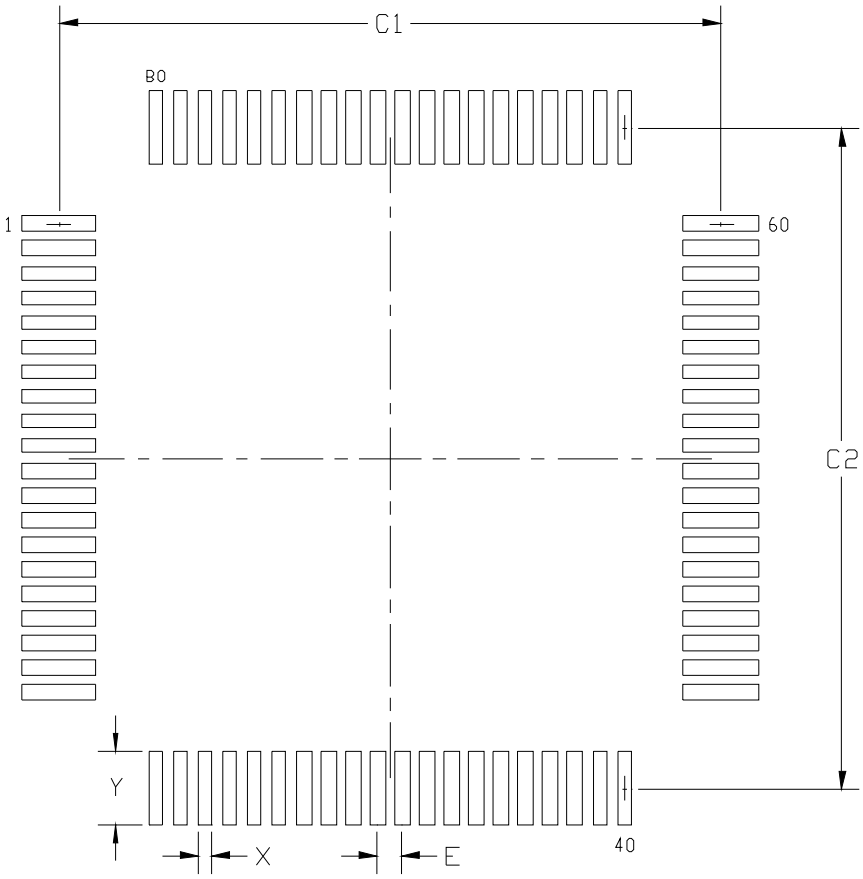

Figure 6.9. TQFP-80 Landing Diagram

Table 6.7. TQFP-80 Landing Diagram Dimensions

Dimension	Min	Max
C1	13.30	13.40
C2	13.30	13.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.5.1. TQFP-80 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.5.2. TQFP-80 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.5.3. TQFP-80 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.6. QFN-64 Package Specifications

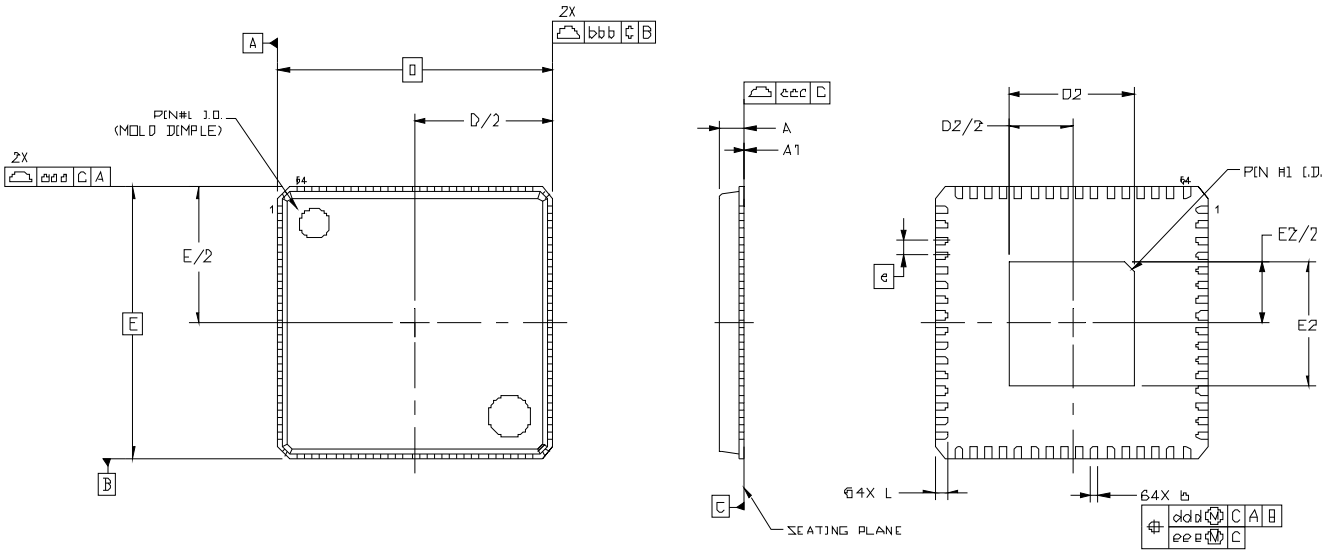

Figure 6.10. QFN-64 Package Drawing

Table 6.8. QFN-64 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		9.00 BSC	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

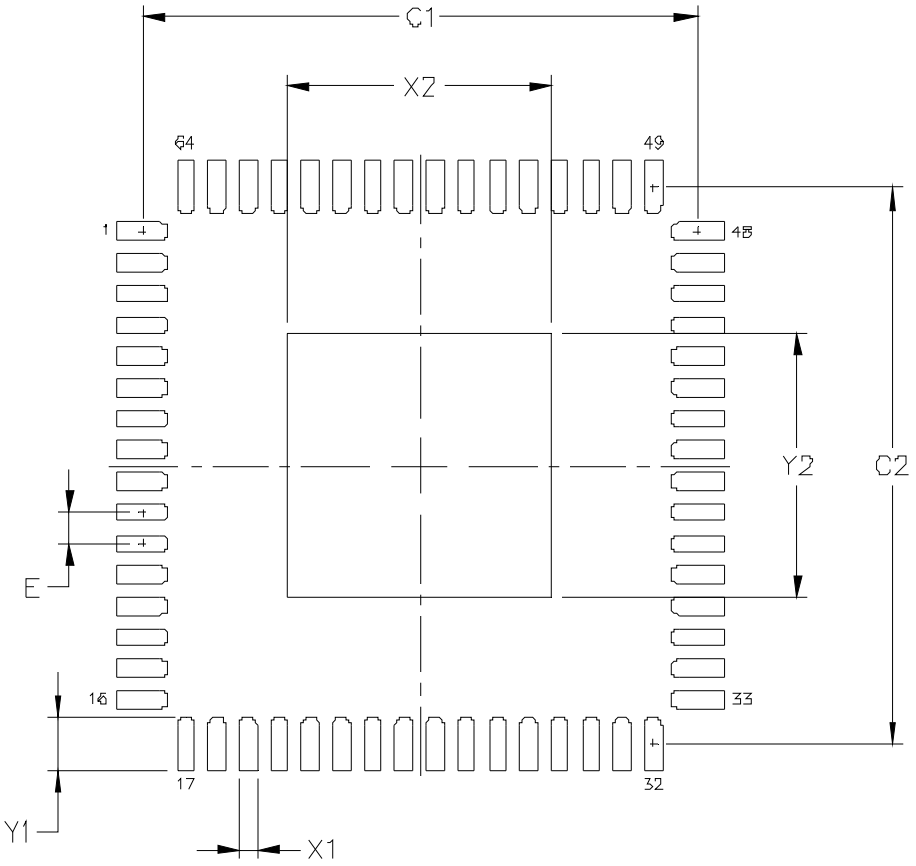

Figure 6.11. QFN-64 Landing Diagram

Table 6.9. QFN-64 Landing Diagram Dimensions

Dimension	mm
C1	8.90
C2	8.90
E	0.50
X1	0.30
Y1	0.85
X2	4.25
Y2	4.25

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

6.6.1. QFN-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.6.2. QFN-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.0 mm square openings on a 1.5 mm pitch should be used for the center ground pad.

6.6.3. QFN-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.7. TQFP-64 Package Specifications

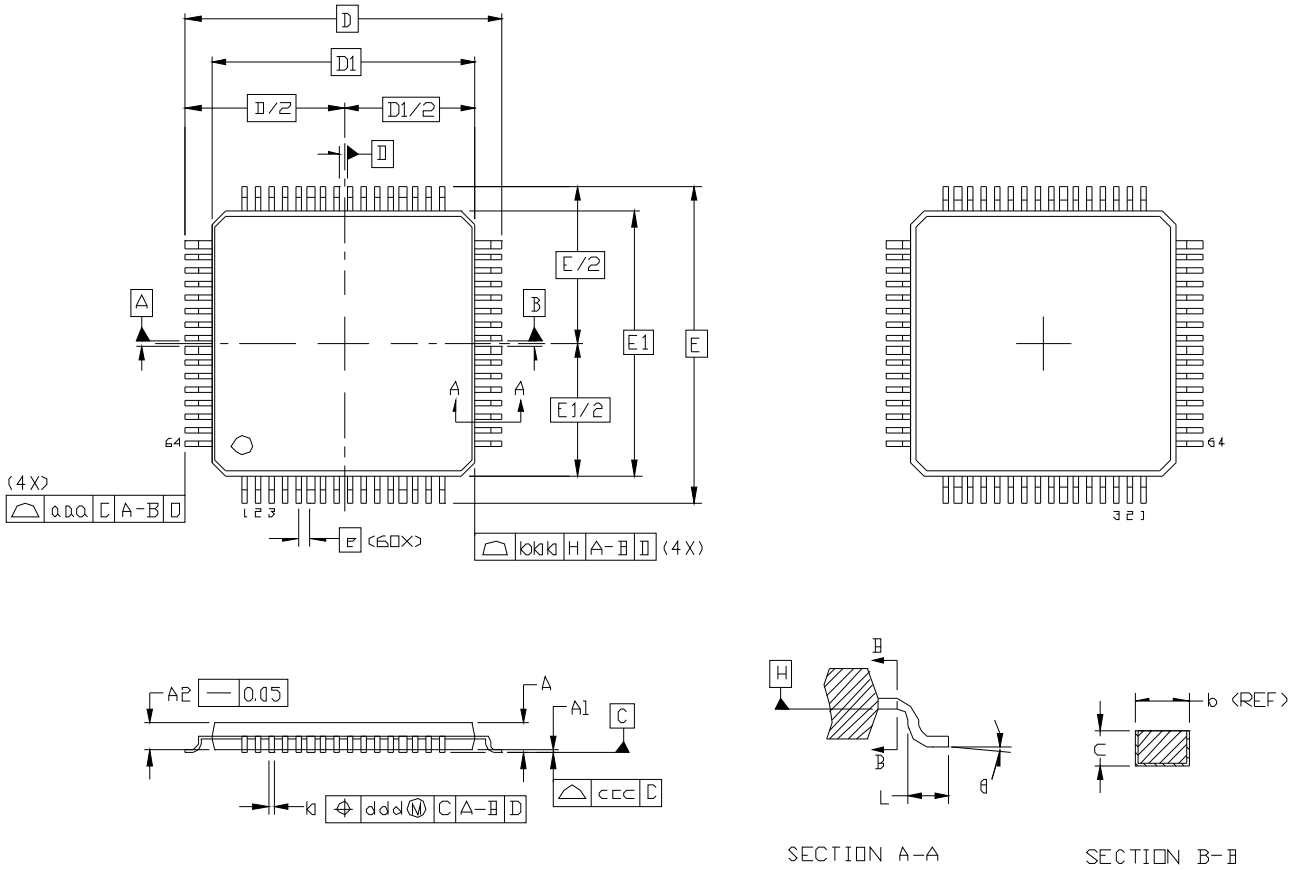

Figure 6.12. TQFP-64 Package Drawing

Table 6.10. TQFP-64 Package Dimensions

Dimension	Min	Nominal	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
L	0.45	0.60	0.75
Θ	0°	3.5°	7°

Table 6.10. TQFP-64 Package Dimensions (Continued)

Dimension	Min	Nominal	Max
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

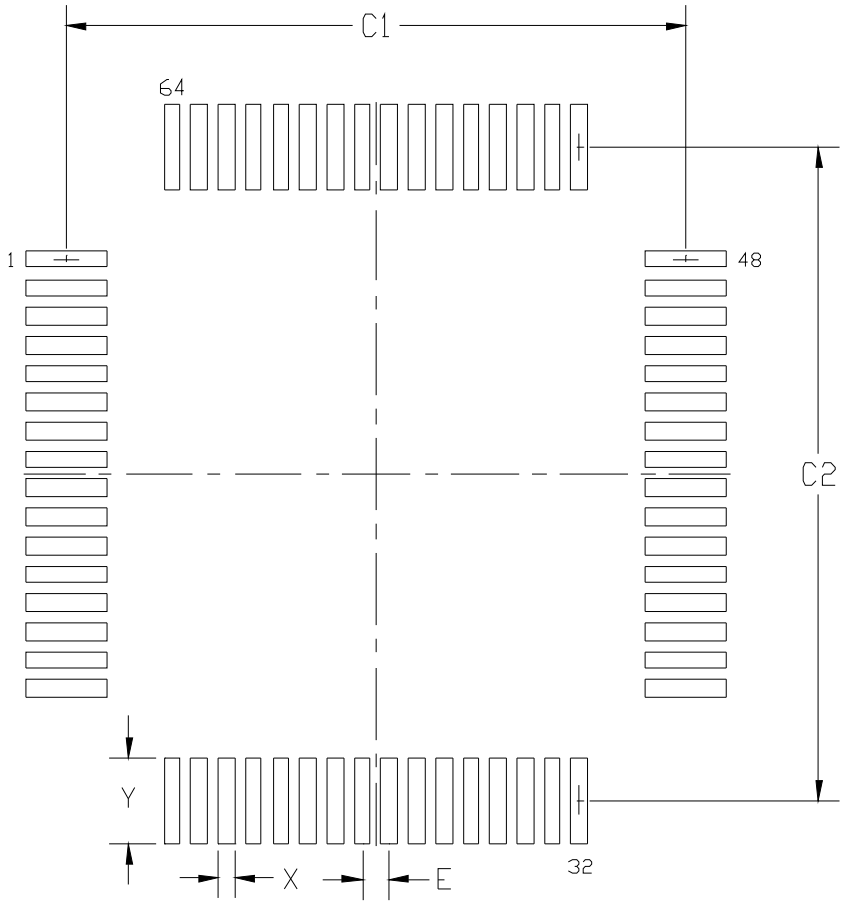

Figure 6.13. TQFP-64 Landing Diagram

Table 6.11. TQFP-64 Landing Diagram Dimensions

Dimension	Min	Max
C1	11.30	11.40
C2	11.30	11.40
E	0.50 BSC	
X	0.20	0.30
Y	1.40	1.50

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

6.7.1. TQFP-64 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.7.2. TQFP-64 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

6.7.3. TQFP-64 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.8. QFN-40 Package Specifications

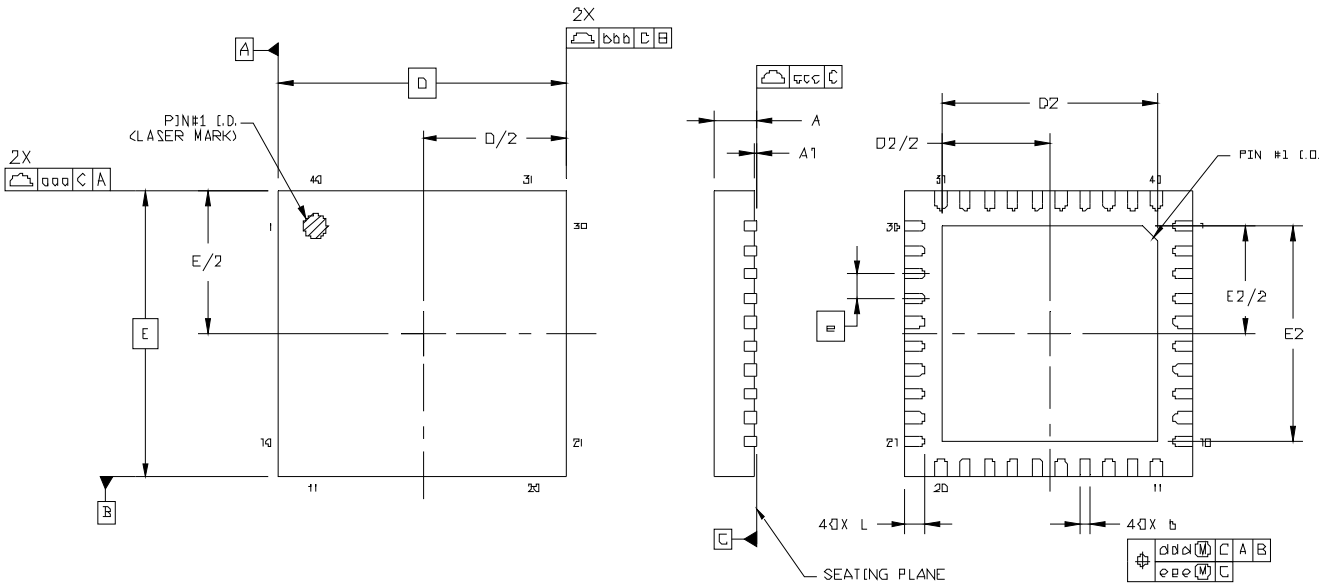

Figure 6.14. QFN-40 Package Drawing

Table 6.12. QFN-40 Package Dimensions

Dimension	Min	Nominal	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E		6.00 BSC	
E2	4.35	4.5	4.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

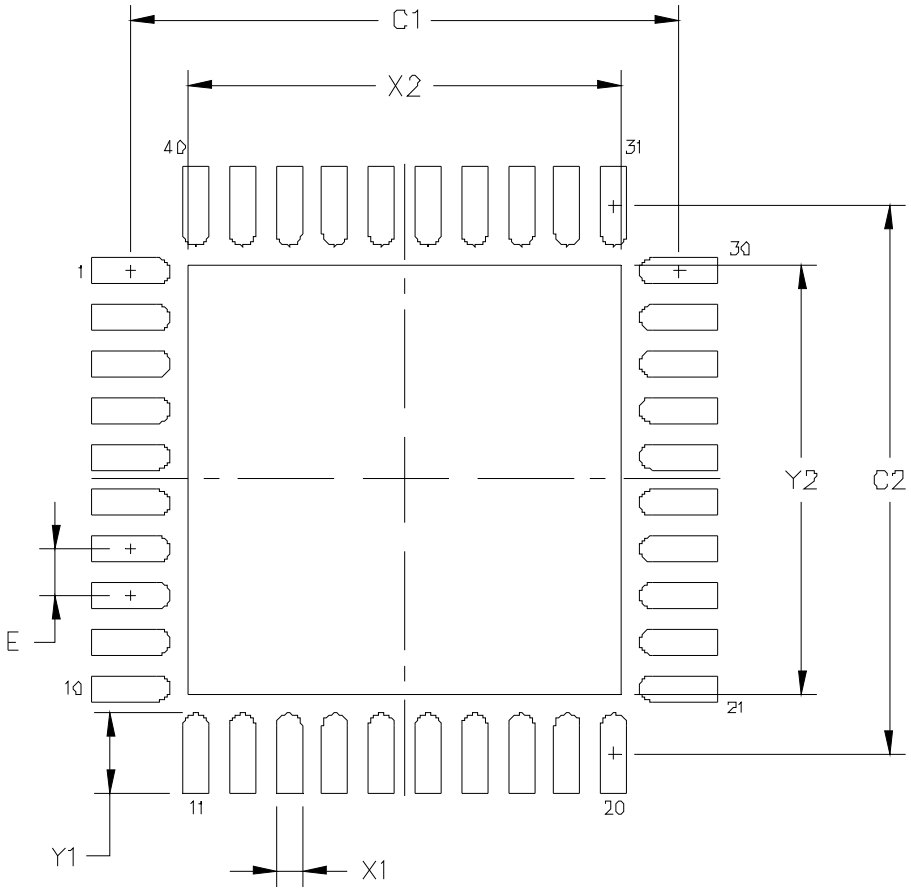

Figure 6.15. QFN-40 Landing Diagram

Table 6.13. QFN-40 Landing Diagram Dimensions

Dimension	mm
C1	5.90
C2	5.90
E	0.50
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Notes:
1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

6.8.1. QFN-40 Solder Mask Design

All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

6.8.2. QFN-40 Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 3x3 array of 1.1 mm square openings on a 1.6 mm pitch should be used for the center ground pad.

6.8.3. QFN-40 Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Revision Specific Behavior

This chapter details any known differences from behavior as stated in the device datasheet and reference manual. All known errata for the current silicon revision are rolled into this section at the time of publication. Any errata found after publication of this document will initially be detailed in a separate errata document until this datasheet is revised.

7.1. Revision Identification

The Lot ID Code on the top side of the device package can be used for decoding device revision information. Figures 7.1, 7.2, 7.3, and 7.4 show how to find the Lot ID Code on the top side of the device package.

In addition, firmware can determine the revision of the device by checking the DEVICEID registers.

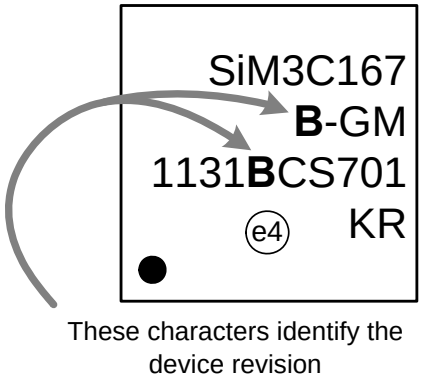

Figure 7.1. LGA-92 SiM3C1x7 Revision Information

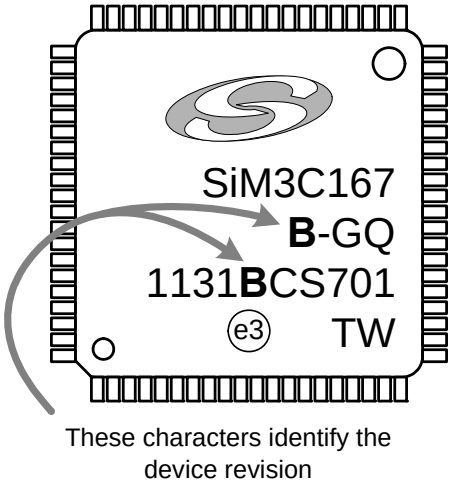

Figure 7.2. TQFP-80 SiM3C1x7 Revision Information

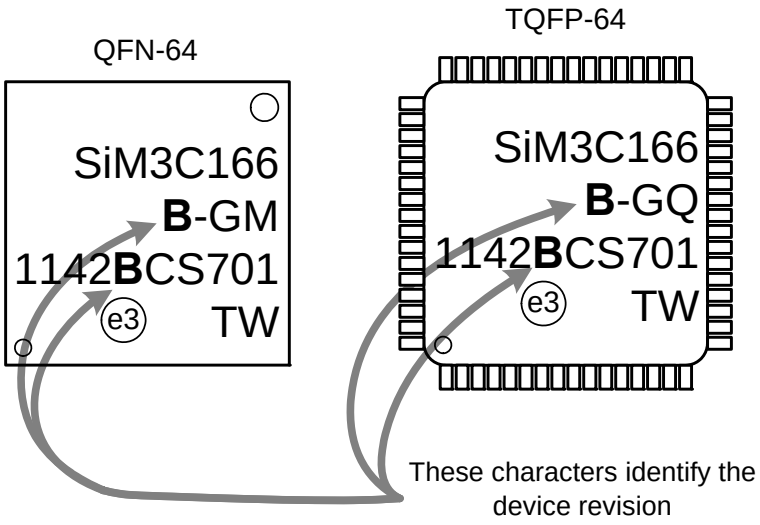

Figure 7.3. SiM3C1x6 Revision Information

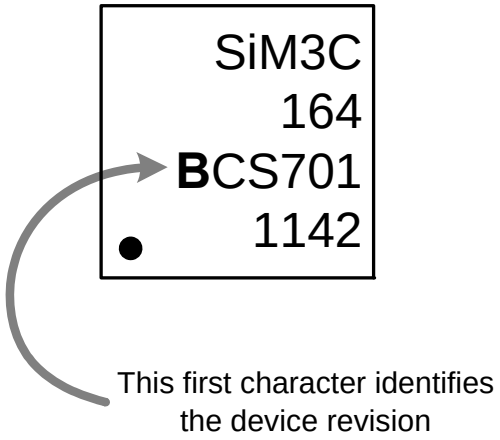

Figure 7.4. SiM3C1x4 Revision Information

7.2. Comparator Rising/Falling Edge Flags in Debug Mode (CMP0, CMP1)

7.2.1. Problem

On Revision A and Revision B devices, if the comparator output is high, the comparator rising and falling edge flags will both be set to 1 upon single-step or exit from debug mode.

7.2.2. Impacts

Firmware using the rising and falling edge flags to make decisions may see a false trigger of the comparator if the output of the comparator is high during a debug session. This does not impact the non-debug operation of the device.

7.2.3. Workaround

There is not a system-agnostic workaround for this issue.

7.2.4. Resolution

This issue exists on Revision A and Revision B devices. It may be corrected in a future device revision.

DOCUMENT CHANGE LIST

Revision 0.8 to Revision 1.0

- Added block diagram to front page; updated feature bullet lists.
- Electrical Specifications Tables Additions:
  - Voltage Regulator Current Sense Supply Current, Typ = 3 µA (Table 3.2)
  - Power Mode 2 Wake Time, Min = 4 clocks, Max = 5 clocks (Table 3.3)
  - External Crystal Clock Frequency, Min = 0.01 MHz, Max = 30 MHz (Table 3.9)
  - Added /RESET pin characteristics (Table 3.17)
- Electrical Specifications Tables Removals:
  - Power Mode 3 Wake Time (Table 3.3)
- Electrical Specifications Tables Corretions/Adjustments:
  - IVC Supply Current, Max = 2.5 µA (Table 3.2)
  - VREG0 Output Voltage Normal Mode, Min = 3.15 V (Table 3.5)
  - VREG0 Output Voltage Suspend Mode, Min = 3.15 V (Table 3.5)
  - External Regulator Internal Pull-Down, Typ = 5 kΩ (Table 3.6)
  - External Regulator Internal Pull-Up, Typ = 10 kΩ (Table 3.6)
  - Flash Memory Endurance, Typ = 100k write/erase cycles (Table 3.7)
  - Flash Memory Retention, Min = 10 Years, Typ = 100 Years (Table 3.7)
  - Low Power Oscillator Frequency, Min = 19.5 MHz, Max = 20.5 MHz (Table 3.8)
  - SAR Dynamic Performance : consolidated all specs. (Table 3.10)
  - IDAC Full Scale Output Current 1 mA Range, Min = 0.99 mA (Table 3.11)
  - IDAC Full Scale Output Current 0.5 mA Range, Min = 493 µA (Table 3.11)
  - IVC Slope @ 1 mA, Min = 1.55 V/mA, Max = 1.75 V/mA (Table 3.13)
  - IVC Slope @ 2 mA, Min = 795 mV/mA, Max = 860 mV/mA (Table 3.13)
  - IVC Slope @ 3 mA, Min = 525 mV/mA, Max = 570 mV/mA (Table 3.13)
  - IVC Slope @ 4 mA, Min = 390 mV/mA, Max = 430 mV/mA (Table 3.13)
  - IVC Slope @ 5 mA, Min = 315 mV/mA (Table 3.13)
  - IVC Slope @ 6 mA, Min = 260 mV/mA (Table 3.13)
  - Temperature Sensor Slope Error, Type = ±120 µV/C (Table 3.15)
  - Comparator Input Offset Voltage, Min = –10 mV, Max = 10 mV (Table 3.16)
- “4. Precision32™ SiM3C1xx System Overview” :
  - Updated Power Modes discussion.
  - Refined and updated feature bullet lists.
- Updated and clarified RTC timer clock output. The RTC output is now referred to as "RTC0TCLK".
- “6. Pin Definitions and Packaging Information” : Renamed RTC0OSC_OUT function to RTC0TCLK_OUT for consistency.
- “7. Revision Specific Behavior” : Updated revision identification drawings to better match physical appearance of packages.

Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701

Please visit the Silicon Labs Technical Support web page:
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and register to submit a technical support request.

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