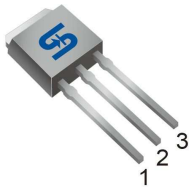
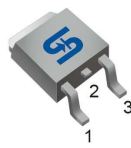




TO-251
(IPAK)



TO-252
(DPAK)



Pin Definition:

1. Gate
2. Drain
3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
500	2.7 @ $V_{GS}=10V$	3

General Description

The TSM4NB50 N-Channel enhancement mode Power MOSFET is produced by planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

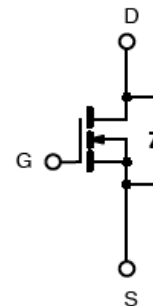
- Low gate charge typical @ 7.6nC
- Low Crss typical @ 18pF
- Fast Switching

Ordering Information

Part No.	Package	Packing
TSM4NB50CH C5G	TO-251	75pcs / Tube
TSM4NB50CP ROG	TO-252	2.5Kpcs / 13" Reel

Note: "G" denotes for Halogen Free

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating ($T_a=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current	I_D	3	A
Pulsed Drain Current	I_{DM}	12	A
Continuous Source Current (Diode Conduction)	I_S	3	A
Single Pulse Drain to Source Avalanche Energy (Note 3)	E_{AS}	110	mJ
Total Power Dissipation @ $T_c=25^\circ C$	P_{DTOT}	45	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R_{\theta JC}$	2.78	$^\circ C/W$
Thermal Resistance - Junction to Ambient	$R_{\theta JA}$	100	$^\circ C/W$

Notes: Surface mounted on FR4 board $t \leq 10sec$

Electrical Specifications ($T_a = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	500	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 1.5A$	$R_{DS(ON)}$	--	2.3	2.7	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.5	3.5	4.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Forward Transconductance	$V_{DS} = 10V, I_D = 1.5A$	g_{fs}	--	2	--	S
Dynamic^b						
Total Gate Charge	$V_{DS} = 300V, I_D = 3A,$ $V_{GS} = 10V$	Q_g	--	7.6	--	nC
Gate-Source Charge		Q_{gs}	--	1.8	--	
Gate-Drain Charge		Q_{gd}	--	3.8	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	C_{iss}	--	327	--	pF
Output Capacitance		C_{oss}	--	60	--	
Reverse Transfer Capacitance		C_{rss}	--	18	--	
Switching^c						
Turn-On Delay Time	$V_{GS} = 10V, I_D = 3A,$ $V_{DD} = 300V, R_G = 4.7\Omega$	$t_{d(on)}$	--	10	--	nS
Turn-On Rise Time		t_r	--	11	--	
Turn-Off Delay Time		$t_{d(off)}$	--	19	--	
Turn-Off Fall Time		t_f	--	14	--	
Source Drain Diode						
Source Drain Current		I_{SD}	--	--	3	A
Diode Forward Voltage	$I_S = 3A, V_{GS} = 0V$	V_{SD}	--	0.9	1.5	V

Note 1: Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

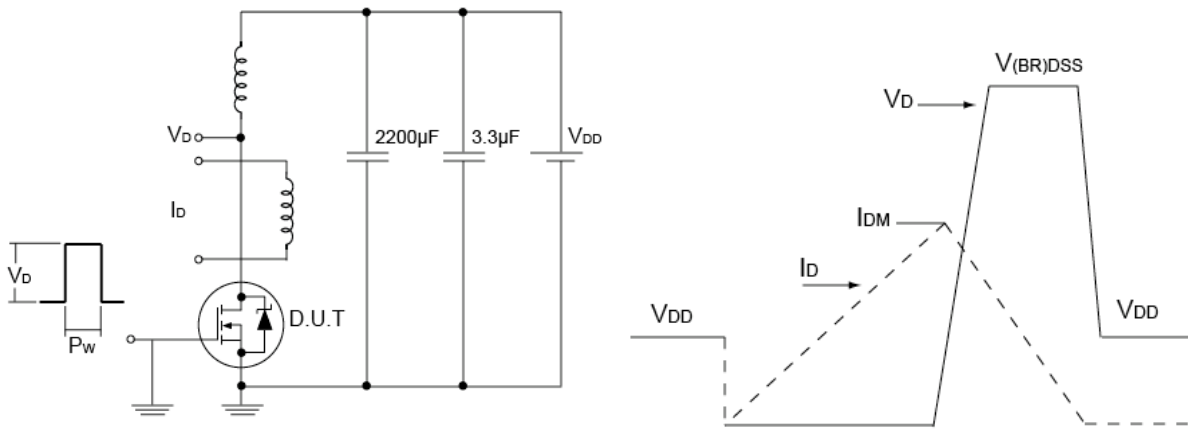
Note 2: $V_{DD} = 50V, I_{AS} = 2A, L = 50\text{mH}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$

Note 3: $I_{SD} \leq 3A, di/dt \leq 200A/\mu S, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

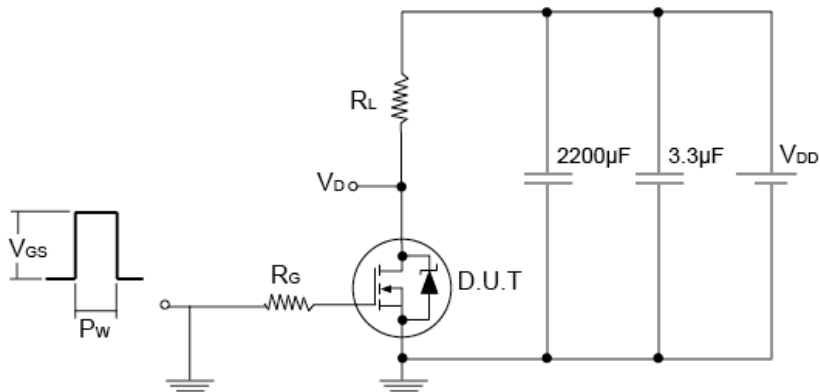
Note 4: Pulse test: pulse width $\leq 300\mu S$, duty cycle $\leq 2\%$

Note 5: Essentially Independent of Operating Temperature

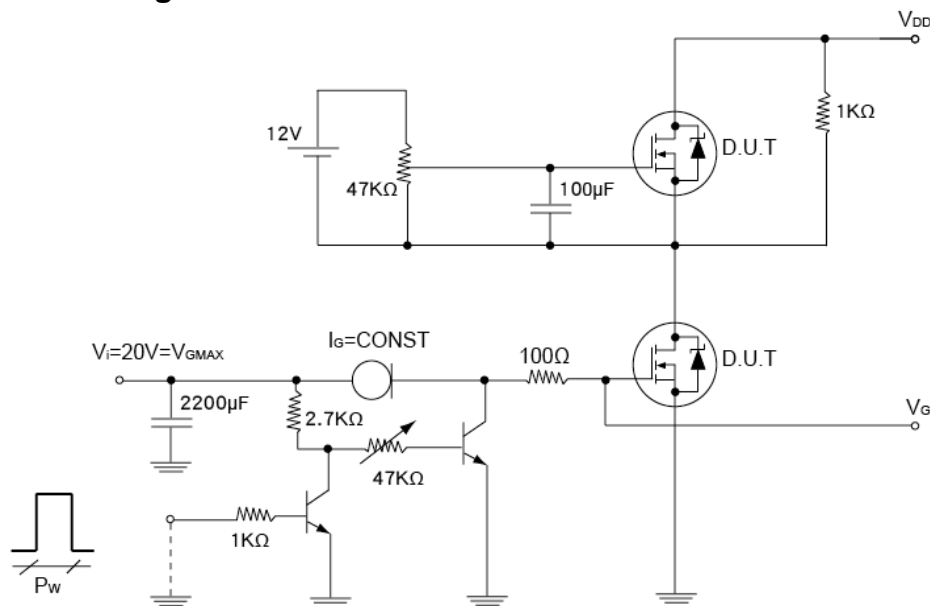
Unclamped Inductive Load Test Circuit and Waveform



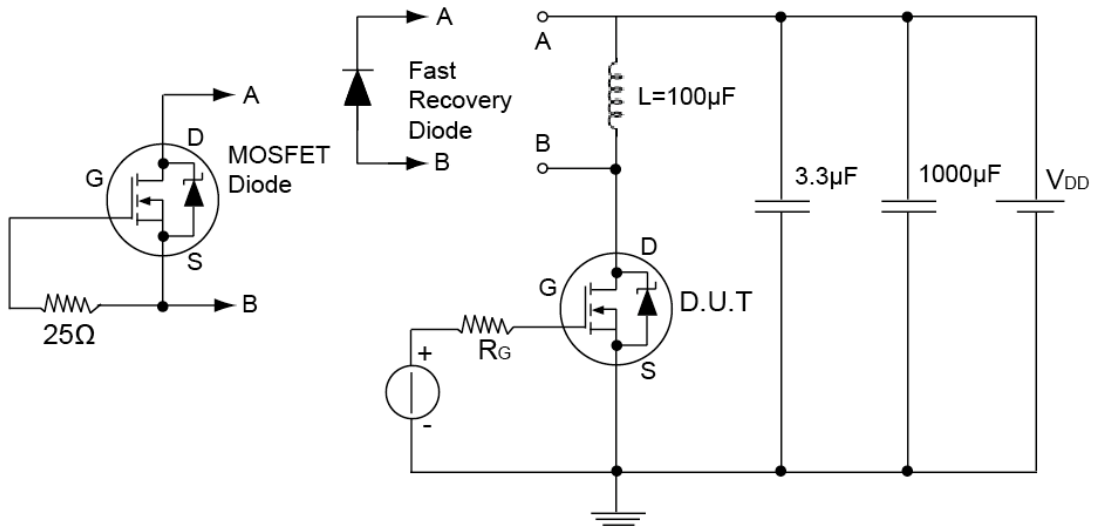
Switching Time Test Circuits for Resistive Load



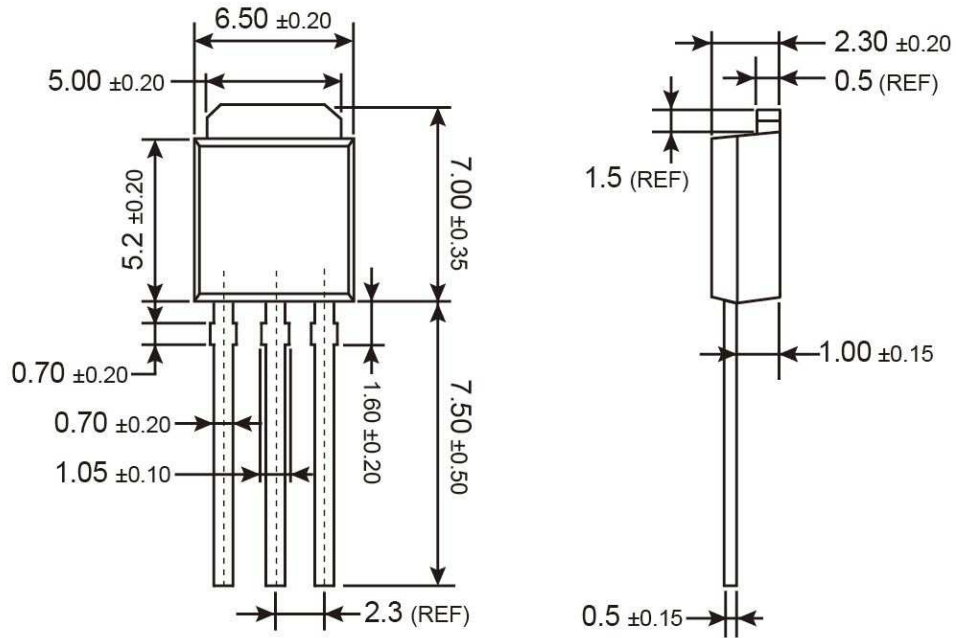
Gate Charge Test Circuit



Test Circuit for Inductive Load Switching and Diode Recovery Times

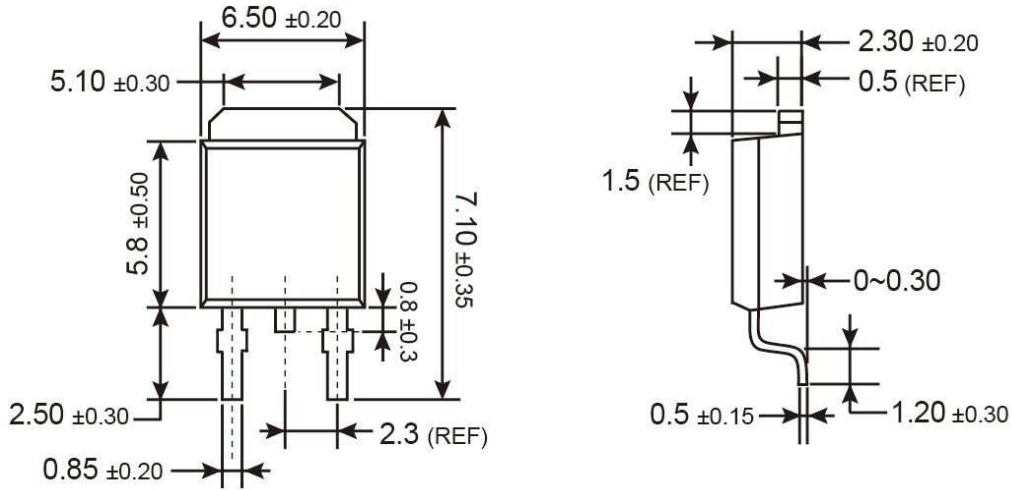


TO-251 Mechanical Drawing



Unit: Millimeters

TO-252 Mechanical Drawing



Unit: Millimeters

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