32-MBIT HIGH-TEMPERATURE FLASH MEMORY WITH SERIAL PERIPHERAL INTERFACE (SPI) BUS

Check for Samples: SM28VLT32-HT

FEATURES

- **32-Megabit Flash for High-Temperature Applications**
- **Serial Peripheral Interface (SPI) Compatible (Mode 0 and 3)**
- **3.3-V Supply for IO, 1.8 V for Core**
- **2-M x 16-Bit Word Access**
- **Asynchronous Read, Write, and Erase Operations**
- **12-MHz Maximum Clock Frequency**
- **Endurance: TBD Program and Erase Cycles**
- **Data Retention: 1000 hrs**
- **ESD Protection: 2-kV HBM, 500-V CDM**
- **8-mm x 20-mm 14-Pin Ceramic Package**

APPLICATIONS

- **Down-Hole Energy Drilling**
- **Test and Measurement Equipment**
- **Seismic Data Collection at Extreme Temperatures**
- **General Data Collection Applications at Extreme High- and Low-Temperatures**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C to 210°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION

SM28VLT32 is a 32-Megabit Flash Memory designed to store program code and/or data from acquisition. The wide temperature rating of this device makes it ideal for applications that need to perform reliably in harsh environments. SM28VLT32 with its serial peripheral interface (SPI) offers low pin count for additional reliability and easy assembly in these applications.

The memory is partitioned as sectors to provide addressing of 2-M words of 16 bits each. Thus, the memory address is 21 bits wide.

SM28VLT32 supports serial peripheral interface to read/write/erase data in the flash memory. The interface is compliant with mode 0 (CPOL = 0, CPHA = 0) and 3 (CPOL = 1, CPHA = 1). Asserting CS# enables the device to enter communication mode. With CS# de-asserted, the device ignores all activity on the SPI pins. As shown in Figure 1, multiple SM28VLT32 devices can be controlled from a single Master by independently controlling CS# pins in order to realize larger memory in the application. Asserting the HOLD# pin (while CS# is also asserted) will let the device ignore activity on the other SPI input pins (SCK and SI).

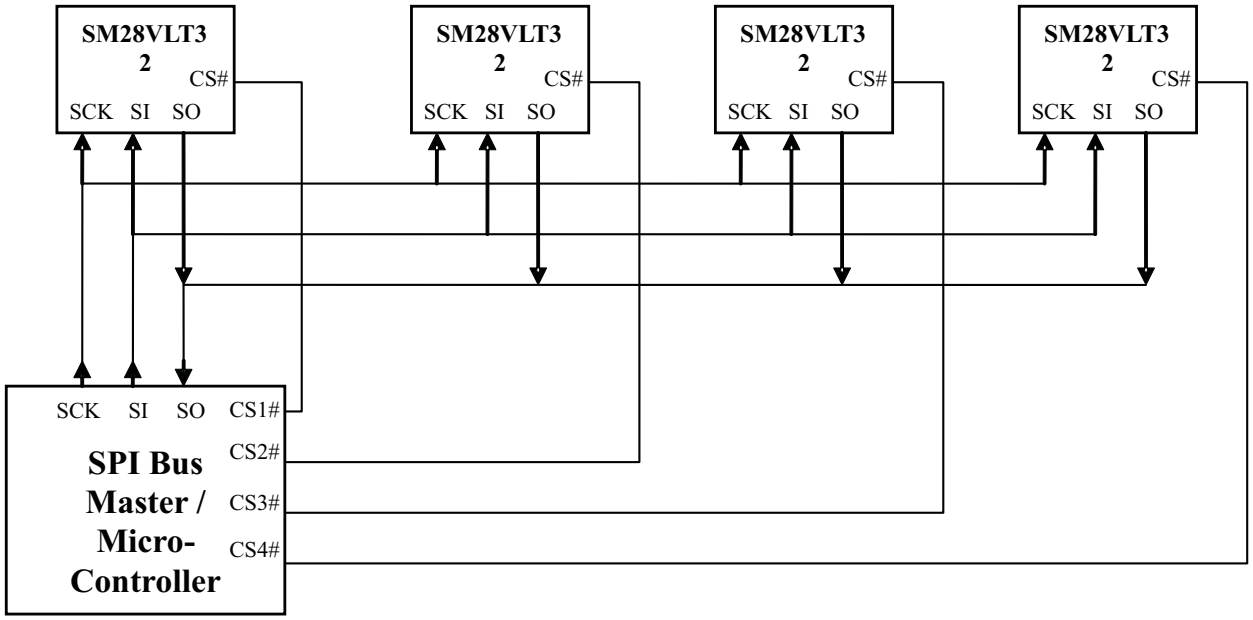


Figure 1. System Block Diagram That Shows Configuration to Use Multiple SM28VLT32 Devices to Realize Larger Memory

The SM28LVT32 supports a hardware data protection scheme using the WP# pin. Erase and program operations are inhibited if WP# is low.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_J	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	14HKN	SM28VLT32SHKN	28VLT32SHKN
	KGD (Bare Die)	SM28LVT32SKGD3	N/A

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
VDDS	Supply voltage range (for IO)	–0.3 V to 3.6 V
VDD	Supply voltage range (for Core)	–0.3 V to 1.98 V
V_I	Input voltage range	–0.2 V to (V_{IO} + 0.2)
V_O	Output voltage range	–0.2 V to (V_{IO} + 0.2)
ESD	Electrostatic discharge (HBM, 1.5 kΩ, 100 pF)	> 2000 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VDDS	Device supply voltage for IO	3	3.3	3.6	V
VDD	Device supply voltage for Core	1.626	1.8	1.98	V
T_J	Junction temperature	–55		210	°C

ELECTRICAL CHARACTERISTICS: IO

V_{IO} = 3 V to 3.6 V, V_{Core} = 1.62 V to 1.98 V, T_A = –55°C to 210°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		0.7VDDS			V
V_{IL}	Input low voltage				0.3VDDS	V
I_{OH}	Output high current		-1.0			mA
I_{OL}	Output low current				1.0	mA
V_{OH}	Output high voltage		0.8VDDS			V
V_{OL}	Output low voltage				0.2VDDS	V

ELECTRICAL CHARACTERISTICS: MEMORY

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Life}	Continuous operating life		1000			hrs
$I_{DDVCORE}$				120	TBD	mA
I_{DDVIO}				12	TBD	mA

ELECTRICAL CHARACTERISTICS: SPI

V_{IO} = 2.7 V to 3.3 V, V_{Core} = 1.62 V to 1.98 V, T_A = –55°C to 210°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK}	SPI input clock frequency(1)				10	MHz
f_{CLK}	Flash clock(1)				12	MHz
t_{WH}	Clock high time					ns
t_{WL}	Clock low time					ns
t_{SU}	Data setup time before SCK					ns
t_{HD}	Data hold time after SCK					ns
t_V	Clock low to data valid					ns

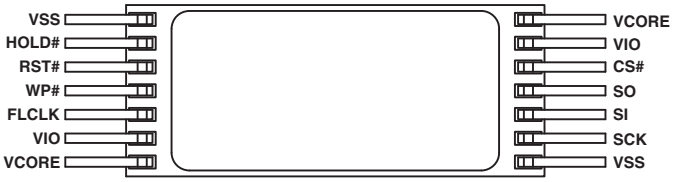
(1) The ratio of f_{CLK}/f_{SCK} must be 6/5 or higher to insure proper asynchronous operation. Operation below 10 MHz is acceptable, however, some configuration changes are required to set proper internal timing. Please contact factory for details if planned usage is below 10 MHz.

DISSIPATION RATINGS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Thermal resistance junction-to-ambient	0 LFM		TBD		°C/W
		150 LFM		TBD		
		250 LFM		TBD		
		500 LFM		TBD		
θ_{JP}	Thermal resistance junction-to-pad			TBD		°C/W

DEVICE INFORMATION

PIN ASSIGNMENT TOP VIEW



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
VIO	6, 13	Power	3.3-V supply for IO
VCORE	7, 14	Power	1.8-V supply for core
VSS	1, 8	Ground	Device ground
CS#	12	Input	Active low SPI chip select
SCK	9	Input	SPI clock for serial communication
SI	10	Input	SPI data input to device
SO	11	Output	SPI data output from device (Hi impedance when CS# is 1)
HOLD#	2	Input	Active low hold input to freeze SPI communication
WP#	4	Input	Active low input for sector protection
RST#	3	Input	Active low reset to IC
FLCLK	5	Input	Flash pump clock

FUNCTIONAL BLOCK DIAGRAM

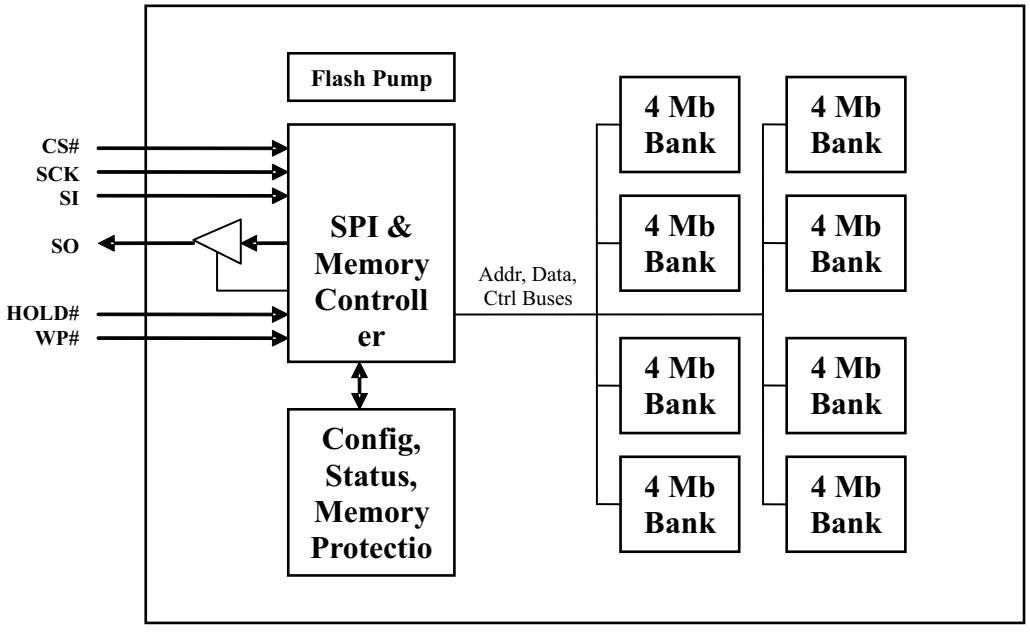


Figure 2. Block Diagram of SM28VLT32 and Memory Architecture

DETAILED DESCRIPTION

SERIAL COMMUNICATION

SM28VLT32 supports mode 0 and mode 3 SPI protocols. In mode 0, the inactive state of SCK is 0 whereas, in mode 3, the state is 1. The input data on SI is always latched on rising edge of SCK and data on SO is output on falling edge of SCK in both modes. CS# is brought low to start a new SPI data frame. The SPI data frame consists of an 8-bit command byte followed by a variable number of bytes of input data as shown in Table 1. The first 8 bits of SO always output the quick status bits. These bits define error conditions and status of the FLASH (see Table 2). These bits should be evaluated after each command is executed to determine if the preceding command completed successfully. This can be implemented as part of the SPI communication protocol with the host device. For more information see the Application Information section. The output data on SO follows after the complete data is provided to the device on SI pin. Invalid command bytes are ignored. Also, any additional SCK clock cycles and additional data on SI beyond the depicted frame size are ignored. CS# going high delineates the end of current data frame.

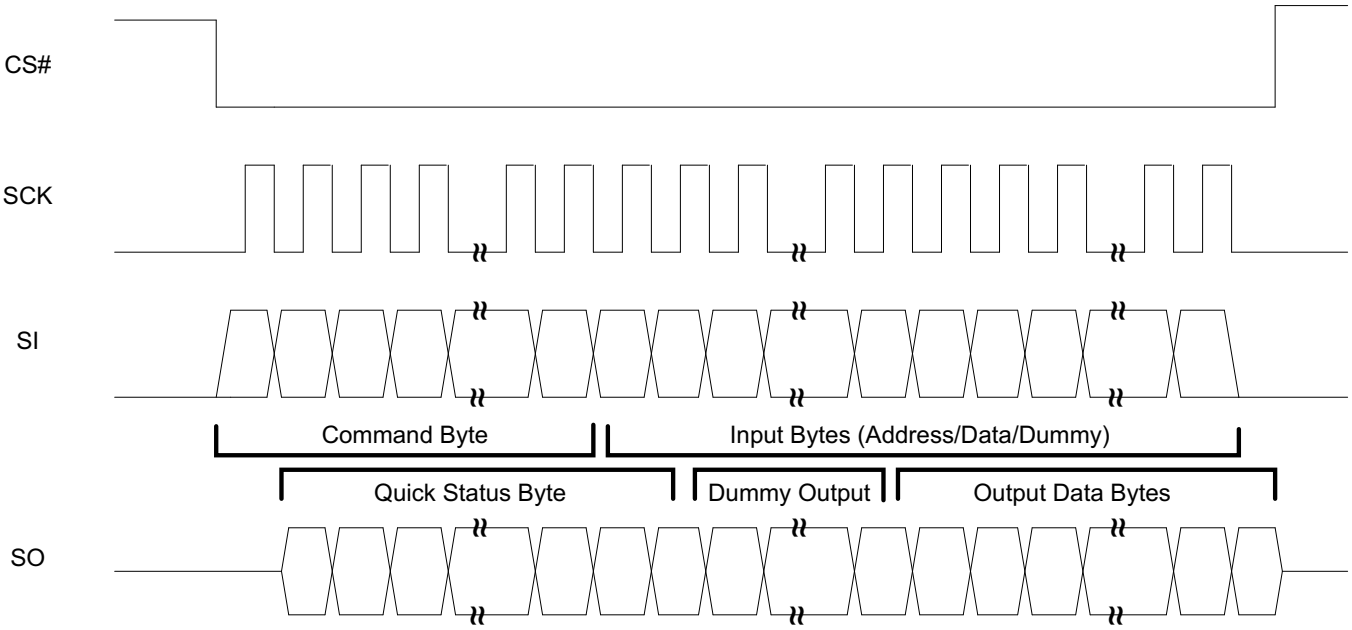


Figure 3. SPI Data Frame to Read, Write, Erase Memory Data and to Access Config/Status Registers

Table 1. Serial Peripheral Interface (SPI) Data Frame(1)

COMMAND NAME	COMMAND BYTE ON SI	ADDRESS BYTES ON SI	DATA BYTES ON SI	DUMMY BYTES ON SI(2)	DATA BYTES ON SO	TOTAL BYTES IN FRAME	DESCRIPTION
Read Word	15h	3	0	1 (3)	2	7	Read word at given address
Read Word with auto addressing	16h	0	0	1 (3)	2	4	Burst read from previous address
Write Word	17h	3	2	1 (1)	0	7	Write word at given address
Write Word with auto addressing	18h	0	2	1 (1)	0	4	Burst write from previous address
Erase segment	19h	3	0	1 (1)	0	5	Erase addressed segment
Read Status Register	22	0	0	0 (2)	2	3	Read SPI status register
Write Command	1F	0	2	1 (1)	0	4	Flash controller command interface for special functions. See Application Information section.

(1) Multi-byte inputs and results are MSB first, LSB last.
(2) (#) indicates total number of dummy SI bytes including overlap with SO output.

REGISTER DEFINITIONS

Table 2. Quick Status Register

BITS	DEFAULT VALUE	TYPE	DESCRIPTION
7	0	R	Unused
6	0	R	SPI Frame error: indicates frame ended with less than required bytes to complete
5	0	R	Write Busy: indicates that a program operation is in progress
4	0	R	Erase Busy: indicates that a sector is being erased
3	0	R	Device Busy
2	0	R	Invalid Data: indicates that an attempt was made to set a bit to 1 that has already been programmed to 0
1	0	R	Read error: indicates that read was attempted on address when data was not available
0	0	R	Command error: indicates that a prior command failed. Must be cleared.

Table 3. Status Register (Command 22h)

BITS	DEFAULT VALUE	TYPE	DESCRIPTION
15:12	0	R	Reserved
11:08	RevID	R	Revision ID (current revision 1001)
7	0	R	Unused
6	0	R	Read Busy
5	0	R	Write Busy
4	0	R	Erase Busy
3	0	R	Write Suspend
2	0	R	Erase Suspend
1	0	R	Flash Pump Ready
0	0	R	SPI Frame error

APPLICATION INFORMATION

The quick status register is intended to be used as feedback of device and command status. The host should evaluate the quick status results at each command execution to determine device status. Additionally, two of the error fields in the quick status are sticky. They will need to be intentionally cleared by the host once detected. The Command and Invalid Data error flags will not self clear. The command error bit indicates that a command failed. This can be either an erase or program command. If this was a program attempt, then the data written may not be valid. The host may decide to re-write this data or pursue some other error recovery path. The Invalid data bit will get set if an attempt to write a bit to a logical 1 (erased state) in a word that has that bit already programmed to a 0. This would likely be the first error seen when writing to an array that contains data. To clear a Command error or Invalid Data error, the host must execute the following SPI command sequence: 1F 00 40 xx. xx is a dummy byte and values are don't care. This SPI command is a special command that is sent to the internal flash controller to clear errors.

It is important to note that the quick status capture of the internal setting of the Command error and the Invalid Data flags are delayed by one transaction. Similarly, the Device Busy flag does not get cleared until a second transaction. For example, in the case of polling after a write. If this write generated an Invalid Data error, the sequence would be as follows.

SPI WRITE	SPI READ	DESCRIPTION
0x17_0000_FFFF	00_xxxx_xxxx	Write to address 0 with erased value This will cause Invalid Data error if word has been programmed.
0xFF	08	Execute quick status. This result is Device Busy.
0xFF	04	Execute quick status with Invalid Data error.

Similarly, if a write or program fails, then the Command error status will show on the second transaction after the failed command. To effectively deal with this in a protocol, the best method is to poll the quick status twice to validate no error occurred. For applications that this method is too costly for SPI bandwidth, the error can be trapped on execution of the following commands with the knowledge that the error belonged to the command 2 transactions earlier.

The SPI Frame error and the Read error are errors that return correct status on the next quick status. These two errors are not sticky and only apply to the prior transaction.

Power Supply Sequencing

The ideal power supply sequence is VCORE coming up before VIO (VCORE > 1.65 V before V_{CCIO} greater than 0.8 V).

For powerdown, the reverse is also true. VIO should be below 0.8 V before VCORE is < 1.65 V.

Alternatively, VIO can come up first or simultaneously with VCORE if RST is asserted low until both supplies are within recommended operating range. Similarly if device is active, it is necessary to assert RST prior to powering down to minimize chance of corrupting the flash array.

Power Saving Features

The device has power saving capabilities that allow it to be put into either standby or sleep states for the banks and flash pump when periods of inactivity are detected. When an access is initiated during sleep or standby, the pump and banks will transition to the active state automatically. Use of these features does not have protocol impact on programming (other than additional time required to wake up), as the device will report Write Busy. However, during read operations, the device will report Read error on next quick status read. This is due to the fact that a read transaction is immediate, while a write is queued. The value read from an address that is in standby or sleep will be 00 00. An application note discussing usage of power saving features will be available.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SM28VLT32SHKN	PREVIEW	CFP	HKN	14	1	TBD	Call TI	Call TI	
SM28VLT32SKGD3	PREVIEW	XCEPT	KGD	0	36	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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