ACPL-077L

Low Power 3.3 V / 5 V High Speed CMOS Optocoupler Design for System Level Reliability

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

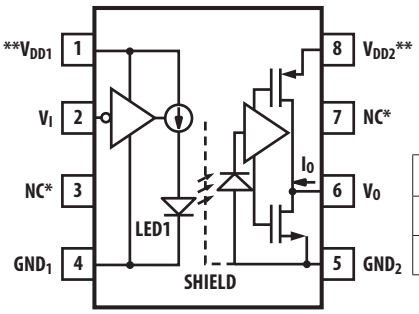
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

Avago's ACPL-077L optocoupler utilizes the latest CMOS IC technology to achieve outstanding speed and low power performance of minimum 25 MBd data rate and 6 ns maximum pulse width distortion with enhanced reliability relative to system level IEC 61000-4-X testing (ESD/Burst/Surge).

Available in SO-8 package, the basic building blocks of ACPL-077L are a CMOS LED driver IC, a high speed LED and a CMOS detector IC. A CMOS logic input signal controls the LED driver IC, which supplies current to the LED. The detector IC incorporates an integrated photodiode, a high speed transimpedance amplifier, and a voltage comparator with an output driver.

Functional Diagram



ACPL-077L

TRUTH TABLE (POSITIVE LOGIC)

V_I	LED	V_O
HIGH	OFF	HIGH
LOW	ON	LOW

* Pin 3 is multiplexed as a test pin that can connect to V_{DD} or left unconnected. Pin 7 is not connected internally.

** A 0.1 µF bypass capacitor must be connected between pins V_{DD1} and GND_1, and V_{DD2} and GND_2

Features

- Enhance reliability relative to system level IEC 61000-4-X testing (ESD/Burst/Surge)
- 3.3 V and 5 V CMOS Compatibility
- CMOS buffer input
- Allow level shifting functionality
- High Speed: DC to 25 MBd
- 35 kV/µs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V
- Guaranteed AC and DC performance over wide temperature: -40° C to +105° C
- Safety and Regulatory Approvals:

  UL Recognised

  – 3750 V_{rms} for 1 min. per UL1577

  CSA Component Acceptance Notice #5
  IEC/EN/DIN EN 60747-5-5

  – V_{IORM} = 567 V_{peak} for Option 060E
- Lead-free option available

Applications

- Digital Fieldbus Isolation: CC-Link, DeviceNet, Profibus, SDS
- Multiplexed Data Transmission
- General Instrument and Data Acquisition
- Computer Peripheral Interface
- Microprocessor System Interface

Ordering Information

The ACPL-064L and ACPL-M61L are UL Recognized with an isolation voltage of 3750 V_{rms} for 1 minute per UL1577. The ACPL-W61L and ACPL-K64L are UL Recognized with an isolation voltage of 5000 V_{rms} for 1 minute per UL1577. All devices are RoHS compliant.

Part number	Option RoHS Compliant	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACPL-077L	-000E	SO-8	X			100 per tube
	-060E		X		X	100 per tube
	-500E		X	X		1500 per reel
	-560E		X	X	X	1500 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-077L-500E to order product of Mini-flat Surface Mount 8-pin package in Tape and Reel packaging with RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Regulatory Information

The ACPL-077L will be approved by the following organizations:

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 3750 V_{RMS}.

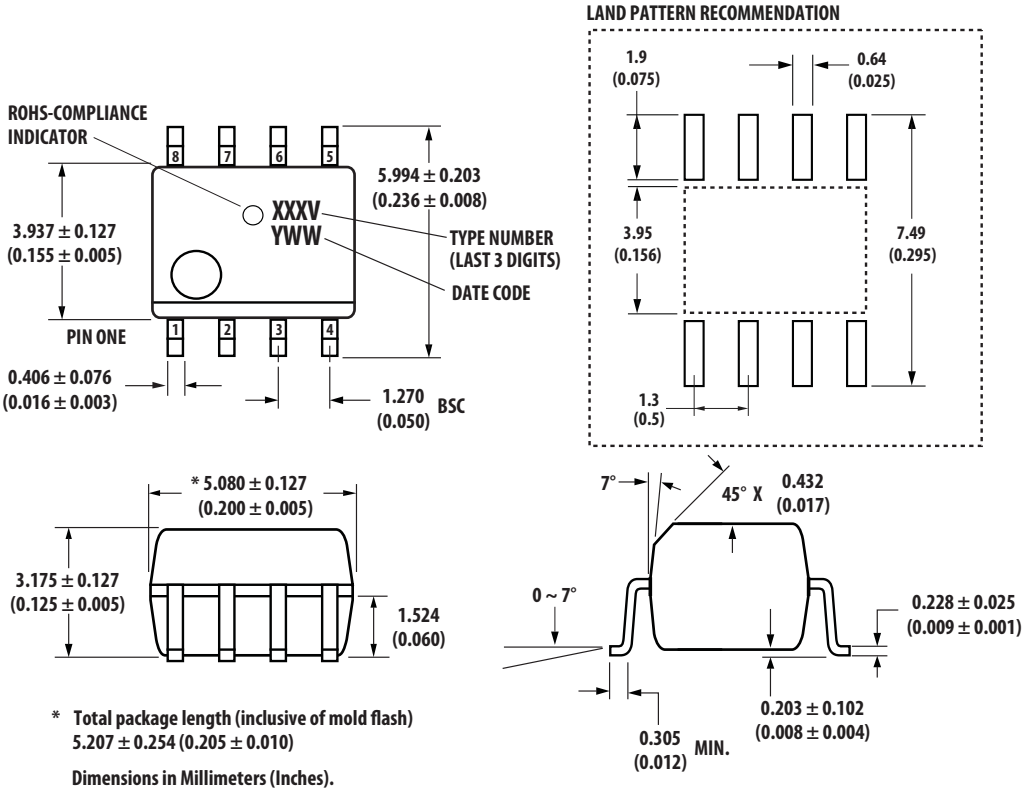
CSA

Approval under CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-5 (Option 060E only)

Package Outline Drawings

ACPL-077L SO-8 Package



* Total package length (inclusive of mold flash) 5.207 ± 0.254 (0.205 ± 0.010)

Dimensions in Millimeters (Inches).

Note: Floating lead protrusion is 0.15 mm (6 mils) max.

Lead coplanarity = 0.10 mm (0.004 inches) max.

Option number 500 not marked.

Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-077L	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	4.8	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option 060E)

		Characteristic	
Description	**Symbol**	**ACPL-077L**	**Unit**
Installation classification per DIN VDE 0110/39, Table 1			
for rated mains voltage ≤ 150 V_{rms}		I – IV	
for rated mains voltage ≤ 300 V_{rms}		I – III	
for rated mains voltage ≤ 600 V_{rms}		I – II	
Climatic Classification		55/105/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m = 10 sec, Partial discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure.			
Case Temperature	T_S	150	°C
Input Current**	$I_{S, INPUT}$	150	mA
Output Power**	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Storage Temperature	T_S	-55	125	°C
Operating Temperature	T_A	-40	105	°C
Supply Voltage	V_{DD1}, V_{DD2}	0	6.5	V
Input Voltage	V_I	-0.5	V_{DD1} +0.5	V
Output Voltage	V_O	-0.5	V_{DD2} +0.5	V
Average Output Current	I_O		10	mA
Lead Solder Temperature	T_{LS}	260° C for 10 sec., 1.6 mm below seating plane		
Solder Reflow Temperature Profile		See Package Outline Drawings section		

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	T_A	-40	105	°C
Supply Voltage (3.3V)	V_{DD1}, V_{DD2}	3.0	3.6	V
Supply Voltage (5V)	V_{DD1}, V_{DD2}	4.5	5.5	V
Logic High Input Voltage	V_{IH}	0.7 x V_{DD1}	V_{DD1}	V
Logic Low Input Voltage	V_{IL}	0	0.3 x V_{DD1}	V
Input Signal Rise and Fall Times	t_r, t_f		1	ms

Electrical Specifications (DC)

Over recommended temperature (T_A = –40° C to 105° C) and supply voltage (4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V), (3 V ≤ V_{DD1} ≤ 3.6 V, 3 V ≤ V_{DD2} ≤ 3.6 V), (4.5 V ≤ V_{DD1} ≤ 5.5 V, 3 V ≤ V_{DD2} ≤ 3.6 V) and (3 V ≤ V_{DD1} ≤3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V). All typical specifications are at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25° C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Logic Low Input Supply Current [2]	I_{DD1L}		5.5	8	mA	V_I = 0 V. Figure 1
Logic High Input Supply Current [2]	I_{DD1H}		0.6	2	mA	V_I = V_{DD1}. Figure 2
Logic Low Output Supply Current	I_{DD2L}		1.5	2.5	mA	V_I = 0 V. Figure 3
Logic High Output Supply Current	I_{DD2H}		1.5	2.5	mA	V_I = V_{DD1}. Figure 4
Input Current	I_I	-10		10	µA	
Logic High Output Voltage	V_{OH}	2.9	3.3		V	I_O = -20 µA, V_I = V_{IH}
		1.9	2.9		V	I_O = -4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.35	1.0	V	I_O = 4 mA, V_I = V_{IL}

Switching Specifications (AC)

Over recommended temperature (T_A = -40° C to 105° C) and supply voltage (4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V), (3 V ≤ V_{DD1} ≤ 3.6 V, 3 V ≤ V_{DD2} ≤ 3.6 V), (4.5 V ≤ V_{DD1} ≤ 5.5 V, 3 V ≤ V_{DD2} ≤ 3.6 V) and (3 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V). All typical specifications are at V_{DD1} = V_{DD2} = +3.3 V, T_A = 25° C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Propagation Delay Time to Logic Low Output [3]	t_{PHL}		24	40	ns	C_L = 15 pF, CMOS Signal Levels Figure 5 ,6
Propagation Delay Time to Logic High Output [3]	t_{PLH}		23	40	ns	C_L = 15 pF, CMOS Signal Levels Figure 5 ,6
Pulse Width	t_{PW}	40			ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate				25	MBd	C_L = 15 pF, CMOS Signal Levels
Pulse Width Distortion [4] $\lvert t_{PHL} - t_{PLH} \rvert$	PWD		1	6	ns	C_L = 15 pF, CMOS Signal Levels Figure 7, 8
Propagation Delay Skew [5]	t_{PSK}			15	ns	C_L = 15 pF, CMOS Signal Levels
Output Rise Time (10% – 90%)	t_R		4		ns	C_L = 15 pF, CMOS Signal Levels Figure 9
Output Fall Time (90% – 10%)	t_F		3		ns	
Common Mode Transient Immunity at Logic High Output [6]	$\lvert CM_H \rvert$	35	50		kV/µs	V_{CM} = 1000 V, T_A = 25° C, V_I = V_{DD1}, V_O > 0.8 x V_{DD2}
Common Mode Transient Immunity at Logic Low Output [6]	$\lvert CM_L \rvert$	35	50		kV/µs	V_{CM} = 1000 V, T_A = 25° C, V_I = 0 V, V_O < 0.8 V

Package Characteristics

All typical at T_A = 25° C

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input-Output Insulation [7,8,9]	V_{ISO}	3750			V_{rms}	RH < 50% for 1 min. T_A = 25° C
Input-Output Resistance [7]	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V
Input-Output Capacitance	C_{I-O}		0.6		pF	f=1 MHz, T_A = 25° C
Input Capacitance [10]	C_I		3.0		pF	

Notes:

1. Absolute maximum ambient operating temperature means the device will not be damaged if operated under these conditions. It does not guarantee functionality.
2. The LED is ON when V_I is low and OFF when V_I is high.
3. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.
4. PWD is defined as $|t_{PHL} - t_{PLH}|$. % PWD (percent pulse width distortion) is equal to the PWD divided by pulse width.
5. t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
6. CMH is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CML is the maximum common mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.
7. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
8. In accordance with UL1577, each ACPL-077L is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5\ \mu A$).
9. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to your equipment level safety specification or Avago Technologies Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
10. C_I is the capacitance measured at pin 2 (V_I).

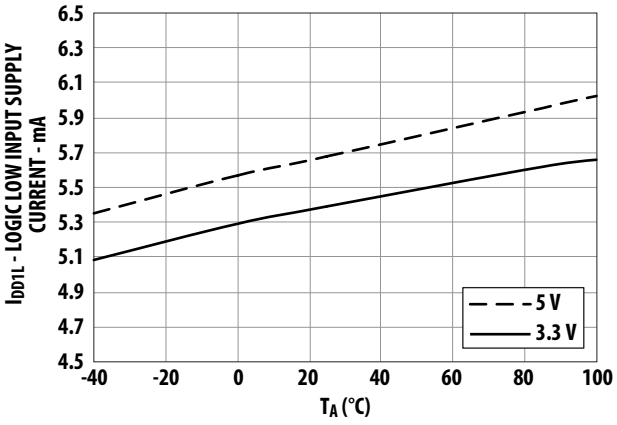


Figure 1. Typical Logic Low Input Supply Current versus temperature.

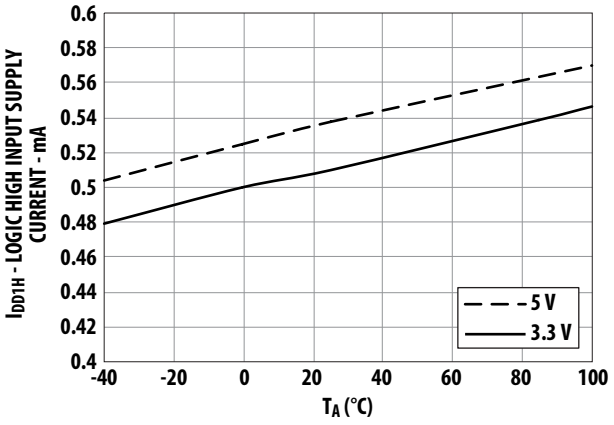


Figure 2. Typical Logic High Input Supply Current versus temperature.

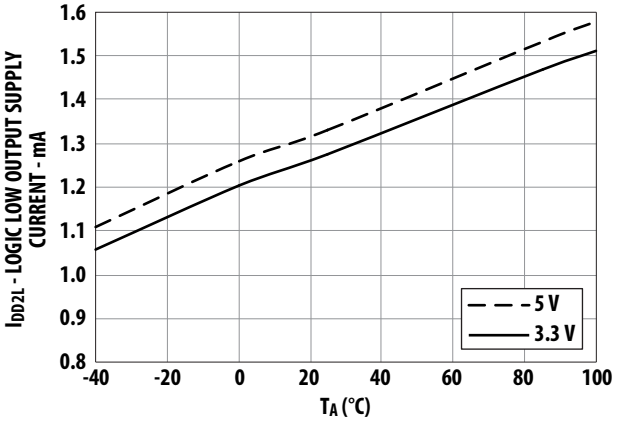


Figure 3. Typical Logic Low Output Supply Current versus temperature.

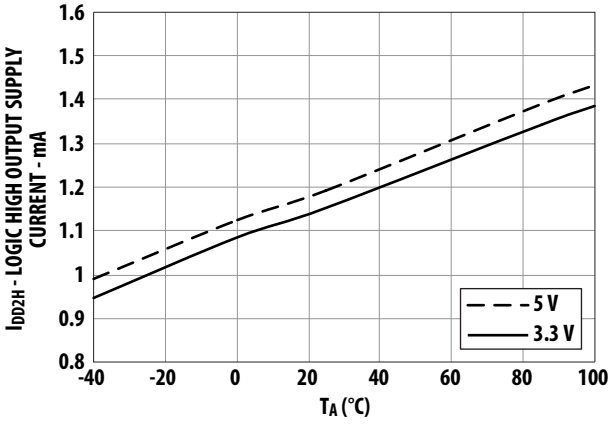


Figure 4. Typical Logic High Output Supply Current versus temperature.

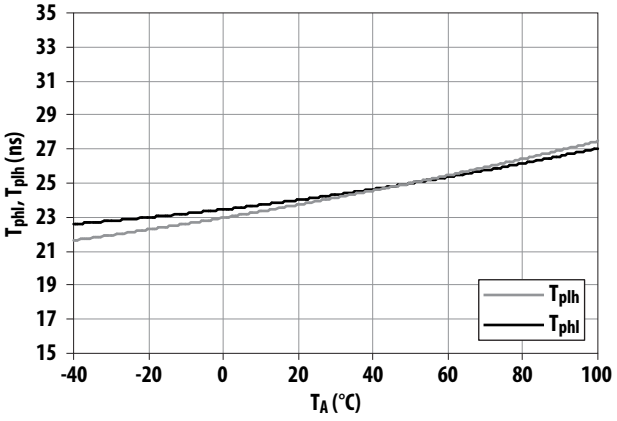


Figure 5. Typical propagation delay versus temperature at 3.3 V supply voltage.

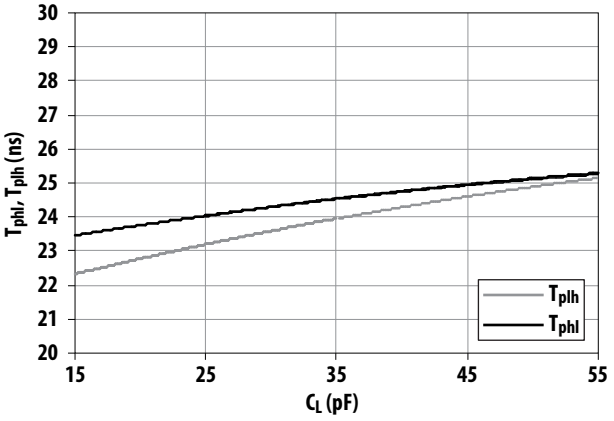


Figure 6. Typical propagation delays vs load capacitance at 3.3 V supply voltage.

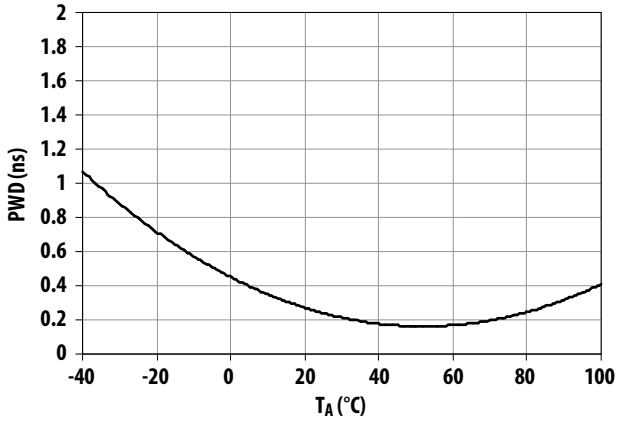


Figure 7. Typical pulse width distortion vs temperature at 3.3 V supply voltage.

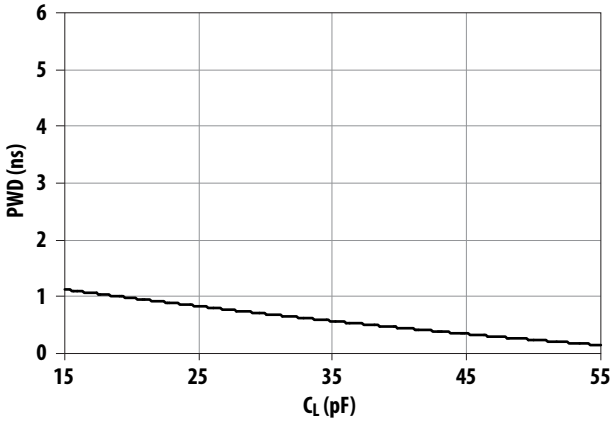


Figure 8. Typical pulse width distortion vs load capacitance at 3.3 V supply voltage.

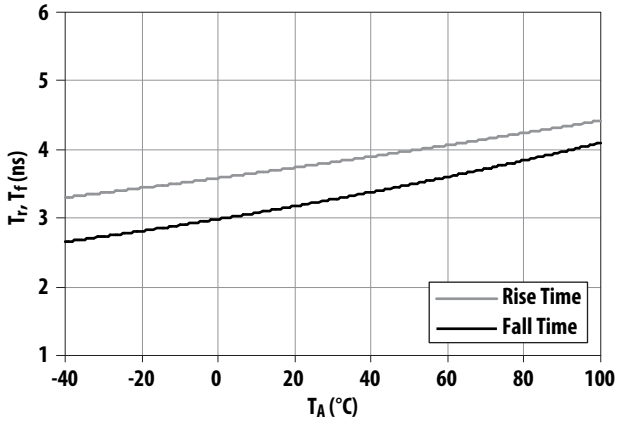


Figure 9. Typical rise and fall time versus temperature at 3.3 V supply voltage.

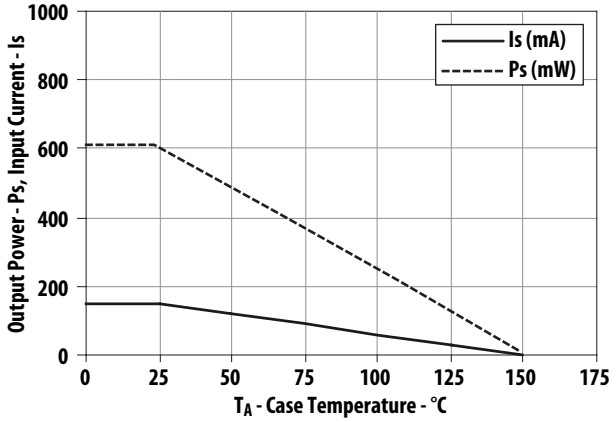


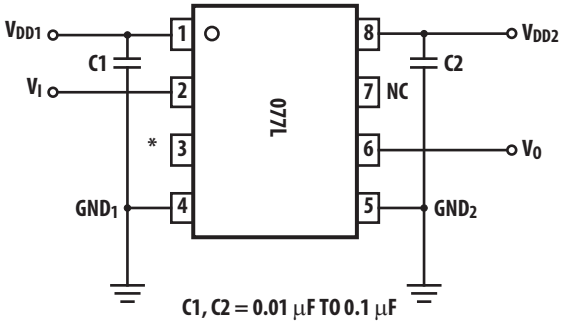
Figure 10. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-5

Application Information

Bypassing and PC Board Layout

The ACPL-077L optocoupler is extremely easy to use. No external interface circuitry is required because ACPL-077L uses high speed CMOS IC technology allowing CMOS logic to be connected directly to the inputs and outputs.

As shown in Figure 11, the only external components required for proper operation are two bypass capacitors. Capacitor values should be between 0.01 μF and 0.1 μF. For each capacitor, the total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm.



* Pin 3 is multiplexed as a test pin that can connect to V_{DD} or left unconnected. Pin 7 is not connected internally.

Figure 11. Recommended Circuit Diagram

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

The propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from a low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output, causing the output to change from high to low (Figure 12).

Pulse-width distortion (PWD) is the difference between t_{PHL} and t_{PLH} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable.

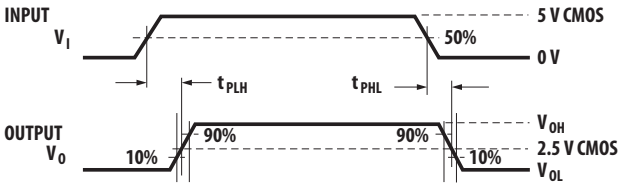


Figure 12. Signal plot shows how propagation delay is defined

Propagation delay skew, t_{PSK}, is an important parameter to consider in parallel data applications where synchronization of signals on parallel data lines is a concern. If the parallel data is sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delay is large enough it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays, either t_{PLH} or t_{PHL} for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 13, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay, either t_{PLH} or t_{PHL} and the longest propagation delay, either t_{PLH} and t_{PHL}.

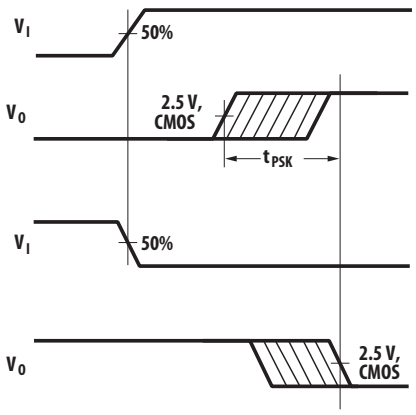


Figure 13. Propagation delay skew waveform

As mentioned earlier, t_{PSK} can determine the maximum parallel data transmission rate. Figure 14 is the timing diagram of a typical parallel data application with both the clock and data lines being sent through the optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. In this case the data is assumes to be clocked off of the rising edge of the clock.

Propagation delay skew represents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 14 shows that there will be uncertainty in both the data and clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all the data outputs have settled, or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

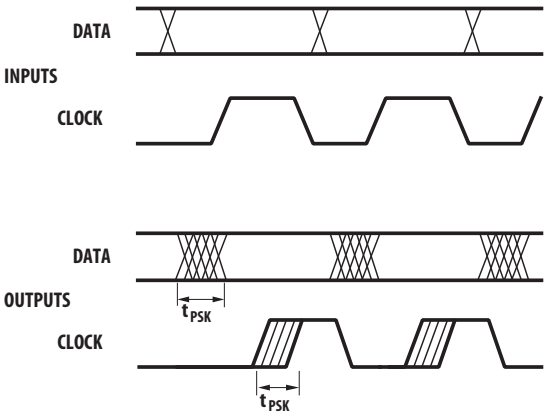


Figure 14. Parallel data transmission example

AV02-3547EN - May 24, 2012