1.2A High Efficient Step Down Converter in 2x2mm SON Package

Check for Samples: TLV62080

FEATURES

- **DCS-Control™ Architecture for Fast Transient Regulation**
- **2.5V to 5.5V Input Voltage Range**
- **100% Duty Cycle for Lowest Dropout**
- **Power Save Mode for Light Load Efficiency**
- **Output Discharge Function**
- **Power Good Output**
- **Thermal Shutdown**
- **Available in 2x2mm 8-Pin SON Package**
- **For Improved Features Set, See TPS62080**

APPLICATIONS

- **Battery Powered Portable Devices**
- **Point of Load Regulators**
- **System Power Rail Voltage Conversion**

DESCRIPTION

The TLV62080 device is a synchronous step down converter with an input voltage range of 2.5V to 5.5V. The TLV62080 focuses on high efficient step down conversion over a wide output current range. At medium to heavy loads, the converter operates in PWM mode and automatically enters Power Save Mode operation at light load currents to maintain high efficiency over the entire load current range.

To address the requirements of system power rails, the internal compensation circuit allows a large selection of external output capacitor values ranging from 10µF up to 100uF effective capacitance. With its DCS-Control™ architecture excellent load transient performance and output voltage regulation accuracy is achieved. The device is available in 2mm x 2mm SON package with Thermal PAD.

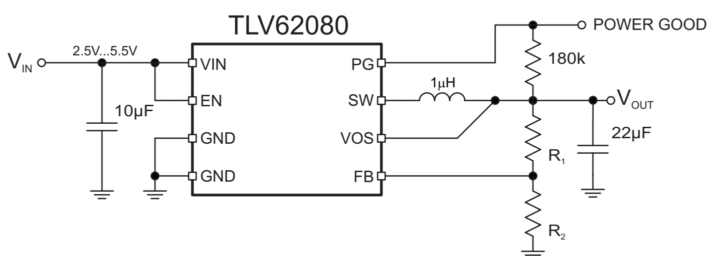


Figure 1. Typical Application of TLV62080

Table 1. ORDERING INFORMATION

T_A	PACKAGE MARKING	PACKAGE	PART NUMBER(1)
–40°C to 85°C	RAU	8-Pin SON	TLV62080DSG

(1) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE	UNIT
Voltage range at VIN, PG, VOS(2)	–0.3 to 7	V
Voltage range at SW(2)(3)	–0.3 to (V_{IN} + 0.3V)	V
Voltage range at FB(2)	–0.3 to 3.6	V
Voltage range at EN(2)	–0.3 to (V_{IN} + 0.3V)	V
ESD rating, Human Body Model	2	kV
ESD rating, Charged Device Model	500	V
Continuous total power dissipation	See Dissipation Rating Table	
Operating junction temperature range, T_J	–40 to 150	°C
Operating ambient temperature range, T_A	–40 to 85	°C
Storage temperature range, T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) During operation, device switching

THERMAL INFORMATION

THERMAL METRIC(1)		TLV62080	UNITS
		DSG (8 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	65.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	100.7	
θ_{JB}	Junction-to-board thermal resistance	135.7	
ψ_{JT}	Junction-to-top characterization parameter	2.3	
ψ_{JB}	Junction-to-board characterization parameter	45.1	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	8.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.5		5.5	V
V_{OUT}	Output voltage range	0.5		4.0	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

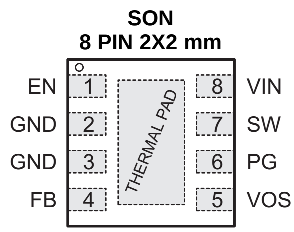
(1) Refer to the APPLICATION INFORMATION section for further information.

ELECTRICAL CHARACTERISTICS

Over recommended free-air temperature range, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted), V_{IN}=3.6V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V
I_Q	Quiescent current into VIN	I_{OUT} = 0mA, Device not switching		30		uA
I_{SD}	Shutdown current into VIN	EN = LOW			1	µA
V_{UVLO}	Under voltage lock out	Input voltage falling		1.8	2.0	V
	Under voltage lock out hysteresis	Rising above V_{UVLO}		120		mV
T_{JSD}	Thermal shut down	Temperature rising		150		°C
	Thermal shutdown hysteresis	Temperature falling below T_{JSD}		20		°C
LOGIC INTERFACE (EN)						
V_{IH}	High level input voltage	2.5V ≤ V_{IN} ≤ 5.5V	1			V
V_{IL}	Low level input voltage	2.5V ≤ V_{IN} ≤ 5.5V			0.4	V
I_{LKG}	Input leakage current			0.01	0.5	µA
POWER GOOD						
V_{PG}	Power good threshold	V_{OUT} falling referenced to V_{OUT} nominal	–15	–10	–5	%
	Power good hysteresis			5		%
V_{IL}	Low level voltage	I_{sink} = 500 µA			0.3	V
$I_{PG,LKG}$	PG Leakage current	V_{PG} = 5.0 V		0.01	0.1	µA
OUTPUT						
V_{OUT}	Output voltage range TLV62080		0.5		4.0	V
V_{FB}	Feedback regulation voltage	V_{IN} ≥ 2.5V and V_{IN} ≥ V_{OUT} + 1V	0.438	0.45	0.462	V
I_{FB}	Feedback input bias current	V_{FB} = 0.45 V		10	100	nA
R_{DIS}	Output discharge resistor	EN = LOW, V_{OUT} = 1.8 V		1		kΩ
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		120		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		90		mΩ
I_{LIM}	High side FET switch current limit	Rising inductor current	1.6	2.8	4	A

DEVICE INFORMATION



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	8	PWR	Power Supply Voltage Input.
EN	1	IN	Device Enable Logic Input. Logic HIGH enables the device, logic LOW disables the device and turns it into shutdown.
GND	2,3	PWR	Power and Signal Ground.
VOS	5	IN	Output Voltage Sense Pin for the internal control loop. Must be connected to output.
SW	7	PWR	Switch Pin connected to the internal MOSFET switches and inductor terminal. Connect the inductor of the output filter here.
FB	4	IN	Feedback Pin for the internal control loop. Connect this pin to the external feedback divider to program the output voltage.
PG	6	OUT	Power Good open drain output. This pin is pulled to low if the output voltage is below regulation limits. Can be left floating if not used.
Thermal Pad			Must be connected to GND. Must be soldered to achieve appropriate power dissipation and mechanical Thermal Pad reliability.

FUNCTIONAL BLOCK DIAGRAMS

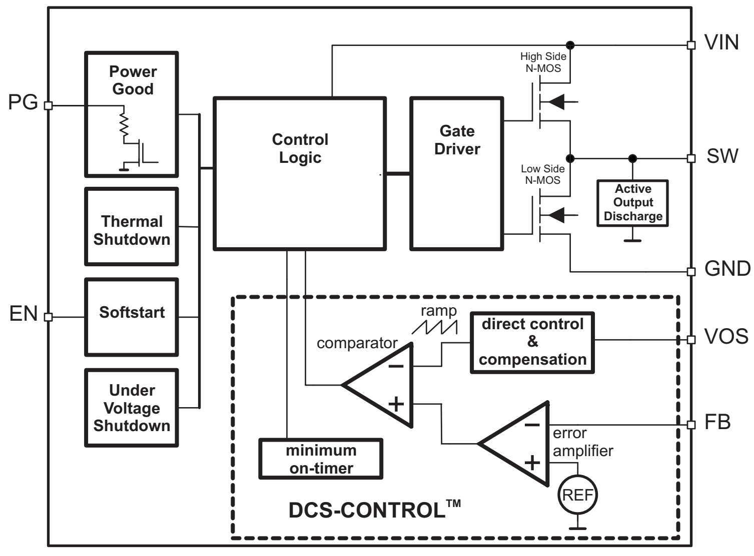


Figure 2. Functional Block Diagram

TYPICAL CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION

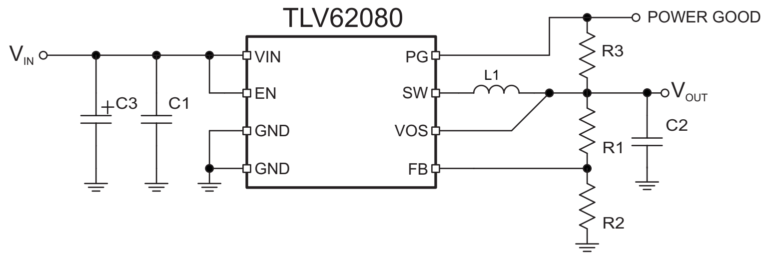


Table 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10uF, Ceramic Capacitor, 6.3V, X5R, size 0603	Std
C2	22uF, Ceramic Capacitor, 6.3V, X5R, size 0805, GRM21BR60J226ME39L	Murata
C3	47uF, Tantalum Capacitor, 8V, 35mΩ, size 3528, T520B476M008ATE035	Kemet
L1	1.0µH, Power Inductor, 2.2A, size 3x3x1.2mm, XFL3012-102MEB	Coilcraft
R1	Depending on the output voltage of TLV62080, 1%;	
R2	39.2k, Chip Resistor, 1/16W, 1%, size 0603	Std
R3	178k, Chip Resistor, 1/16W, 1%, size 0603	Std

TABLE OF GRAPHS

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Efficiency	Load Current, V_{OUT} = 0.9V	Figure 3
	Load Current, V_{OUT} = 1.2V	Figure 4
	Load Current, V_{OUT} = 2.5V	Figure 5
Output Voltage Accuracy	Input Voltage, V_{OUT} = 0.9V	Figure 6
	Input Voltage, V_{OUT} = 2.5V	Figure 7
	Load Current, V_{OUT} = 0.9V	Figure 8
	Load Current, V_{OUT} = 2.5V	Figure 9
Switching Frequency	Load Current, V_{OUT} = 2.5V,	Figure 10
Typical Operation	V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 500mA, PWM Mode	Figure 11
	V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 10mA, PFM Mode	Figure 12
Load Transient	V_{IN} = 3.3V, V_{OUT} = 1.2V, Load Current = 50mA to 1A	Figure 13
Line Transient	V_{IN} = 3.3V to 4.2V, V_{OUT} = 1.2V, Load = 2.2Ω	Figure 14
Startup	V_{IN} = 3.3V, V_{OUT} = 1.2V, Load = 2.2Ω	Figure 15
	V_{IN} = 3.3V, V_{OUT} = 1.2V, No Load	Figure 16

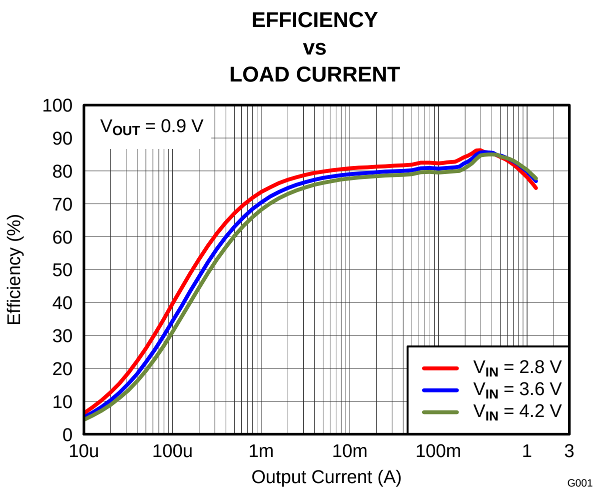

Figure 3.

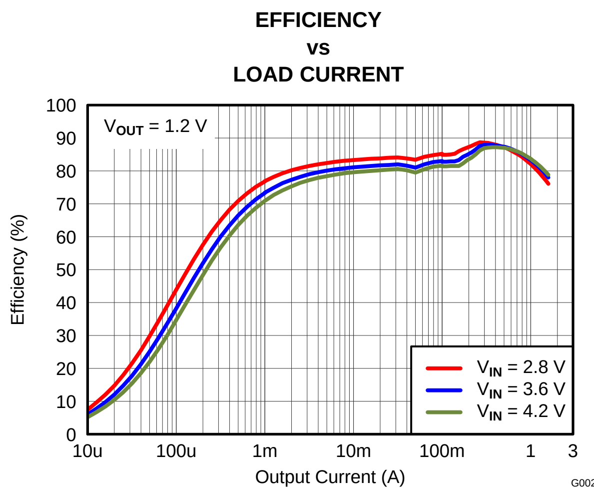

Figure 4.

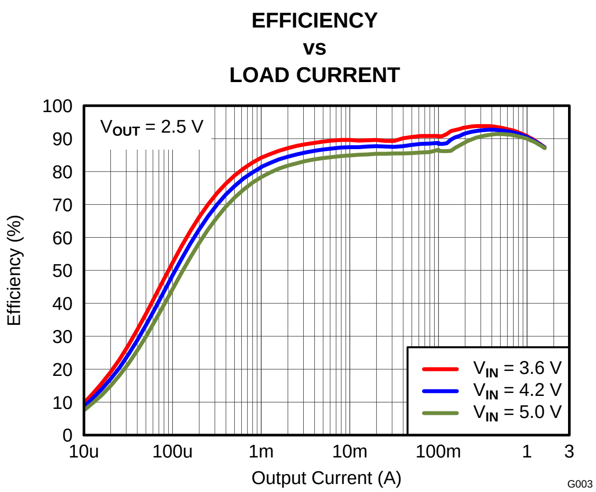

Figure 5.

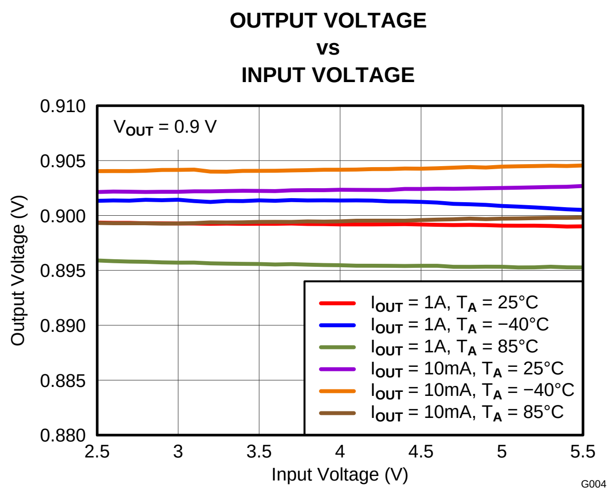

Figure 6.

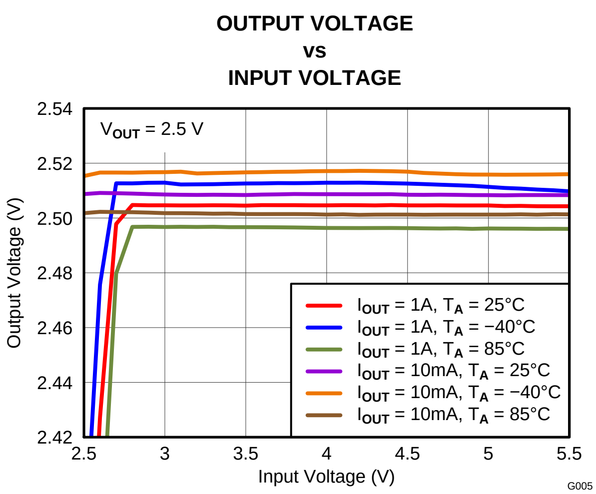

Figure 7.

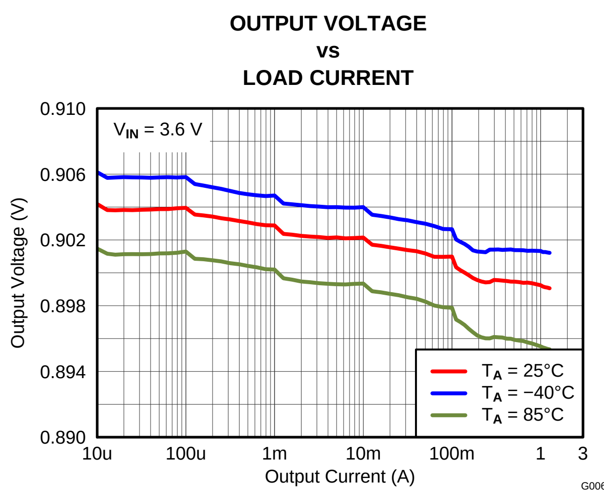

Figure 8.

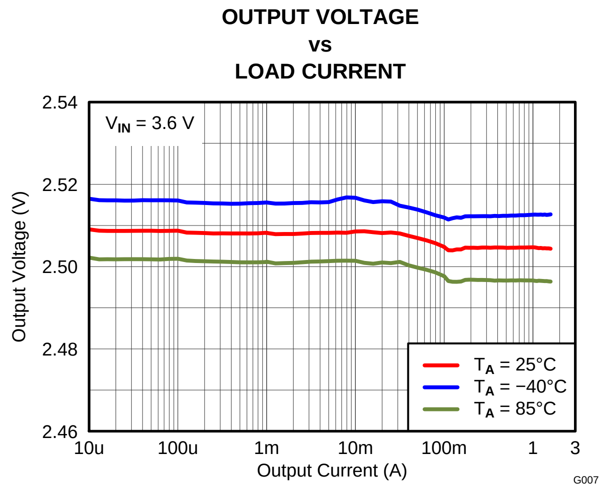

Figure 9.

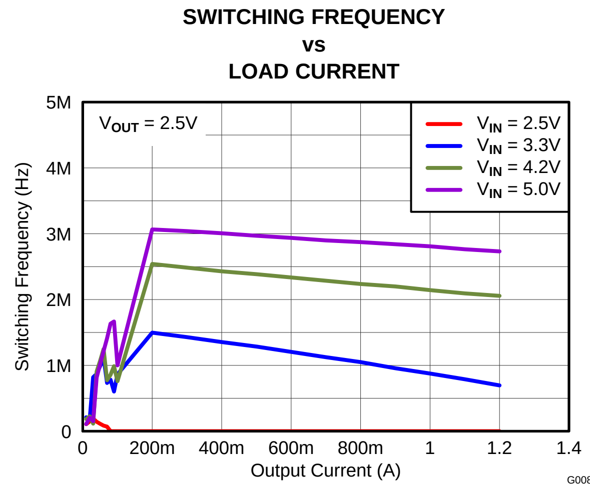

Figure 10.

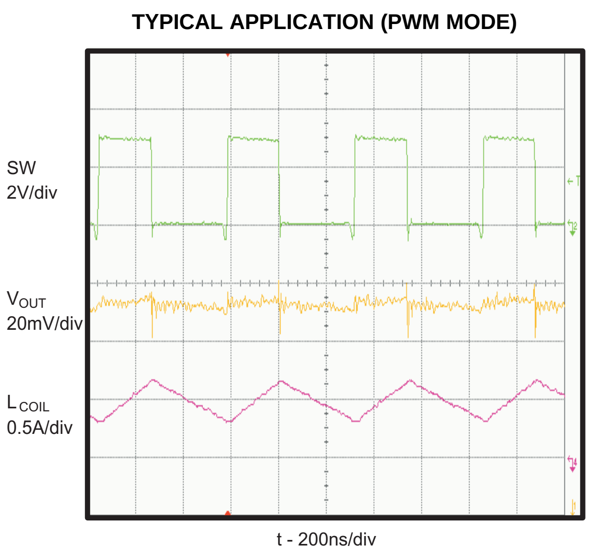

Figure 11.

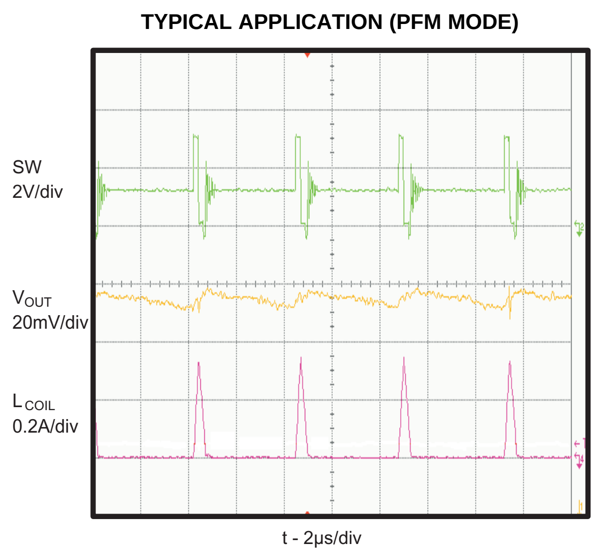

Figure 12.

LOAD TRANSIENT

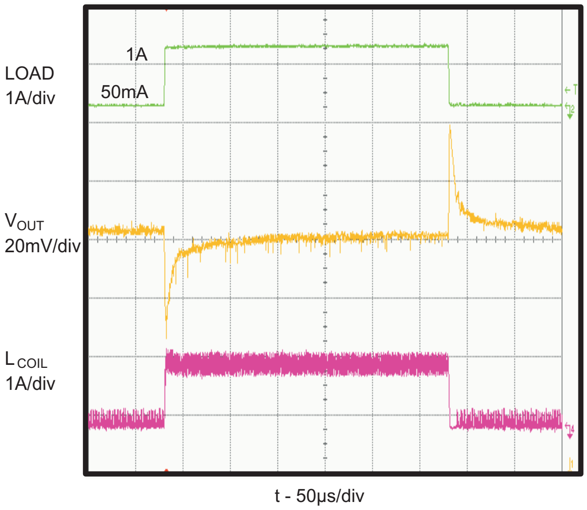

Figure 13.

LINE TRANSIENT

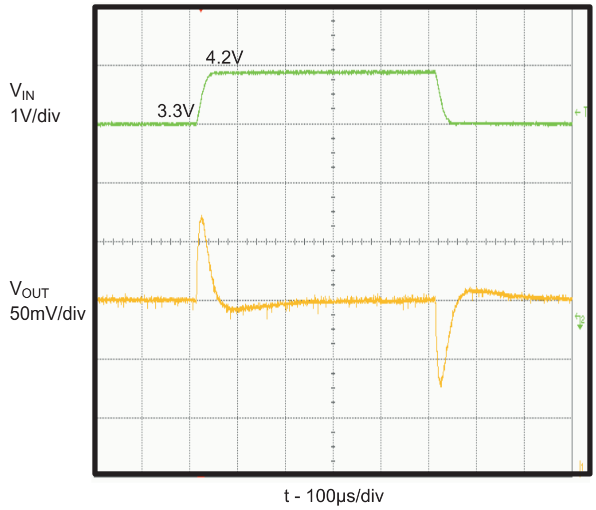

Figure 14.

START UP

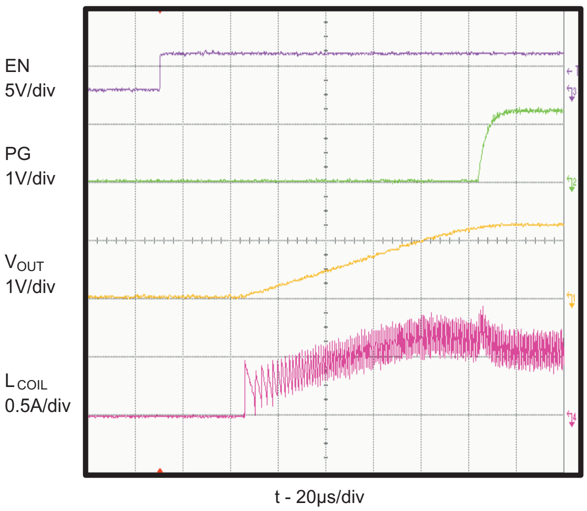

Figure 15.

START UP (WITHOUT LOAD)

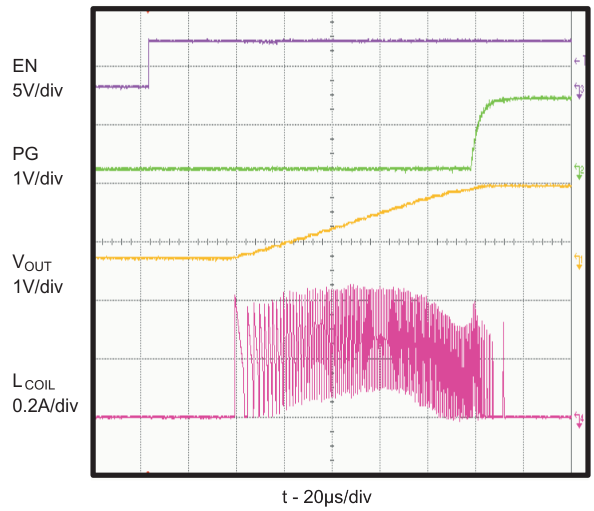

Figure 16.

DETAILED DESCRIPTION

DEVICE OPERATION

The TLV62080 synchronous switched mode converter is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM the converter operates with its nominal switching frequency of 2MHz having a controlled frequency variation over the input voltage range. As the load current decreases the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to Power Save Mode without effects on the output voltage. The TLV62080 offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

POWER SAVE MODE

As the load current decreases the TLV62080 enters the Power Save Mode operation. During Power Save Mode the converter operates with reduced switching frequency in PFM mode and with a minimum quiescent current maintaining high efficiency. The power save mode occurs when the inductor current becomes discontinuous. It is based on a fixed on time architecture. The typical on time is given by t_{on}=210ns·(V_{IN} / V_{OUT}). The switching frequency over the whole load current range is shown in Figure 10.

100% DUTY CYCLE LOW DROPOUT OPERATION

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on and the low side MOSFET is switched off. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain switching regulation, depending on the load current and output voltage can be calculated as:

$$V_{IN,MIN} = V_{OUT} + I_{OUT,MAX} \times (R_{DS(on)} + R_L) \quad (1)$$

With:

$V_{IN,MIN}$ = Minimum input voltage
$I_{OUT,MAX}$ = Maximum output current
$R_{DS(on)}$ = High side FET on-resistance
R_L = Inductor ohmic resistance

ENABLING / DISABLING THE DEVICE

The device is enabled by setting the EN input to a logic HIGH. Accordingly, a logic LOW disables the device. If the device is enabled, the internal power stage will start switching and regulate the output voltage to the programmed threshold. The EN input must be terminated with a resistance less than 1MΩ pulled to VIN or GND.

OUTPUT DISCHARGE

The output gets discharged by the SW pin with a typical discharge resistor of R_{DIS} whenever the device shuts down. This is the case when the device gets disabled by enable, thermal shutdown trigger, and undervoltage lockout trigger.

SOFT START

After enabling the device, an internal soft-start circuitry monotonically ramps up the output voltage and reaches the nominal output voltage during a soft start time (100µs, typical). This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

If the output voltage is not reached within the soft start time, such as in the case of heavy load, the converter will enter regular operation. Consequently, the inductor current limit will operate as described below. The TLV62080 is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

POWER GOOD

The TLV62080 has a power good output going low when the output voltage is below its nominal value. The power good keeps high impedance once the output is above 95% of the regulated voltage, and is driven to low once the output voltage falls below typically 90% of the regulated voltage. The PG pin is a open drain output and is specified to sink typically up to 0.5mA. The power good output requires a pull up resistor that is recommended connecting to the device output. When the device is off due to disable, UVLO or thermal shutdown, the PG pin is at high impedance.

The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. Leave the PG pin unconnected when not used.

UNDER VOLTAGE LOCKOUT

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, that shuts down the device at voltages lower than V_{UVLO} with a V_{HYS_UVLO} hysteresis.

THERMAL SHUTDOWN

The device goes into thermal shutdown once the junction temperature exceeds typically T_{JSD}. Once the device temperature falls below the threshold the device returns to normal operation automatically.

INDUCTOR CURRENT LIMIT

The Inductor Current Limit prevents the device from high inductor current and drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted/saturated inductor or a heavy load/shorted output circuit condition.

The incorporated inductor peak current limit measures the current during the high side and low side power MOSFET on-phase in PWM mode. Once the high side switch current limit is tripped, the high side MOSFET is turned off and the low side MOSFET is turned on to reduce the inductor current. Until the inductor current drops down to low side switch current limit, the low side MOSFET is turned off and the high side switch is turned on again. This operation repeats until the inductor current does not reach the high side switch current limit. Due to the internal propagation delay, the real current limit value can exceed the static current limit in the electrical characteristics table.

APPLICATION INFORMATION

Output Filter Design

The inductor and the output capacitor together provide a low pass frequency filter. To simplify this process Table 3 outlines possible inductor and capacitor value combinations for the most application.

Table 3. Matrix of Output Capacitor / Inductor Combinations

L [µH][(1)]	C_{OUT} [µF][(1)]				
	10	22	47	100	150
0.47					
1	+	+[(2)(3)]	+	+	
2.2	+	+	+	+	
4.7					

(1) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by+20% and -50%. Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Plus mark indicates recommended filter combinations.
(3) Filter combination in typical application.

Inductor Selection

Main parameter for the inductor selection is the inductor value and then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, Equation 2 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}} \quad (2)$$

Where

$I_{OUT,MAX}$ = Maximum output current
ΔI_L = Inductor current ripple
f_{SW} = Switching frequency
L = Inductor value

It's recommended to choose the saturation current for the inductor 20%~30% higher than the $I_{L,MAX}$, out of Equation 2. A higher inductor value is also useful to lower ripple current, but will increase the transient response time as well. The following inductors are recommended to be used in designs.

Table 4. List of Recommended Inductors

INDUCTANCE [µH]	CURRENT RATING [mA]	DIMENSIONS L x W x H [mm^3]	DC RESISTANCE [mΩ typ]	TYPE	MANUFACTURER
1.0	2500	3 x 3 x 1.2	35	XFL3012-102ME	Coilcraft
1.0	1650	3 x 3 x 1.2	40	LQH3NPN1R0NJ0	Murata
2.2	2500	4 x 3.7 x 1.65	49	LQH44PN2R2MP0	Murata
2.2	1600	3 x 3 x 1.2	81	XFL3012-222ME	Coilcraft

Capacitor Selection

The input capacitor is the low impedance energy source for the converter which helps to provide stable operation. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and GND as close as possible to that pins. For most applications 10µF will be sufficient, a larger value reduces input current ripple.

The architecture of the TLV62080 allows to use tiny ceramic-type output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its resistance up to high frequencies and to get narrow capacitance variation with temperature, it's recommended to use X7R or X5R dielectric. The TLV62080 is designed to operate with an output capacitance of 10µF to 100µF, as outlined in Table 3.

Table 5. List of Recommended Capacitors

CAPACITANCE [µF]	TYPE	DIMENSIONS L x W x H [mm^3]	MANUFACTURER
10	GRM188R60J106M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM188R60G226M	0603: 1.6 x 0.8 x 0.8	Murata
22	GRM21BR60J226M	0805: 2.0 x 1.2 x 1.25	Murata

Setting the Output Voltage

By selecting R_1 and R_2, the output voltage is programmed to the desired value. The following equation can be used to calculate R_1 and R_2.

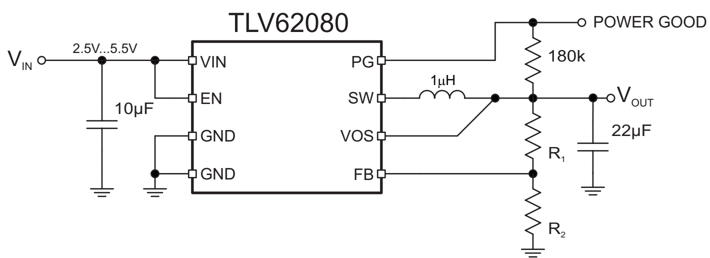

Figure 17. Typical Application Circuit

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.45V \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

For best accuracy, R2 should be kept smaller than 40kΩ to ensure that the current flowing through R2 is at least 100 times larger than I_{FB}. Changing the sum towards a lower value increases the robustness against noise injection. Changing the sum towards higher values reduces the quiescent current.

PCB Layout

The PCB layout is an important step to maintain the high performance of the TLV62080 device.

The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the traces short. Routing these traces direct and wide results in low trace resistance and low parasitic inductance. A common power GND should be used. The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.

The sense traces connected to FB and VOS pins are signal traces. Special care should be taken to avoid noise being induced. By a direct routing, parasitic inductance can be kept small. GND layers might be used for shielding. Keep these traces away from SW nodes.

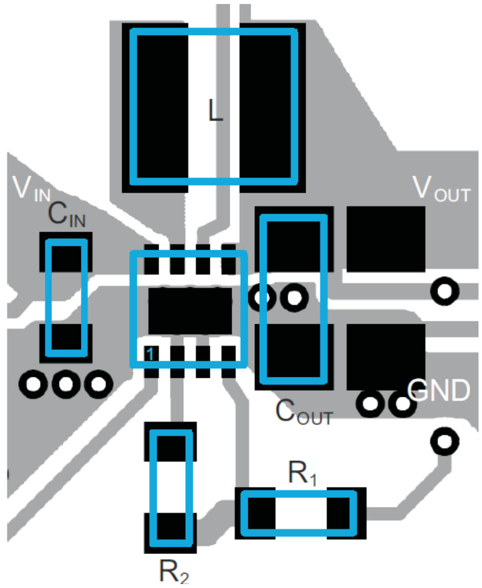

Figure 18. PCB Layout Suggestion

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the ThermalPAD™
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Notes SZZA017 and SPRA953.

APPLICATION EXAMPLES

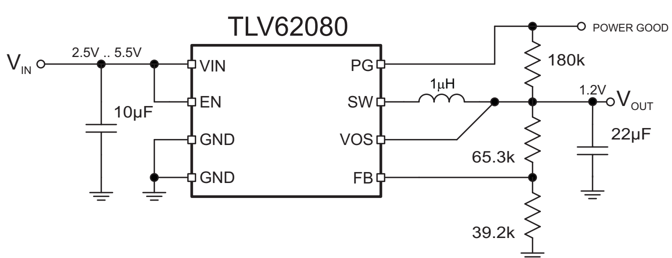

Figure 19. 1.2V Output Voltage Application

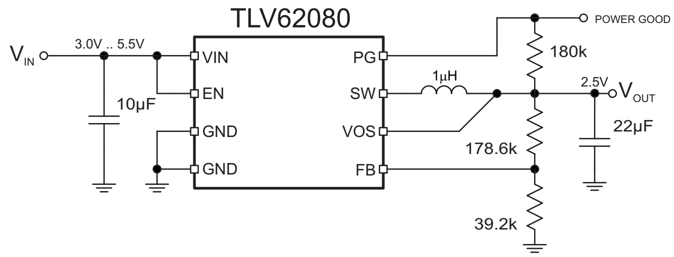

Figure 20. 2.5V Output Voltage Application

REVISION HISTORY

Changes from Original (October 2011) to Revision A — Page

Changes from Revision A (November 2011) to Revision B — Page