

TLP700

Industrial inverters
 Inverter for air conditioners
 IGBT/Power MOS FET gate drive

TLP700 consists of a GaAlAs light-emitting diode and an integrated photodetector.

This unit is 6-lead SDIP package. The TLP700 is 50% smaller than the 8-pin DIP and meets the reinforced insulation class requirements of international safety standards. Therefore the mounting area can be reduced in equipment requiring safety standard certification.

The TLP700 is suitable for gate driving circuits for IGBTs or power MOSFETs. In particular, the TLP700 is capable of "direct" gate driving of low-power IGBTs.

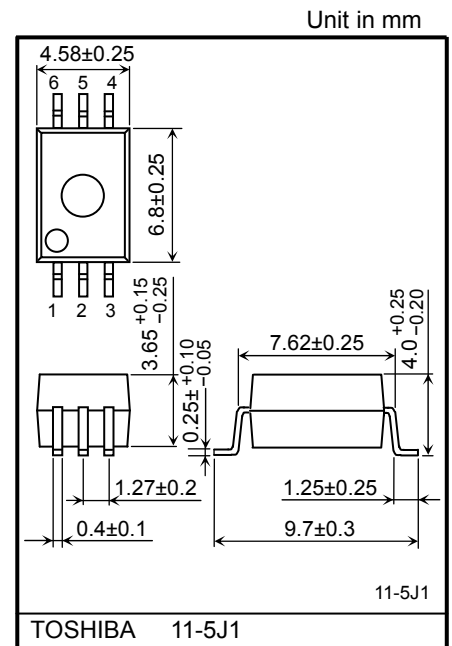
- Peak output current : ± 2.0 A (max)
- Guaranteed performance over temperature : $-40\sim 100^{\circ}\text{C}$
- Supply current : 2 mA (max)
- Power supply voltage : 15~30 V
- Threshold input current : $I_{FLH} = 5$ mA (max)
- Switching time (t_{pLH} / t_{pHL}) : 500 ns (max)
- Common mode transient immunity : ± 10 kV/ μs (min)
- Isolation voltage : 5000 Vrms (min)
- Construction mechanical rating

	7.62-mm pitch standard type	10.16-mm pitch TLPXXXXF type
Creepage Distance	7.0 mm (min)	8.0 mm (min)
Clearance	7.0 mm (min)	8.0 mm (min)
Insulation Thickness	0.4 mm (min)	0.4 mm (min)

- UL recognized : UL1577, File No. E67349
- Option (D4) type TÜV approval : EN60747-5-2 under plan

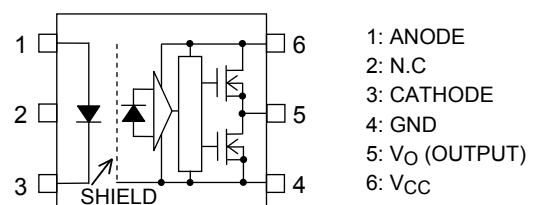
Truth Table

Input	LED	M1	M2	Output
H	ON	ON	OFF	H
L	OFF	OFF	ON	L

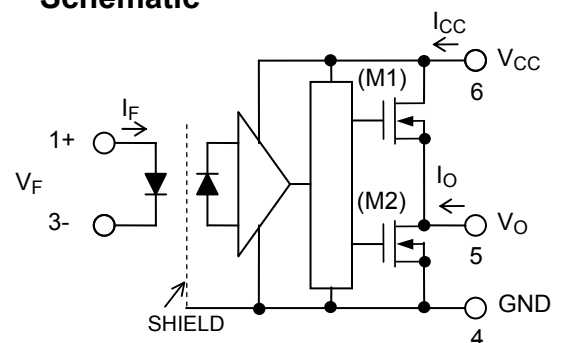


Weight: 0.26 g (typ.)

Pin Configuration (Top View)



Schematic



A 0.1- μF bypass capacitor must be connected between pins 6 and 4. (See Note 6.)

Absolute Maximum Ratings (Ta = 25 °C)

Characteristics		Symbol	Rating	Unit
LED	Forward current	I _F	20	mA
	Forward current derating (Ta ≥ 85°C)	ΔI _F /ΔTa	-0.54	mA/°C
	Peak transient forward current (Note 1)	I _{FP}	1	A
	Reverse voltage	V _R	6	V
	Junction temperature	T _j	125	°C
Detector	"H" peak output current	I _{OPH}	-2.0	A
	"L" peak output current			
	Output voltage	V _O	35	V
	Supply voltage	V _{CC}	35	V
	Junction temperature	T _j	125	°C
Operating frequency (Note 3)	f	50	kHz	
Operating temperature range	T _{opr}	-40~100	°C	
Storage temperature range	T _{stg}	-55~125	°C	
Lead soldering temperature (10 s) (Note 4)	T _{sol}	260	°C	
Isolation voltage (AC, 1 minute, R.H. ≤ 60%) (Note 5)	BV _S	5000	V _{rms}	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Pulse width P_W ≤ 1 μs, 300 pps

Note 2: Exponential waveform pulse width P_W ≤ 0.3 μs, f ≤ 15 kHz

Note 3: Exponential waveform I_{OPH} ≤ -1.5 A (≤ 0.3 μs), I_{OPL} ≤ +1.5 A (≤ 0.3 μs), Ta=100°C

Note 4: For the effective lead soldering area

Note 5: Device considered a two-terminal device: pins 1, 2 and 3 paired with pins 4, 5 and 6 respectively.

Note 6: A ceramic capacitor (0.1 μF) should be connected from pin 6 to pin 4 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property.
The total lead length between capacitor and coupler should not exceed 1 cm.

Recommended Operating Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Input current, ON (Note 7)	I _F (ON)	7.5	—	10	mA
Input voltage, OFF	V _F (OFF)	0	—	0.8	V
Supply voltage * (Note 8)	V _{CC}	15	—	30	V
Peak output current	I _{OPH} / I _{OPL}	—	—	± 1.5	A
Operating temperature	T _{opr}	-40	—	100	°C

* This item denotes operating ranges, not meaning of recommended operating conditions.

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Note 7: Input signal rise time (fall time) ≤ 0.5 μs.

Note 8: If the V_{cc} rise slope is sharp, an internal circuit might not operate with stability. Please design the V_{cc} rise slope under 3.0 V/μs.

Electrical Characteristics (Ta = -40~100 °C, unless otherwise specified)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Forward voltage		V _F	—	I _F = 10 mA, Ta = 25 °C	—	1.57	1.75	V	
Temperature coefficient of forward voltage		ΔV _F /ΔTa	—	I _F = 10 mA	—	-2.0	—	mV/°C	
Input reverse current		I _R	—	V _R = 6 V, Ta = 25 °C	—	—	10	μA	
Input capacitance		C _T	—	V = 0 V, f = 1 MHz, Ta = 25 °C	—	100	—	pF	
Output current (Note 9)	"H" Level	I _{OPH1}	1	V _{CC} = 15 V I _F = 5 mA	V ₆₋₅ = -3.5 V	-1.0	-1.4	—	A
		I _{OPH2}			V ₆₋₅ = -7 V	-1.5	—		
	"L" Level	I _{OPL1}	2	V _{CC} = 15 V I _F = 0 mA	V ₅₋₄ = 2.5 V	1.0	1.4	—	
		I _{OPL2}			V ₅₋₄ = 7 V	1.5	—	—	
Output voltage	"H" Level	V _{OH}	3	V _{CC1} =+15V, V _{EE1} =-15V R _L = 200Ω, I _F = 5 mA	11	13.7	—	V	
	"L" Level	V _{OL}	4	V _{CC1} =+15V, V _{EE1} =-15V R _L = 200Ω, V _F = 0.8 V	—	-14.9	-12.5		
Supply current	"H" Level	I _{CCH}	5	V _{CC} = 30 V V _O = Open	I _F = 10 mA	—	1.3	2.0	mA
	"L" Level	I _{CCL}	6		I _F = 0 mA	—	1.3	2.0	
Threshold input current	L → H	I _{FLH}	—	V _{CC} = 15 V, V _O > 1 V	—	1.8	5	mA	
Threshold input voltage	H → L	V _{FHL}	—	V _{CC} = 15 V, V _O < 1 V	0.8	—	—	V	
Supply voltage	V _{CC}		—	—	15	—	30	V	
UVLO thresh hold	V _{UVLO+}		—	V _O > 2.5V, I _F = 5 mA	11.0	12.5	13.5	V	
	V _{UVLO-}		—	V _O < 2.5V, I _F = 5 mA	9.5	11.0	12.0	V	
UVLO hysteresis	V _{UVLOHYS}		—	—	—	1.5	—	V	

(*): All typical values are at Ta = 25 °C

Note 9: Duration of I_O time ≤ 50 μs, 1 pulse

Note 10: This product is more sensitive than conventional products to electrostatic discharge (ESD) owing to its low power consumption design.

It is therefore all the more necessary to observe general precautions regarding ESD when handling this component.

Isolation Characteristics (Ta = 25 °C)

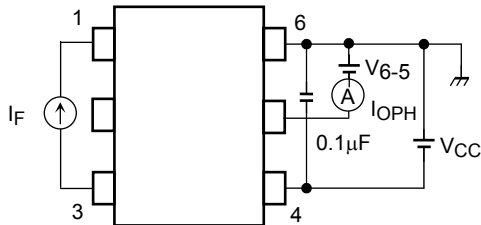
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Capacitance input to output	C _S	V _s = 0 V, f = 1MHz (Note 5)	—	1.0	—	pF
Isolation resistance	R _S	R.H. ≤ 60 %, V _S = 500 V (Note 5)	1×10 ¹²	10 ¹⁴	—	Ω
Isolation voltage	BV _S	AC, 1 minute	5000	—	—	V _{rms}
		AC, 1 second, in oil	—	10000	—	
		DC, 1 minute, in oil	—	10000	—	V _{dc}

Switching Characteristics (Ta = -40~100 °C, unless otherwise specified)

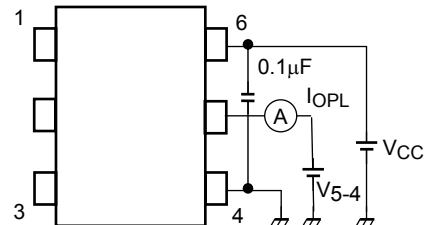
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.*	Max	Unit	
Propagation delay time	L → H	7	V _{CC} = 30 V R _g = 20 Ω C _g = 10 nF	I _F = 0 → 5 mA	50	—	500	ns
	H → L			t _{pHL}	I _F = 5 → 0 mA	50	—	
Output rise time (10–90 %)	t _r	7	V _{CC} = 30 V R _g = 20 Ω C _g = 10 nF	I _F = 0 → 5 mA	—	50	—	ns
Output fall time (90–10 %)	t _f			I _F = 5 → 0 mA	—	50	—	
Switching time dispersion between ON and OFF	t _{pHL} - t _{pLH}	7	V _{CC} = 30 V	I _F = 0 ↔ 5 mA	—	—	250	ns
Common mode transient immunity at HIGH level output	CM _H	8	V _{CM} = 1000 Vp-p Ta = 25 °C	I _F = 5 mA V _O (min) = 26 V	-10000	—	—	V/μs
Common mode transient immunity at LOW level output	CM _L		V _{CC} = 30 V	I _F = 0 mA V _O (max) = 1 V	10000	—	—	

(*): All typical values are at Ta = 25 °C.

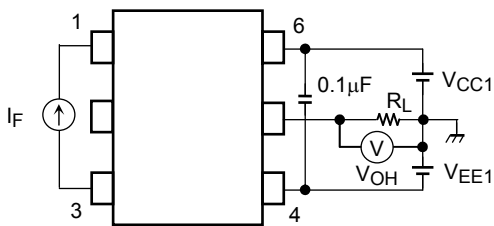
Test Circuit 1: I_{OPH}



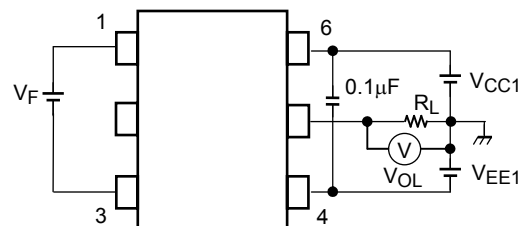
Test Circuit 2: I_{OPL}



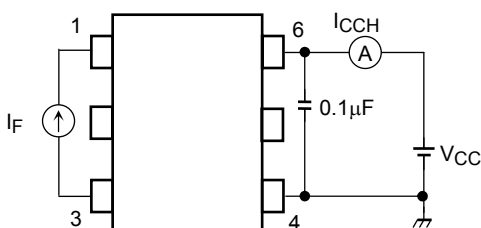
Test Circuit 3: V_{OH}



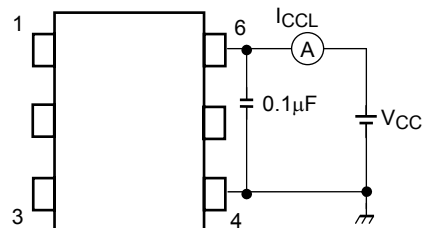
Test Circuit 4: V_{OL}



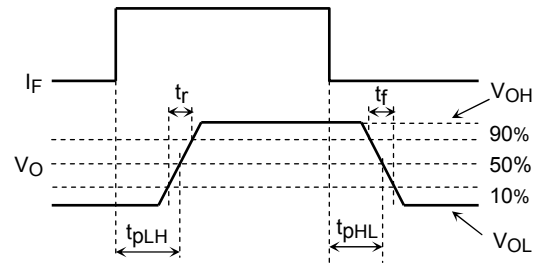
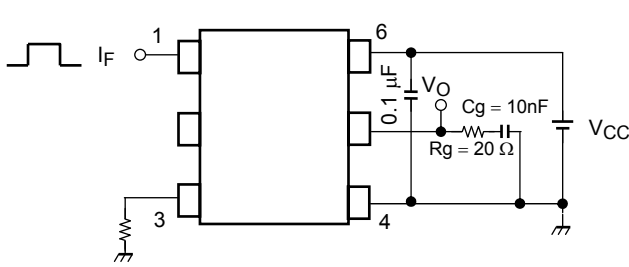
Test Circuit 5: I_{CCH}



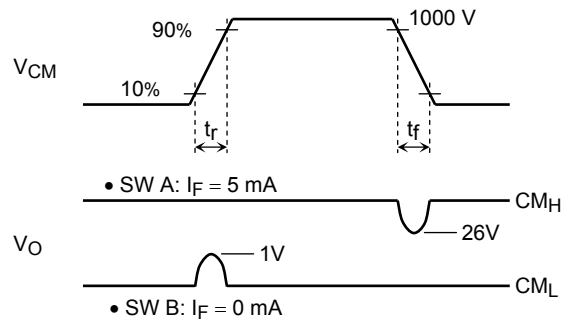
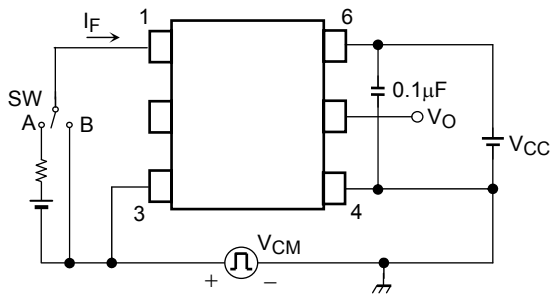
Test Circuit 6: I_{CCL}



Test Circuit 7: t_{pLH} , t_{pHL} , t_r , t_f , $|t_{pHL}-t_{pLH}|$



Test Circuit 8: CM_H , CM_L



$$CM_H = - \frac{800 \text{ V}}{t_f (\mu\text{s})}$$

$$CM_L = \frac{800 \text{ V}}{t_r (\mu\text{s})}$$

CM_L (CM_H) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the LOW (HIGH) state.

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20070701-EN

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