

DSI Inertial Sensor

The MMA26xxKW family of devices are DSI2.5 compatible overdamped X-axis satellite accelerometers.

Features

- $\pm 25g$ to $\pm 312.5g$ Nominal Full-Scale Range
- Selectable 180 Hz, 2-pole, 400 Hz, 4-pole, or 800 Hz, 4-pole LPF
- DSI2.5 Compatible with full support of Mandatory Commands
- Internal High Side Bus Switch for DSI2.5 Daisy Chain Applications
- 16 μs internal sample rate, with interpolation to 1 ms
- $-40^{\circ}C$ to $125^{\circ}C$ Operating Temperature Range
- Pb-Free 16-Pin QFN, 6 by 6 Package
- Qualified AECQ100, Revision G, Grade 1 ($-40^{\circ}C$ to $+125^{\circ}C$)
(<http://www.aecouncil.com/>)

Typical Applications

- Airbag Front and Side Crash Detection

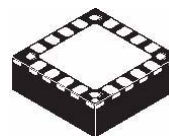
ORDERING INFORMATION

| Device | Axis | Range | Package | Shipping |
|-------------|-------------|---------|-------------|-------------|
| MMA2602KW | X | 25g | 2086-01 | Tubes |
| MMA2605KW | X | 50g | 2086-01 | Tubes |
| MMA2606KW | X | 62.5g | 2086-01 | Tubes |
| MMA2612KW | X | 125g | 2086-01 | Tubes |
| MMA2618KW | X | 187g | 2086-01 | Tubes |
| MMA2631KW | X | 312g | 2086-01 | Tubes |
| MMA2602KWR2 | X | 25g | 2086-01 | Tape & Reel |
| MMA2605KWR2 | X | 50g | 2086-01 | Tape & Reel |
| MMA2606KWR2 | X <td 62.5g | 2086-01 | Tape & Reel | |
| MMA2612KWR2 | X | 125g | 2086-01 | Tape & Reel |
| MMA2618KWR2 | X | 187g | 2086-01 | Tape & Reel |
| MMA2631KWR2 | X | 312g | 2086-01 | Tape & Reel |

For user register array programming, please consult your Freescale representative.

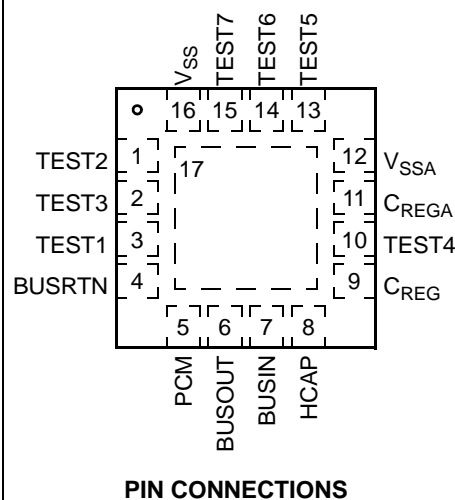
MMA26xxKW

Bottom View



16-PIN QFN
CASE 2086-01

Top View



Application Diagram

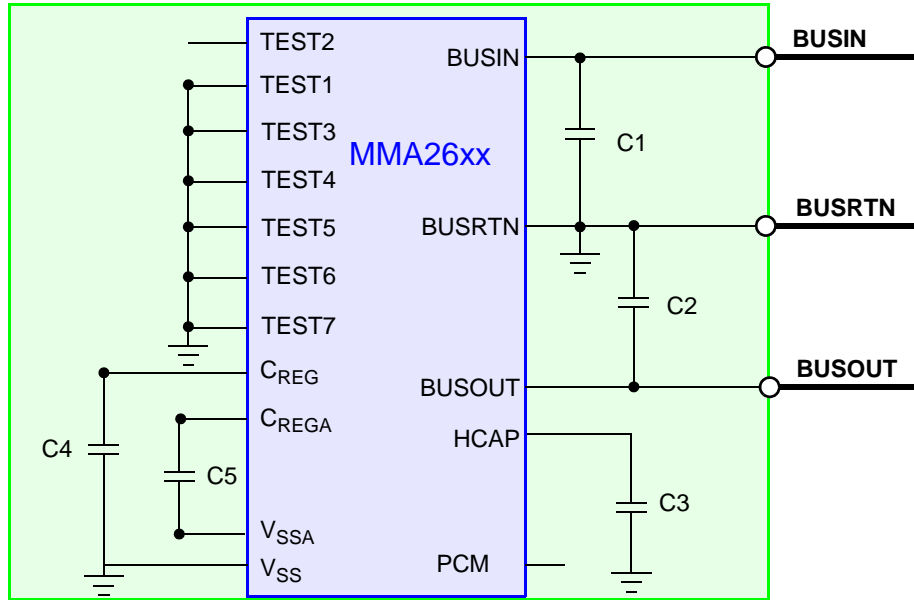


Figure 1. Application Diagram

| External Component Recommendations | | | |
|------------------------------------|-------------------|--------------------------------------|---|
| Ref Des | Type | Description | Purpose |
| C1 | Ceramic | 100 pF ≤ C1 ≤ 1000 pF 10%, 50V, X7R | BUSIN Power Supply Decoupling, ESD |
| C2 | Ceramic | 100 pF ≤ C2 ≤ 1000 pF, 10%, 50V, X7R | BUSOUT Power Supply Decoupling, ESD |
| C3 | Ceramic, Tantalum | 1 μF ≤ C3 ≤ 100 μF, 10%, 50V, X7R | Reservoir Capacitor for Keep Alive during Signaling |
| C4 | Ceramic | 1 μF, 10%, 10V, X7R | Voltage Regulator Output Capacitor (C _{REG}) |
| C5 | Ceramic | 1 μF, 10%, 10V, X7R | Voltage Regulator Output Capacitor (C _{REGA}) |

Device Orientation

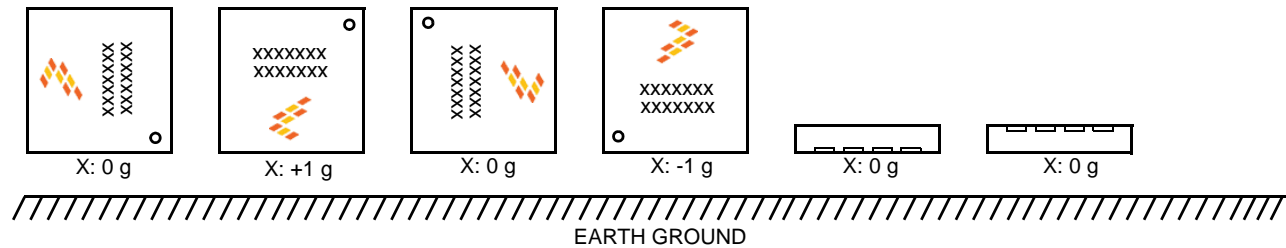


Figure 2. Device Orientation Diagram

Internal Block Diagram

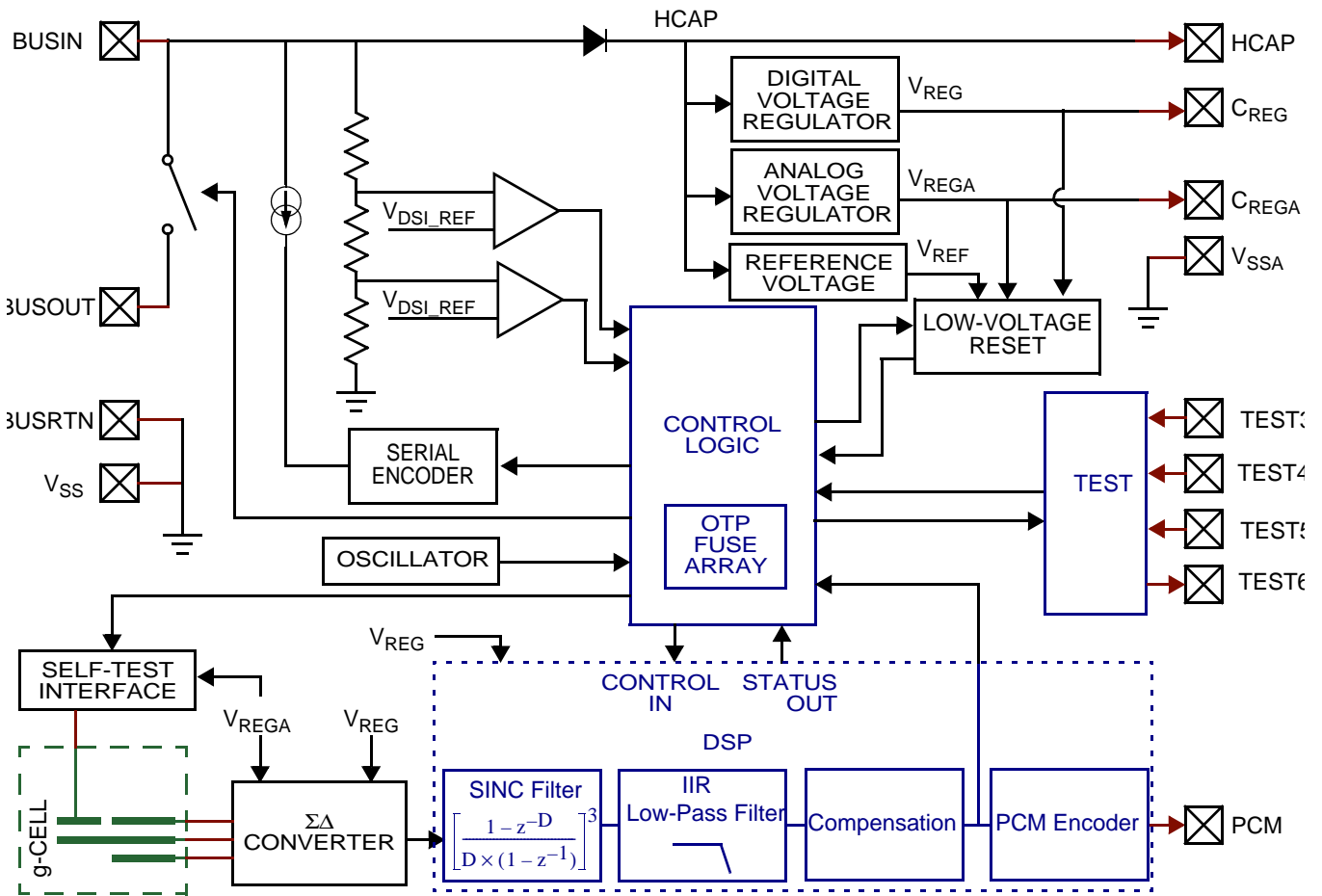


Figure 3. Block Diagram

1 Pin Connections

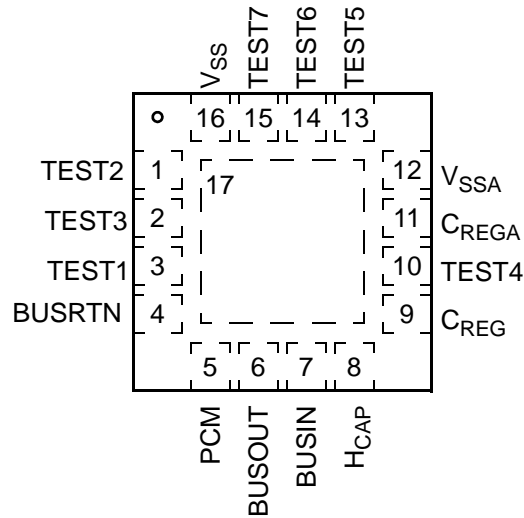


Figure 4. Block Diagram

Table 1. Pin Description

| Pin | Pin Name | Formal Name | Definition |
|-----|-------------------|----------------|--|
| 1 | TEST2 | Test Pin | This pin must be left unconnected in the application. |
| 2 | TEST3 | Test Pin | This pin must be grounded in the application. |
| 3 | TEST1 | Test Pin | This pin must be grounded in the application. |
| 4 | BUSRTN | Ground | This pin is the common return for power and signalling. |
| 5 | PCM | PCM Output | This pin provides a 4 MHz PCM signal proportional to the acceleration data for test purposes. The output can be enabled or disabled via OTP. If unused, this pin must be left unconnected in the application. Reference Section 3.5.3.6 . |
| 6 | BUSOUT | BUS output | This pin is internally connected to BUSIN through a switch. For daisy chain configurations, this pin is connected to the BUSIN pin of the next slave on the DSI bus. The internal bus switch is open following reset, and is closed when an Initialization command is received. |
| 7 | BUSIN | Supply / Comm | This pin is connected to the DSI positive bus node & provides the power supply & communication to the system master. An external capacitor must be connected between this pin and the BUSRTN pin. Reference Figure 1 . |
| 8 | HCAP | Hold Capacitor | This pin rectifies the supply voltage on the BUSIN pin to create the supply voltage for the device. An external capacitor must be connected between this pin and the BUSRTN pin to store energy for operation during master communication signalling. Reference Figure 1 . |
| 9 | C _{REG} | Digital Supply | This pin is connected to the power supply for the internal digital circuitry. An external capacitor must be connected between this pin and V _{SS} . Reference Figure 1 . |
| 10 | TEST4 | Test Pin | This pin must be grounded in the application. |
| 11 | C _{REGA} | Analog Supply | This pin is connected to the power supply for the internal analog circuitry. An external capacitor must be connected between this pin and V _{SSA} . Reference Figure 1 . |
| 12 | VSSA | Analog GND | This pin is the power supply return node for analog circuitry. |
| 13 | TEST5 | Test Pin | This pin enables test mode, and provides the SPI programming voltage in test mode. This pin is must be grounded in the application. |
| 14 | TEST6 | Test Pin | This pin must be grounded in the application. |
| 15 | TEST7 | Test Pin | This pin must be grounded in the application. |
| 16 | VSS | Digital GND | This pin is the power supply return node for the digital circuitry. |
| 17 | PAD | Die Attach Pad | This pin is the die attach flag, & should be connected to VSS in the application. Reference Section 5 . |
| | Corner Pads | Corner Pads | The corner pads are internally connected to V _{SS} . |

2 Electrical Characteristics

2.1 Maximum Ratings

Maximum ratings are the extreme limits to which the device can be exposed without permanently damaging it. Do not apply voltages higher than those shown in the table below.

| # | Rating | Symbol | Value | Unit | |
|----|---|---------------|---------------|------|------|
| 1 | Supply Voltage (continuous) (BUSIN, BUSOUT, HCAP) | V_{CC} | -0.3 to +30.0 | V | (3) |
| 2 | Supply Voltage (pulsed < 400 ms, repetition rate 60s) (BUSIN, BUSOUT, HCAP) | V_{CC} | -0.3 to +34.0 | V | (3) |
| 3 | C_{REG} , C_{REGA} , PCM, TEST1, TEST2, TEST3, TEST4, TEST5, TEST6, TEST7 | | -0.3 to +3.0 | V | (3) |
| 4 | BUSIN, BUSOUT, BUSRTN and H_{CAP} Current | | | | |
| 5 | Maximum duration 1 s | I_{IN} | 400 | mA | (3) |
| 5 | Continuous | I_{IN} | 75 | mA | (3) |
| 6 | Powered Shock (six sides, 0.5 ms duration) | g_{pms} | ±2000 | g | (5) |
| 7 | Unpowered Shock (six sides, 0.5 ms duration) | g_{shock} | ±2000 | g | (5) |
| 8 | Drop Shock (to concrete, tile or steel surface, 10 drops, any orientation) | h_{DROP} | 1.2 | m | (5) |
| 9 | Electrostatic Discharge (per AECQ100) | | | | |
| 9 | HBM (100 pF, 1.5 kΩ) | V_{ESD} | ±2000 | V | (5) |
| 10 | CDM (R = 0Ω) | V_{ESD} | ±500 | V | (5) |
| 11 | MM (200 pF, 0Ω) | V_{ESD} | ±200 | V | (5) |
| 12 | Temperature Range | | | | |
| 12 | Storage | T_{stg} | -40 to +125 | °C | (3) |
| 13 | Junction | T_J | -40 to +150 | °C | (3) |
| 14 | Thermal Resistance | θ_{JC} | 2.5 | °C/W | (11) |

2.2 Operating Range

The operating ratings are the limits normally expected in the application.

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|---|------------|-------|-----|-------|-------|--------|
| 15 | Supply Voltage | | V_L | | V_H | | (1,12) |
| 16 | V_{HCAP} | V_{HCAP} | 6.3 | — | 30 | V | (1,12) |
| 16 | BUSIN | V_{BUS} | -0.3 | — | 30 | V | (1,12) |
| 17 | Programming Voltage Applied to BUSIN (DSI) | V_{PP} | 14.0 | — | 30.0 | V | (3) |
| 18 | Programming Current BUSIN | I_{PP} | 85 | — | — | mA | (3) |
| 19 | Operating Temperature Range | | T_L | | T_H | | (1) |
| 20 | | T_A | -40 | — | +105 | °C | (3) |
| 20 | | T_A | -40 | — | +125 | °C | (3) |

2.3 Electrical Characteristics - Supply and I/O

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | | |
|----|---|--|--------------------------------|------|-------|-------------|-------------|-------|
| 21 | Quiescent Supply Current * | I_{DD} | — | — | 8.0 | mA | (1) | |
| 22 | Inrush Current (excluding HCAP Capacitor charge current) Power On until V_{REG} Stable | I_{INRUSH} | — | — | 20 | mA | (3) | |
| 23 | Internally Regulated Voltages | V_{REG} | 2.425 | 2.50 | 2.575 | V | (1) | |
| 24 | | V_{REGA} | 2.425 | 2.50 | 2.575 | V | (1) | |
| 25 | V_{HCAP} Under-Voltage Detection (See Figure 5) Under-Voltage Detection Threshold | $V_{PORHCAP_f}$ | 5.8 | 6.0 | 6.2 | V | (3,6) | |
| 26 | | V_{HCAP} Recovery Threshold | — | — | 6.3 | V | (3,6) | |
| 27 | | Hysteresis ($V_{PORHCAP_f} - V_{PORHCAP_r}$) | V_{HYST_HCAP} | 70 | 100 | 140 | mV | (3) |
| 28 | Internal Regulator Low Voltage Detection Threshold | $V_{PORVREG_f}$ | 2.15 | 2.25 | 2.40 | V | (3,6) | |
| 29 | | V_{REGA} Falling | $V_{PORVREGA_f}$ | 2.15 | 2.25 | 2.40 | V | (3,6) |
| 30 | | Hysteresis | V_{HYST_VREG} | 0.05 | 0.10 | 0.15 | V | (3) |
| 31 | | | V_{HYST_VREGA} | 0.05 | 0.10 | 0.15 | V | (3) |
| 32 | External Capacitor (C_{REG} , C_{REGA}) Capacitance | C_{REG} , C_{REGA} | 500 | 1000 | 1500 | nF | (9) | |
| 33 | | ESR (including interconnect resistance) | $R_{CREGESR}$, $R_{CREGAESR}$ | — | — | 200 | m Ω | (9) |
| 34 | Output High Voltage (PCM) $I_{Load} = 100 \mu A$ | V_{OH} | $V_{REG} - 0.1$ | — | — | V | (9) | |
| 35 | Output Low Voltage (PCM) $I_{Load} = 100 \mu A$ | V_{OL} | — | — | 0.1 | V | (9) | |
| 36 | Temperature Monitoring | Under-Temperature Monitor Threshold | — | — | -55 | $^{\circ}C$ | (9) | |
| 37 | | Over-Temperature Monitor Threshold | T_{UNDER} T_{OVER} | 155 | — | — | $^{\circ}C$ | (9) |

2.4 Electrical Characteristics - DSI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|---|-------------------------|------|------|------|----------|-----|
| 38 | BUSOUT Bus Switch Resistance $0V \leq V_{BUSIN} \leq 30V$, $I_{SW} = 160mA$ | R_{SW} | — | 4.0 | 8.0 | Ω | (1) |
| 39 | HCAP Rectifier Leakage Current $V_{BUSIN} = 0V$, $V_{HCAP} = 9.0V$ | I_{RLKG} | — | — | 100 | μA | (1) |
| 40 | BUSIN to HCAP Rectifier Voltage Drop ($V_{BUSIN} = 7V$) $I_{HCAP} = -15mA$ $I_{HCAP} = -100mA$ | V_{RECT} | — | 0.75 | 1.0 | V | (1) |
| 41 | | V_{RECT} | — | 0.9 | 1.2 | V | (1) |
| 42 | BUSIN Bias Current $V_{BUSIN} = 8.0V$, $V_{HCAP} = 9.0V$ $V_{BUSIN} = 4.5V$, $V_{HCAP} = 24V$, No Response Current | I_{BUSIN_BIAS} | -100 | — | 100 | μA | (1) |
| 43 | | I_{BUSIN_BIAS} | -100 | — | 100 | μA | (1) |
| 44 | BUSOUT Bias Current $V_{BUSOUT} = 8.0V$, $V_{HCAP} = 9.0V$ $V_{BUSOUT} = 4.5V$, $V_{HCAP} = 24V$, No Response Current | I_{BUSOUT_BIAS} | -100 | — | 100 | μA | (1) |
| 45 | | I_{BUSOUT_BIAS} | -100 | — | 100 | μA | (1) |
| 46 | BUSOUT Discharge Resistance | $R_{BUSOUT_Discharge}$ | 3500 | — | 8000 | Ω | (3) |
| 47 | BUSIN Response Current $V_{BUSIN} = 4.0V$ | I_{RESP} | 9.9 | 11 | 12.1 | mA | (1) |
| 48 | BUSIN to BUSOUT Leakage Current (BUS SWITCH open) $V_{BUSIN} = 24.0V$, $V_{BUSOUT} = 0V$ $V_{BUSIN} = 0V$, $V_{BUSOUT} = 16V$ | I_{SW_Leak} | -20 | — | 20 | μA | (1) |
| 49 | | I_{RSW_Leak} | -20 | — | 20 | μA | (1) |
| 50 | BUSIN Logic Thresholds | | | | | | |
| | Signal Threshold | V_{THS} | 2.8 | 3.0 | 3.2 | V | (1) |
| 51 | Frame Threshold | V_{THF} | 5.5 | 6.0 | 6.5 | V | (1) |
| 52 | BUSIN Logic Hysteresis | | | | | | |
| | Signal | V_{HYSS} | 30 | — | 90 | mV | (3) |
| 53 | Frame | V_{HYSF} | 100 | — | 300 | mV | (3) |

2.5 Electrical Characteristics - Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|---|---------------------|-----|-------|------|-------|--------|
| 54 | Sensitivity (10-bit @ 100Hz referenced to 0Hz) 25g Range 50g Range 62.5g Range 125g Range 187g Range 312g Range | $SENS$ | — | 20.48 | — | LSB/g | (1,14) |
| 55 | | $SENS$ | — | 10.24 | — | LSB/g | (1,14) |
| 56 | | $SENS$ | — | 8.192 | — | LSB/g | (1,14) |
| 57 | | $SENS$ | — | 4.096 | — | LSB/g | (1,14) |
| 58 | | $SENS$ | — | 2.731 | — | LSB/g | (1,14) |
| 59 | | $SENS$ | — | 1.638 | — | LSB/g | (1,14) |
| 60 | Total Sensitivity Error (including non-linearity) $T_A = 25^\circ C$ $T_L \leq T_A \leq T_H$ | $\Delta SENS_{25}$ | -5 | — | +5 | % | (1) |
| 61 | | $\Delta SENS$ | -7 | — | +7 | % | (1) |
| 62 | Digital Offset 10-bit output | OFF_{10Bit} | 460 | 512 | 564 | LSB | (1) |
| 63 | Range of Output (10-Bit Mode) Acceleration Internal Error | $RANGE_{ACC}$ | 1 | — | 1023 | LSB | (3) |
| 64 | | $RANGE_{ERR}$ | — | 0 | — | LSB | (3) |
| 65 | Cross-Axis Sensitivity Z-axis to X-axis Y-axis to X-axis | V_{ZX} | -5 | — | +5 | % | (3) |
| 66 | | V_{YX} | -5 | — | +5 | % | (3) |
| 67 | ADC Output Noise Peak (1 Hz - 1 kHz, 10-Bit) | n_{SD} | -4 | — | +4 | LSB | (3) |
| 68 | System Output Noise (10-Bit, RMS, All Ranges) | n_{RMS} | — | — | +1.2 | LSB | (3) |
| 69 | Non-linearity (all ranges) 10-bit output, Range < 50g 10-bit output, 50g \leq Range \leq 312.5g | NL_{OUT_sub50g} | -2 | — | +2 | % | (3) |
| 70 | | $NL_{OUT_sub250g}$ | -2 | — | +2 | % | (3) |

2.6 Electrical Characteristics - Self-Test and Overload

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|----|---|----------------------------|------|------|------|-------|-----|
| 71 | Acceleration (without hitting internal g-cell stops) ±25g, ±50g, ±62.5g, ±125g | $g_{g-cell_Clip60X}$ | 400 | 456 | 500 | g | (9) |
| 72 | Acceleration (without hitting internal g-cell stops) ±187g, ±312g | $g_{g-cell_Clip240X}$ | 1750 | 2065 | 2300 | g | (9) |
| 73 | $\Sigma\Delta$ and Sinc Filter Clipping Limit ±25g | $g_{ADC_Clip60X}$ | 98 | 108 | 121 | g | (9) |
| 74 | $\Sigma\Delta$ and Sinc Filter Clipping Limit ±50g | $g_{ADC_Clip60X}$ | 191 | 210 | 232 | g | (9) |
| 75 | $\Sigma\Delta$ and Sinc Filter Clipping Limit ±62.5g | $g_{ADC_Clip60X}$ | 191 | 210 | 232 | g | (9) |
| 76 | $\Sigma\Delta$ and Sinc Filter Clipping Limit ±125g | $g_{ADC_Clip120X}$ | 353 | 379 | 409 | g | (9) |
| 77 | $\Sigma\Delta$ and Sinc Filter Clipping Limit ±187g | $g_{ADC_Clip240X}$ | 1690 | 1876 | 2106 | g | (9) |
| 78 | $\Sigma\Delta$ and Sinc Filter Clipping Limit ±312g | $g_{ADC_Clip480X}$ | 1690 | 1876 | 2106 | g | (9) |
| 79 | Deflection, 10-Bit, Self-Test - Offset, 30 sample ave, $T_A = 25^\circ\text{C}$) ±25g Range * | $\Delta\text{DFLCT_X25}$ | — | 246 | — | LSB | (1) |
| 80 | ±50g Range * | $\Delta\text{DFLCT_X50}$ | — | 123 | — | LSB | (1) |
| 81 | ±62.5g Range * | $\Delta\text{DFLCT_X62}$ | — | 98 | — | LSB | (1) |
| 82 | ±125g Range * | $\Delta\text{DFLCT_X125}$ | — | 49 | — | LSB | (1) |
| 83 | ±187g Range * | $\Delta\text{DFLCT_X187}$ | — | 82 | — | LSB | (1) |
| 84 | ±312g Range * | $\Delta\text{DFLCT_X312}$ | — | 49 | — | LSB | (1) |
| 85 | Self-test deflection range, $T_A = 25^\circ\text{C}$ | ΔDFLCT | -10 | — | +10 | % | (1) |
| 86 | Self-test deflection range, $T_L \leq T_A \leq T_H$ | ΔDFLCT | -20 | — | +20 | % | (1) |

2.7 Dynamic Electrical Characteristics - DSI

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|---|-------------------------|---------------|-------------------|-------------------|-------------|-----|
| 87 | Reset Recovery (See Figure 20) POR negated to 1st DSI Command (Initialization Command) | t_{DSI_INIT} | — | $400 / f_{OSC}$ | — | s | (7) |
| 88 | POR negated to Acceleration Data Valid (Including LPF Init) | t_{DSP_INIT} | — | — | $10000 / f_{OSC}$ | s | (7) |
| 89 | DSI Clear Command to 1st DSI Command (Initialization Command) | t_{DSI_INIT} | — | $400 / f_{OSC}$ | — | s | (7) |
| 90 | DSI Clear Command to Acceleration Data Valid (Including LPF Init) | t_{DSP_INIT} | — | — | $10000 / f_{OSC}$ | s | (7) |
| 91 | HCAP Under-Voltage Reset Delay (See Figure 5) $V_{HCAP} < V_{PORHCAP_f}$ to POR assertion | t_{HCAP_POR} | — | $880 / f_{OSC}$ | — | s | (7) |
| 92 | V_{REG} Under-Voltage Reset Delay (See Figure 6) $V_{REG} < V_{PORVREG_f}$ to POR assertion | t_{VREG_POR} | — | — | 5 | μ s | (3) |
| 93 | V_{REGA} Under-Voltage Reset Delay (See Figure 7) $V_{REGA} < V_{PORVREGA_f}$ to POR assertion | t_{VREGA_POR} | — | — | 5 | μ s | (3) |
| 94 | V_{REG} , V_{REGA} Capacitor Monitor POR to first Capacitor Test Disconnect | $t_{POR_CAPTEST}$ | — | $12000 / f_{OSC}$ | — | s | (7) |
| 95 | Disconnect Time () | $t_{CAPTEST_TIME}$ | — | $6 / f_{OSC}$ | — | s | (7) |
| 96 | Disconnect Rate () | $t_{CAPTEST_RATE}$ | — | $256 / f_{OSC}$ | — | s | (7) |
| 97 | Initialization to Bus Switch Closing | t_{BS} | 89 | — | 138 | μ s | (7) |
| 98 | BUSOUT Discharge Resistance Activation Time | $t_{BUSOUT_Discharge}$ | 9.5 | 10 | 10.5 | μ s | (3) |
| 99 | Communication Data Rate | D_{RATE} | 100 | — | 200 | kbps | (7) |
| 100 | Loss of Signal Reset Time Maximum time below frame threshold | t_{TO} | 2.00 | — | 4.00 | ms | (7) |
| 101 | BUSIN Response Current Slew Rate 1.0 mA to 9.0 mA, 9.0 to 1.0 mA | t_{ITR} | 0.33 | — | 10.0 | mA/ μ s | (3) |
| 102 | BUSIN Timing to Response Current BUSIN Negative Voltage Transition = 3.0V to $I_{RSP} = 7.0$ mA rise | t_{RSP_R} | — | — | 2.50 | μ s | (7) |
| 103 | BUSIN Negative Voltage Transition = 3.0V to $I_{RSP} = 5.0$ mA fall | t_{RSP_F} | — | — | 2.50 | μ s | (7) |
| 104 | DSI BUSIN Signal Duty Cycle Logic '0' | D_{CL} | 10 | 33 | 40 | % | (7) |
| 105 | Logic '1' | D_{CH} | 60 | 67 | 90 | % | (7) |
| 106 | Inter-frame Separation Time (See Figure 8) Following Read Write NVM Command | t_{IFS} | 2 | — | — | ms | (7) |
| 107 | Following Initialization, BS = 1 | t_{IFS} | 200 | — | — | μ s | (7) |
| 108 | Following Initialization, BS = 0 | t_{IFS} | 20 | — | — | μ s | (7) |
| 109 | Following other DSI bus commands | t_{IFS} | 20 | — | — | μ s | (7) |
| 110 | DSI Data Latency | t_{LAT_DSI} | $4 / f_{OSC}$ | — | $5 / f_{OSC}$ | s | (7) |
| 111 | Bus Switch Open Time Reset Asserted to $I_{SW_LEAK} \leq 20$ μ A | t_{BSOPEN} | — | — | 500 | μ s | (3) |
| 112 | OTP Program Timing Time to program one OTP bit | t_{PROG_BIT} | 64 | — | 256 | μ s | (7) |
| 113 | Self-Test Response Time Self-Test Activation time (EOF _{Slave} to 90% Δ DFLCT _{xxx} , 180 Hz LPF) | $t_{ST_ACT_180}$ | 2.00 | — | 5.00 | ms | (7) |
| 114 | Self-Test Deactivation time (EOF _{Slave} to 10% Δ DFLCT _{xxx} , 180 Hz LPF) | $t_{ST_DEACT_180}$ | 2.00 | — | 5.00 | ms | (7) |
| 115 | Self-Test Activation time (EOF _{Slave} to 90% Δ DFLCT _{xxx} , 400 Hz LPF) | $t_{ST_ACT_400}$ | 1.00 | — | 2.50 | ms | (7) |
| 116 | Self-Test Deactivation time (EOF _{Slave} to 10% Δ DFLCT _{xxx} , 400 Hz LPF) | $t_{ST_DEACT_400}$ | 1.00 | — | 2.50 | ms | (7) |
| 117 | Self-Test Activation time (EOF _{Slave} to 90% Δ DFLCT _{xxx} , 800 Hz LPF) | $t_{ST_ACT_800}$ | 0.50 | — | 1.75 | ms | (7) |
| 118 | Self-Test Deactivation time (EOF _{Slave} to 10% Δ DFLCT _{xxx} , 800 Hz LPF) | $t_{ST_DEACT_800}$ | 0.50 | — | 1.75 | ms | (7) |
| 119 | Error Detection Response Time Mirror Register CRC Error to Status Flag (S) set (Factory or User Array) | t_{CRC_Err} | — | $75 / f_{OSC}$ | — | s | (7) |

2.8 Dynamic Electrical Characteristics - Signal Chain

$V_L \leq (V_{CC} - V_{SS}) \leq V_H$, $T_L \leq T_A \leq T_H$, $\Delta T \leq 25$ K/min, unless otherwise specified.

| # | Characteristic | Symbol | Min | Typ | Max | Units | |
|-----|--|----------------------------|----------------|-----|----------------|---------|-----|
| 120 | Internal Oscillator Frequency * | f_{OSC} | 3.80 | 4 | 4.20 | MHz | (1) |
| 121 | Data Interpolation Latency | t_{LAT_INTERP} | $64 / f_{OSC}$ | — | $65 / f_{OSC}$ | s | (7) |
| 122 | DSP Low-Pass Filter | | | | | | |
| | Cutoff frequency LPF0 (referenced to 0 Hz) | f_{C_LPF0} | 171 | 180 | 189 | Hz | (7) |
| 123 | Filter Order LPF0 | O_{LPF0} | — | 2 | — | 1 | (7) |
| 124 | Cutoff frequency LPF1 (referenced to 0 Hz) | f_{C_LPF1} | 380 | 400 | 420 | Hz | (7) |
| 125 | Filter Order LPF1 | O_{LPF1} | — | 4 | — | 1 | (7) |
| 126 | Cutoff frequency LPF2 (referenced to 0 Hz) | f_{C_LPF2} | 760 | 800 | 840 | Hz | (7) |
| 127 | Filter Order LPF2 | O_{LPF2} | — | 4 | — | 1 | (7) |
| 128 | Sensing Element Rolloff Frequency (-3db) | | | | | | |
| | $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$ | $f_{gcell_3dB_xlo}$ | 938 | — | 2592 | Hz | (9) |
| 129 | $\pm 187g, \pm 312g$ | $f_{gcell_3dB_xhi}$ | 3952 | — | 14370 | Hz | (9) |
| 130 | Sensing Element Natural Frequency | | | | | | |
| | $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$ | f_{gcell_xlo} | 12651 | — | 13871 | Hz | (9) |
| 131 | $\pm 187g, \pm 312g$ | f_{gcell_xhii} | 26000 | — | 28700 | Hz | (9) |
| 132 | Sensing Element Damping Ratio | | | | | | |
| | $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$ | ζ_{gcell_xlo} | 2.760 | — | 6.770 | — | (9) |
| 133 | $\pm 187g, \pm 312g$ | ζ_{gcell_xhi} | 1.260 | — | 3.602 | — | (9) |
| 134 | Sensing Element Delay (@100Hz) | | | | | | |
| | $\pm 25g, \pm 50g, \pm 62.5g, \pm 125g$ | $f_{gcell_delay100_xlo}$ | 63 | — | 170 | μs | (9) |
| 135 | $\pm 187g, \pm 312g$ | $f_{gcell_delay100_xhi}$ | 13 | — | 40 | μs | (9) |
| 136 | Package Resonance Frequency | $f_{Package}$ | 100 | — | — | kHz | (9) |

Notes:

- Parameters tested 100% at final test at -40°C, 25°C, and 105°C.
- Parameters tested 100% at probe.
- Verified by characterization.
- * Indicates critical characteristic.
- Verified by qualification testing, not tested in production.
- Parameters verified by pass/fail testing in production.
- Functionality guaranteed by modeling, simulation and/or design verification. Circuit integrity assured through IDDQ and scan testing. Timing is determined by internal system clock frequency.
- Verified by user system level characterization, not tested in production, or at component level.
- Verified by Simulation.
- Measured at final test. Self-test activation occurs under control of the test program.
- Thermal resistance between the die junction and the exposed pad; cold plate is attached to the exposed pad.
- Maximum voltage characterized. Minimum voltage tested 100% at final test. Maximum voltage tested 100% to 24 V at final test.
- N/A.
- Sensitivity, and overload capability specifications will be reduced when 800Hz filter is selected.
- Filter cut-off frequencies are directly dependent upon the internal oscillator frequency.
- Target values. Actual values to be determined during device characterization.

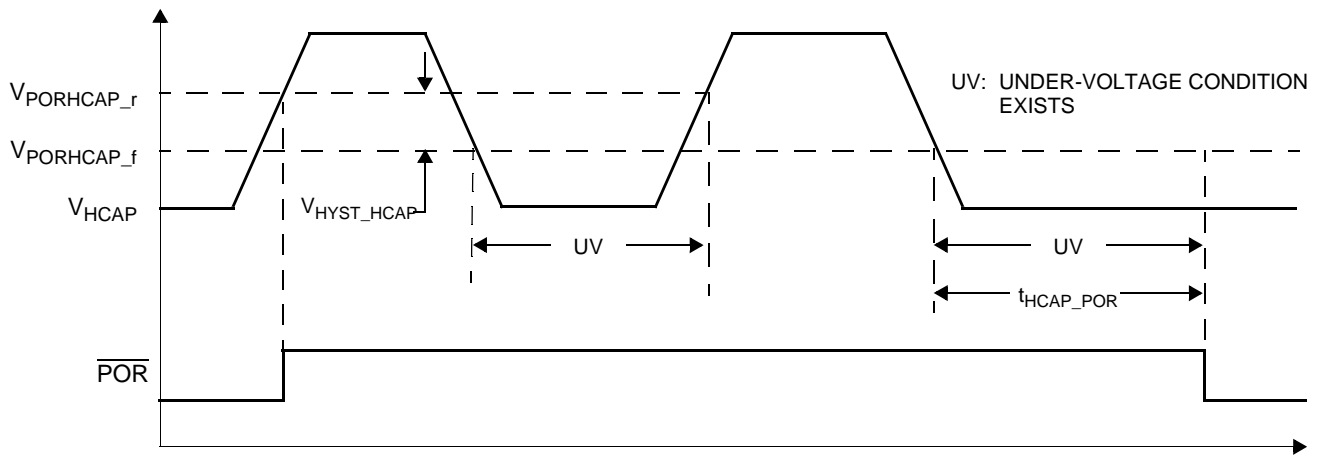


Figure 5. V_{HCAP} Under-Voltage Detection

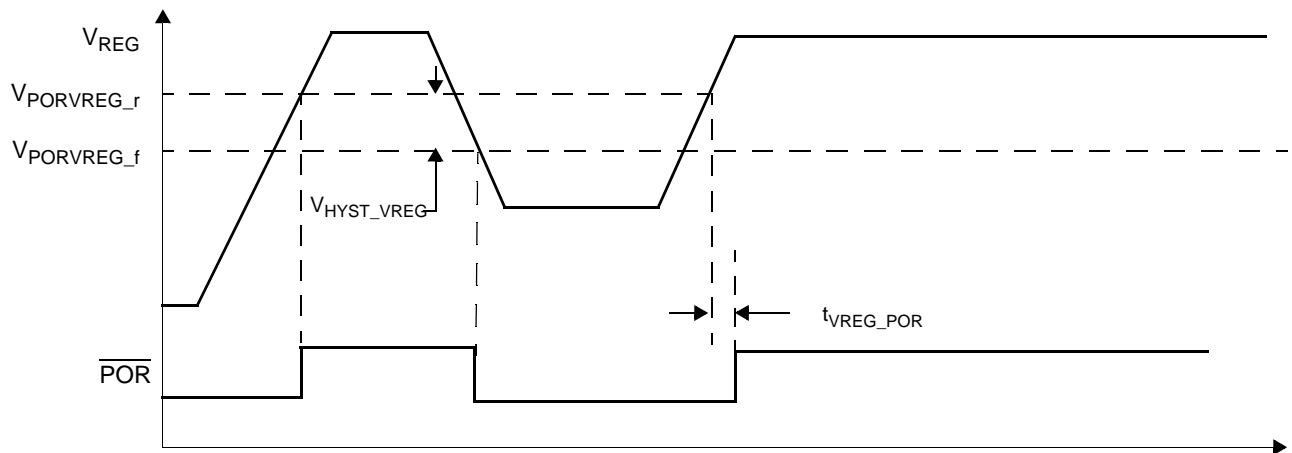


Figure 6. V_{REG} Under-Voltage Detection

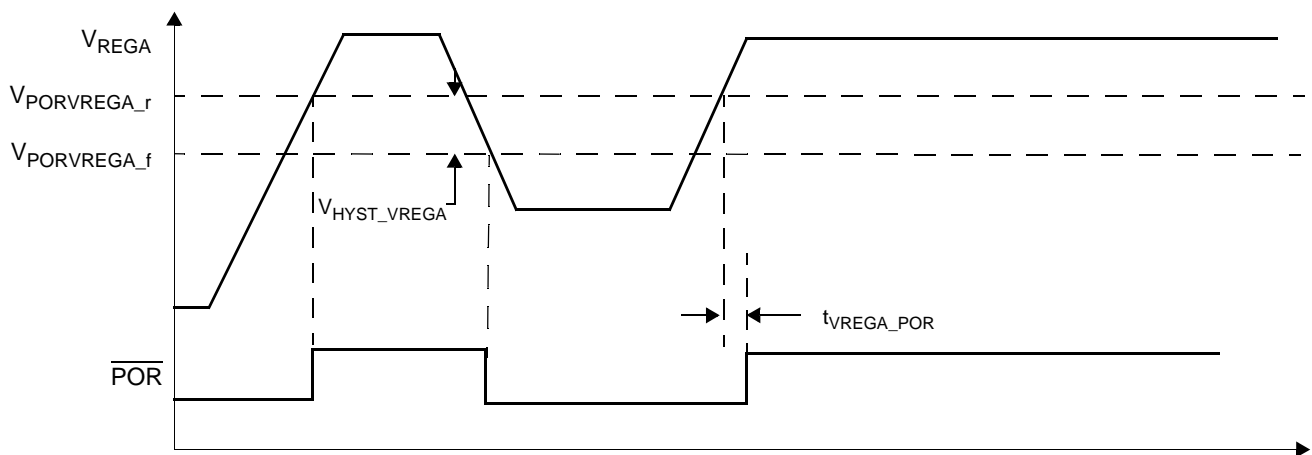


Figure 7. V_{REGA} Under-Voltage Detection

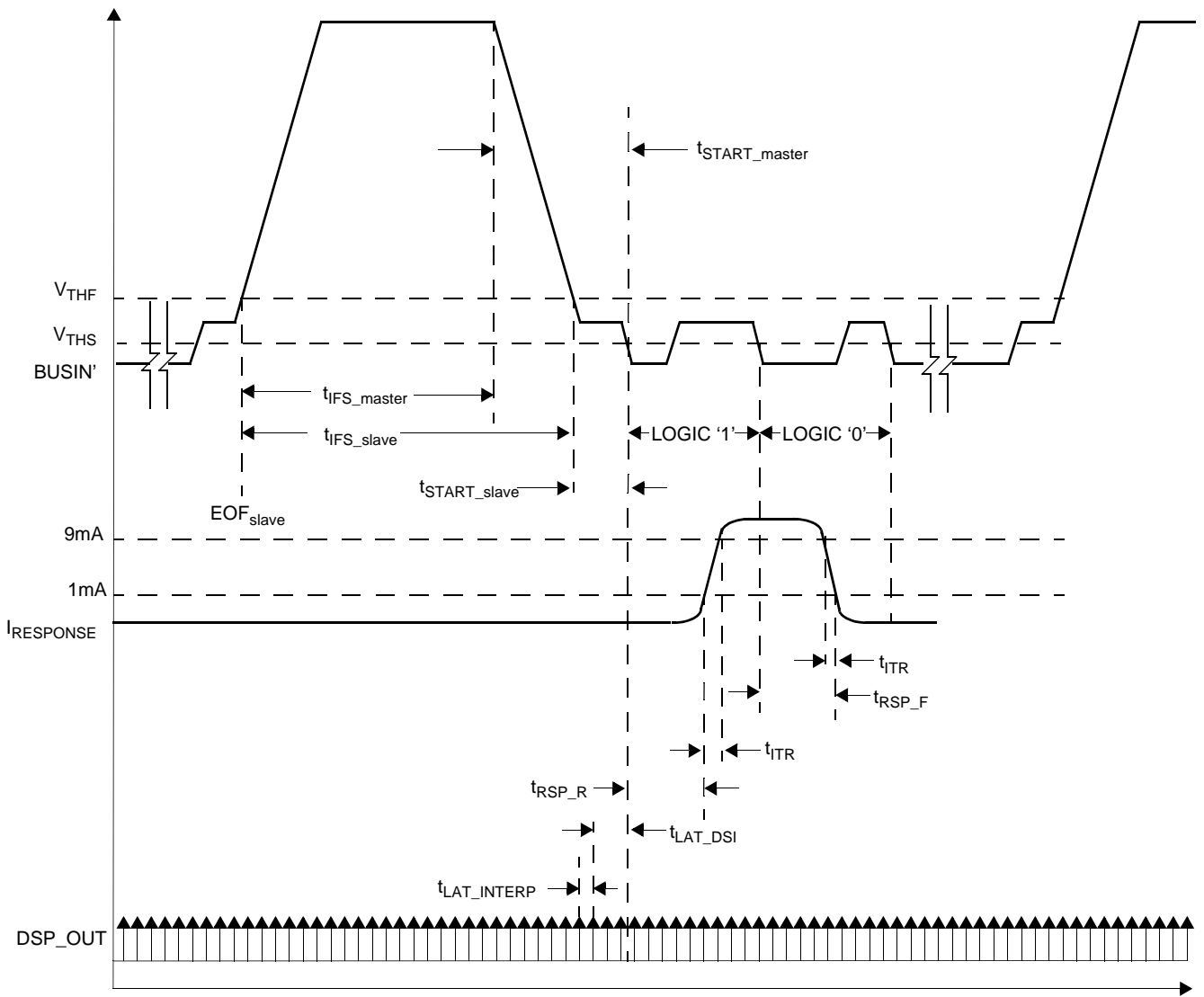


Figure 8. DSI Bus Inter-frame Timing

3 Functional Description

3.1 User Accessible Data Array

A user accessible data array allows for each device to be customized. The array consists of an OTP factory programmable array, an OTP user programmable array, and read only registers for device status. The OTP arrays incorporate independent CRC circuitry for fault detection (reference [Section 3.2](#)). Portions of the factory programmable array are reserved for factory-programmed trim values. The user accessible data is shown in the table below.

Table 2. User Accessible Data

| Byte Addr RA[3:0] | Register | Nibble Addr WA[3:0] | Bit Function | | | | Nibble Addr (WA[3:0]) | Bit Function | | | | Type |
|-------------------|----------|-----------------------|--------------|---------|---------|----------|-----------------------|--------------|----------|-----------|-----------|------|
| | | | 7 | 6 | 5 | 4 | | 3 | 2 | 1 | 0 | |
| \$00 | SN0 | | SN[7] | SN[6] | SN[5] | SN[4] | | SN[3] | SN[2] | SN[1] | SN[0] | F |
| \$01 | SN1 | | SN[15] | SN[14] | SN[13] | SN[12] | | SN[11] | SN[10] | SN[9] | SN[8] | |
| \$02 | SN2 | | SN[23] | SN[22] | SN[21] | SN[20] | | SN[19] | SN[18] | SN[17] | SN[16] | |
| \$03 | SN3 | | SN[31] | SN[30] | SN[29] | SN[28] | | SN[27] | SN[26] | SN[25] | SN[24] | |
| \$04 | TYPE | Reference Table 39 | LPF[1] | LPF[0] | 1 | 0 | Reference Table 39 | RNG[3] | RNG[2] | RNG[1] | RNG[0] | U/F |
| \$05 | DEVCFG | | DEVID | UNUSED | UNUSED | UNUSED | | UNUSED | CRC_U[2] | CRC_U[1] | CRC_U[0] | |
| \$06 | DEVCFG1 | | UD00[5] | UD00[4] | UD00[3] | UD00[2] | | UD00[1] | UD00[0] | AT_OTP[1] | AT_OTP[0] | |
| \$07 | DEVCFG2 | | LOCK_U | UNUSED | PCM | RESERVED | | ADDR[3] | ADDR[2] | ADDR[1] | ADDR[0] | |
| \$08 | UD01 | | UD01[7] | UD01[6] | UD01[5] | UD01[4] | | UD01[3] | UD01[2] | UD01[1] | UD01[0] | |
| \$09 | UD02 | | UD02[7] | UD02[6] | UD02[5] | UD02[4] | | UD02[3] | UD02[2] | UD02[1] | UD02[0] | |
| \$0A | UD03 | | UD03[7] | UD03[6] | UD03[5] | UD03[4] | | UD03[3] | UD03[2] | UD03[1] | UD03[0] | |
| \$0B | UD04 | | UD04[7] | UD04[6] | UD04[5] | UD04[4] | | UD04[3] | UD04[2] | UD04[1] | UD04[0] | |
| \$0C | UD05 | | UD05[7] | UD05[6] | UD05[5] | UD05[4] | | UD05[3] | UD05[2] | UD05[1] | UD05[0] | |
| \$0D | UD06 | | UD06[7] | UD06[6] | UD06[5] | UD06[4] | | UD06[3] | UD06[2] | UD06[1] | UD06[0] | |
| \$0E | UD07 | | UD07[7] | UD07[6] | UD07[5] | UD07[4] | | UD07[3] | UD07[2] | UD07[1] | UD07[0] | |
| \$0F | UD08 | | UD08[7] | UD08[6] | UD08[5] | UD08[4] | | UD08[3] | UD08[2] | UD08[1] | UD08[0] | |

Type codes

F: Freescale programmed OTP location U/F: User and/or Freescale programmed OTP location

R: Read-only register U: User Programmed OTP location

Note: Unused and Unprogrammed Spare bits always read '0'.

3.1.1 Device Serial Number Registers

A unique serial number is programmed into the serial number registers of each device during manufacturing. The serial number is composed of the following information:

| Bit Range | Content |
|-----------|---------------|
| SN[12:0] | Serial Number |
| SN[31:13] | Lot Number |

Serial numbers begin at 1 for all produced devices in each lot, and are sequentially assigned. Lot numbers begin at 1 and are sequentially assigned. No lot will contain more devices than can be uniquely identified by the 13-bit serial number. Depending on lot size and quantities, all possible lot numbers and serial numbers may not be assigned.

The serial number registers are included in the factory programmed OTP CRC verification. Reference [Section 3.2.1](#) for details regarding the CRC verification. Beyond this, the contents of the serial number registers have no impact on device operation or performance, and are only used for traceability purposes.

3.1.2 Device Type Register (TYPE)

The Device Type Register is an OTP configuration register which contains device configuration information. Bit 5 - Bit 0 are factory programmed and are included in the factory programmed OTP CRC verification. These bits are read only to the user. Bit 7 - Bit 6 are user programmable OTP bits and are included in the user programmable OTP CRC verification.

Table 3. Factory Configuration Register

| Location | | Bit | | | | | | | | | |
|-----------------|----------|------------|--------|--------|---|---|---------|--------|--------|--------|--------|
| RA[3:0] | Register | WA[3:0] | 7 | 6 | 5 | 4 | WA[3:0] | 3 | 2 | 1 | 0 |
| \$04 | TYPE | Bank0 \$08 | LPF[1] | LPF[0] | 1 | 0 | | RNG[3] | RNG[2] | RNG[1] | RNG[0] |
| Factory Default | | | 0 | 0 | 1 | 0 | | 0 | 0 | 0 | 0 |

3.1.2.1 Low-Pass Filter Selection Bits (LPF[1:0]) (TYPE[7:6])

The Low Pass Filter selection bit selects between one of three low pass filter options. These bits can be factory or user programmed.

| LPF[1] | LPF[0] | Low Pass Filter Selected |
|--------|--------|--------------------------|
| 0 | 0 | 400 Hz, 4-Pole |
| 0 | 1 | Not Enabled ¹ |
| 1 | 0 | 180 Hz, 2-Pole |
| 1 | 1 | 800 Hz, 4-Pole |

¹This filter option is not implemented. LPF[1:0] must not be set to this value to guarantee proper operation and performance.

3.1.2.2 Range Selection Bits (RNG[3:0]) (TYPE[3:0])

The Range Selection Bits indicate the full-scale range of the device, as shown below. These bits are factory programmed.

| RNG[3] | RNG[2] | RNG[1] | RNG[0] | Full-Scale Range | g-Cell Design |
|--------|--------|--------|--------|------------------|---------------|
| 0 | 0 | 0 | 0 | N/A | N/A |
| 0 | 0 | 0 | 1 | 25g | Medium-g |
| 0 | 0 | 1 | 0 | 50g | Medium-g |
| 0 | 0 | 1 | 1 | 62g | Medium-g |
| 0 | 1 | 0 | 0 | 125g | Medium-g |
| 0 | 1 | 0 | 1 | 187g | High-g |
| 0 | 1 | 1 | 0 | 312g | High-g |
| 0 | 1 | 1 | 1 | N/A | N/A |
| 1 | 0 | 0 | 0 | Reserved | N/A |
| 1 | 0 | 0 | 1 | | |
| 1 | 0 | 1 | 0 | | |
| 1 | 0 | 1 | 1 | | |
| 1 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 1 | | |

3.1.3 Device Configuration Register (DEVCFG)

The Device configuration register is a user programmable OTP register which contains device configuration information. This register is included in the user register CRC check. Refer to [Section 3.2.2](#) for details regarding the CRC for the user programmable OTP array.

Table 4. Device Control Register

| Location | | Bit | | | | | | | | | |
|-----------------|----------|------------|-------|---|---|---|------------|---|----------|----------|----------|
| RA[3:0] | Register | WA[3:0] | 7 | 6 | 5 | 4 | WA[3:0] | 3 | 2 | 1 | 0 |
| \$05 | DEVCFG | Bank0 \$0A | DEVID | 0 | 0 | 0 | Bank0 \$09 | 0 | CRC_U[2] | CRC_U[1] | CRC_U[0] |
| Factory Default | | | 1 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |

3.1.3.1 Device ID Bit (DEVCFG[7])

The Device ID Bit is a user programmable bit which allows the user to select between 2 device IDs. The Device ID is transmitted in response to the Request ID DSI command. Reference [Section 4.2.1.5](#) for more information regarding the Request ID DSI command. This bit can be factory or user programmed.

| DEVID | Device ID |
|-------|-----------|
| 0 | '00110' |
| 1 | '00100' |

3.1.3.2 User Configuration CRC (CRC_U[2:0], DEVCFG[2:0])

The User Configuration CRC bits contain the 3-bit CRC used for verification of the user programmable OTP array. Reference [Section 3.2.2](#) for details regarding the CRC for the user programmable OTP array. These bits can be factory or user programmed.

3.1.4 Device Configuration Register 1 (DEVCFG1)

The Device configuration register is a user programmable OTP register which contains device configuration information. This register is included in the user register CRC check. Refer to [Section 3.2.2](#) for details.

Table 5. Device Control Register 1

| Location | | Bit | | | | | | | | | |
|-----------------|----------|------------|---------|---------|---------|---------|------------|---------|---------|-----------|-----------|
| RA[3:0] | Register | WA[3:0] | 7 | 6 | 5 | 4 | WA[3:0] | 3 | 2 | 1 | 0 |
| \$06 | DEVCFG1 | Bank2 \$06 | UD00[5] | UD00[4] | UD00[3] | UD00[2] | Bank1 \$06 | UD00[1] | UD00[0] | AT_OTP[1] | AT_OTP[0] |
| Factory Default | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |

3.1.4.1 User Specific Data 00 Bits (UD00[5:0], DEVCFG1[7:2])

The User Specific Data bits have no impact on the device function or performance. The bits can be programmed with user or assembly specific information. These bits can be factory or user programmed.

3.1.4.2 Attribute Bits (AT_OTP[1:0], DEVCFG1[1:0])

The Attribute Bits are user defined bits which are transmitted in response to the Request Status, Disable Self-Test Stimulus or Enable Self-Test Stimulus DSI commands. The transmitted values are qualified by the LOCK_U bit as shown in the table below. These bits can be factory or user programmed.

| LOCK_U | DEVCFG1 Values | | DSI Transmitted Values | |
|--------|----------------|-----------|------------------------|-------|
| | AT_OTP[1] | AT_OTP[0] | AT[1] | AT[0] |
| 0 | X | X | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| | 0 | 1 | 0 | 1 |
| | 1 | 0 | 1 | 0 |
| | 1 | 1 | 1 | 1 |

3.1.5 Device Configuration 2 Register (DEVCFG2)

Device configuration register 2 is a user programmable OTP register which contains device configuration information. This register is included in the user register CRC check. Refer to [Section 3.2.2](#) for details regarding the CRC for the user programmable OTP array.

Table 6. Device Control Register

| Location | | Bit | | | | | | | | | |
|-----------------|----------|--|--------|--------|-----|----------|-----------|---------|---------|---------|---------|
| RA[3:0] | Register | WA[3:0] | 7 | 6 | 5 | 4 | WA[3:0] | 3 | 2 | 1 | 0 |
| \$07 | DEVCFG2 | Bnk0 \$07 Bnk2 \$07 Bnk3 \$07 Bnk3 \$0F | LOCK_U | UNUSED | PCM | RESERVED | Bnk1 \$07 | ADDR[3] | ADDR[2] | ADDR[1] | ADDR[0] |
| Factory Default | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |

3.1.5.1 User Configuration Lock Bit (LOCK_U, DEVCFG2[7])

The LOCK_U bit is a factory or user programmed OTP bit which inhibits writes to the user configuration array when active. Reference [Section 3.2.2](#) for details regarding the LOCK_U bit and CRC verification.

3.1.5.2 PCM Bit (DEVCFG2[5])

The PCM Bit enables the PCM output pin. When the PCM bit is set, the PCM output pin is active and outputs a Pulse Code Modulated signal proportional to the acceleration response. Reference [Section 3.5.3.6](#) for more information regarding the PCM output. When the PCM output is cleared, the PCM output pin is actively pulled low. This bit can be factory or user programmed.

3.1.5.3 Device Address (ADDR[3:0], DEVCFG2[3:0])

The Device Address bits define the preprogrammed DSI Bus device address. If the Device Address bits are programmed to '0000', there is not preprogrammed address, and the address must be assigned via the Initialization DSI command. Reference [Section 4.2.1.1](#) for more details regarding the Initialization DSI command. These bits can be factory or user programmed.

3.1.6 User Data Registers (UDx)

The User Data Registers are user programmable OTP register which can be programmed with user or assembly specific information. These registers have no impact on the device performance, but are included in the user register CRC check. Refer to [Section 3.2.2](#) for details regarding the user register CRC check. These registers can be factory or user programmed.

| Location | | Bit | | | | | | | | | |
|-----------------|----------|-----------|---------|---------|---------|---------|-----------|---------|---------|---------|---------|
| RA[3:0] | Register | WA[3:0] | 7 | 6 | 5 | 4 | WA[3:0] | 3 | 2 | 1 | 0 |
| \$08 | UD01 | Bnk2 \$08 | UD01[7] | UD01[6] | UD01[5] | UD01[4] | Bnk1 \$08 | UD01[3] | UD01[2] | UD01[1] | UD01[0] |
| \$09 | UD02 | Bnk2 \$09 | UD02[7] | UD02[6] | UD02[5] | UD02[4] | Bnk1 \$09 | UD02[3] | UD02[2] | UD02[1] | UD02[0] |
| \$0A | UD03 | Bnk2 \$0A | UD03[7] | UD03[6] | UD03[5] | UD03[4] | Bnk1 \$0A | UD03[3] | UD03[2] | UD03[1] | UD03[0] |
| \$0B | UD04 | Bnk2 \$0B | UD04[7] | UD04[6] | UD04[5] | UD04[4] | Bnk1 \$0B | UD04[3] | UD04[2] | UD04[1] | UD04[0] |
| \$0C | UD05 | Bnk2 \$0C | UD05[7] | UD05[6] | UD05[5] | UD05[4] | Bnk1 \$0C | UD05[3] | UD05[2] | UD05[1] | UD05[0] |
| \$0D | UD06 | Bnk2 \$0D | UD06[7] | UD06[6] | UD06[5] | UD06[4] | Bnk1 \$0D | UD06[3] | UD06[2] | UD06[1] | UD06[0] |
| \$0E | UD07 | Bnk2 \$0E | UD07[7] | UD07[6] | UD07[5] | UD07[4] | Bnk1 \$0E | UD07[3] | UD07[2] | UD07[1] | UD07[0] |
| \$0F | UD08 | Bnk2 \$0F | UD08[7] | UD08[6] | UD08[5] | UD08[4] | Bnk1 \$0F | UD08[3] | UD08[2] | UD08[1] | UD08[0] |
| Factory Default | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |

3.2 OTP Array Lock and CRC Verification

3.2.1 Factory Programmed OTP Array Lock and CRC Verification

The Factory programmed OTP array is verified for errors with a 3-bit CRC. The CRC verification is enabled only when the Factory programmed OTP array is locked and the lock is active. The lock is active only after an automatic OTP readout in which the internal lock bit is read as '1'. Automatic OTP readouts occur only after POR or a DSI Clear Command is received.

| Factory Lock Bit Value in Fuse Array | Lock Bit Value in Mirror Register After Automatic Readout | Lock Bit Active? | CRC Verification Enabled? |
|--------------------------------------|---|------------------|---------------------------|
| 0 | N/A | NO | NO |
| 1 | 0 | NO | NO |
| 1 | 1 | YES | YES |

The Factory programmed OTP array is locked by Freescale and will always be active after POR. The CRC is continuously calculated on the factory programmed OTP array, which includes the registers listed below:

| Register Name | Register Addresses | Included in Factory CRC? |
|--|-----------------------|--------------------------|
| Serial Number Registers | SN0, SN1, SN2, SN3 | Yes |
| Type Register | TYPE[5:0] | Yes |
| Factory Programmable Device Configuration Bits | Internal Register Map | Yes |
| Factory OTP Array CRC | CRC_F[2:0] | No |
| Factory OTP Array Lock Bit | LOCK_F | No |

Bits are fed in from right to left (LSB first), and top to bottom (lower addresses first) in the register map. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'. The calculated CRC is compared against the CRC_F[2:0] bits. If a CRC mismatch is detected, an internal data error is set and the device responds to DSI messages as specified in [Section 4.3](#). The CRC verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values.

3.2.2 User Programmable OTP Array Lock and CRC Verification

The User Programmable OTP array is independently verified for errors with a 3-bit CRC. The CRC verification is enabled only when the User Programmable OTP array is locked and the lock is active. The lock is active only after an automatic OTP readout in which the LOCK_U bit is read as '1'. Automatic OTP readouts occur only after POR or a DSI Clear Command is received.

| Factory Lock Bit Value in Fuse Array | Lock Bit Value in Mirror Register After Automatic Readout | Lock Bit Active? | CRC Verification Enabled? |
|--------------------------------------|---|------------------|---------------------------|
| 0 | N/A | NO | NO |
| 1 | 0 | NO | NO |
| 1 | 1 | YES | YES |

Once the LOCK_U bit is active, the CRC is continuously calculated on the user programmable OTP Array, which includes the registers listed below:

| Register Name | Register Addresses | Included in User CRC? |
|--------------------------------------|---------------------------|-----------------------|
| Type Register | TYPE[7:6] | Yes |
| Device ID Bit | DEVCFG[7]: DEVID | Yes |
| User Data Register 0 | DEVCFG1[7:2]: UD00[5:0] | Yes |
| Attribute Bits | DEVCFG1[1:0]: AT_OTP[1:0] | Yes |
| PCM Bit | DEVCFG2[5]: PCM | Yes |
| RESERVED Bit | DEVCFG2[4] | Yes |
| Device Address | DEVCFG2[3:0]: ADDR[3:0] | Yes |
| User Data Registers 1 - 8 | UD01 - UD08 | Yes |
| User Programmable OTP Array CRC | DEVCFG2[2:0]: CRC_U[2:0] | No |
| User Programmable OTP Array Lock Bit | DEVCFG2[7]: LOCK_U | No |

Bits are fed in from right to left (LSB first), and top to bottom (lower addresses first) in the register map. The CRC verification uses a generator polynomial of $g(x) = X^3 + X + 1$, with a seed value = '111'. The calculated CRC is compared against the user programmed CRC, CRC_U[2:0], which is also included in the user programmable array. If a CRC mismatch is detected, an internal data error is set, and the device responds to DSI messages as specified in [Section 4.3](#). The CRC verification is completed on the memory registers which hold a copy of the fuse array values, not the fuse array values. Writes to the User Programmable OTP array using the Write NVM Command will update the mirror registers and result in a change to the CRC calculation regardless of the state of the LOCK_U bit. A CRC mismatch will only be detected if the LOCK_U bit is active.

3.3 Voltage Regulators

The device derives its internal supply voltage from the HCAP supply voltage. The device includes separate internal voltage regulators for the analog (V_{REGA}) and digital circuitry (V_{REG}). External filter capacitors are required, as shown in Figure 1.

The voltage regulator module includes voltage monitoring circuitry which holds the device in reset following power-on until the HCAP and internal voltages have stabilized sufficiently for proper operation. The voltage monitor asserts internal reset when the HCAP supply or internally regulated voltages fall below predetermined levels. A reference generator provides a stable voltage which is used by the $\Sigma\Delta$ converter.

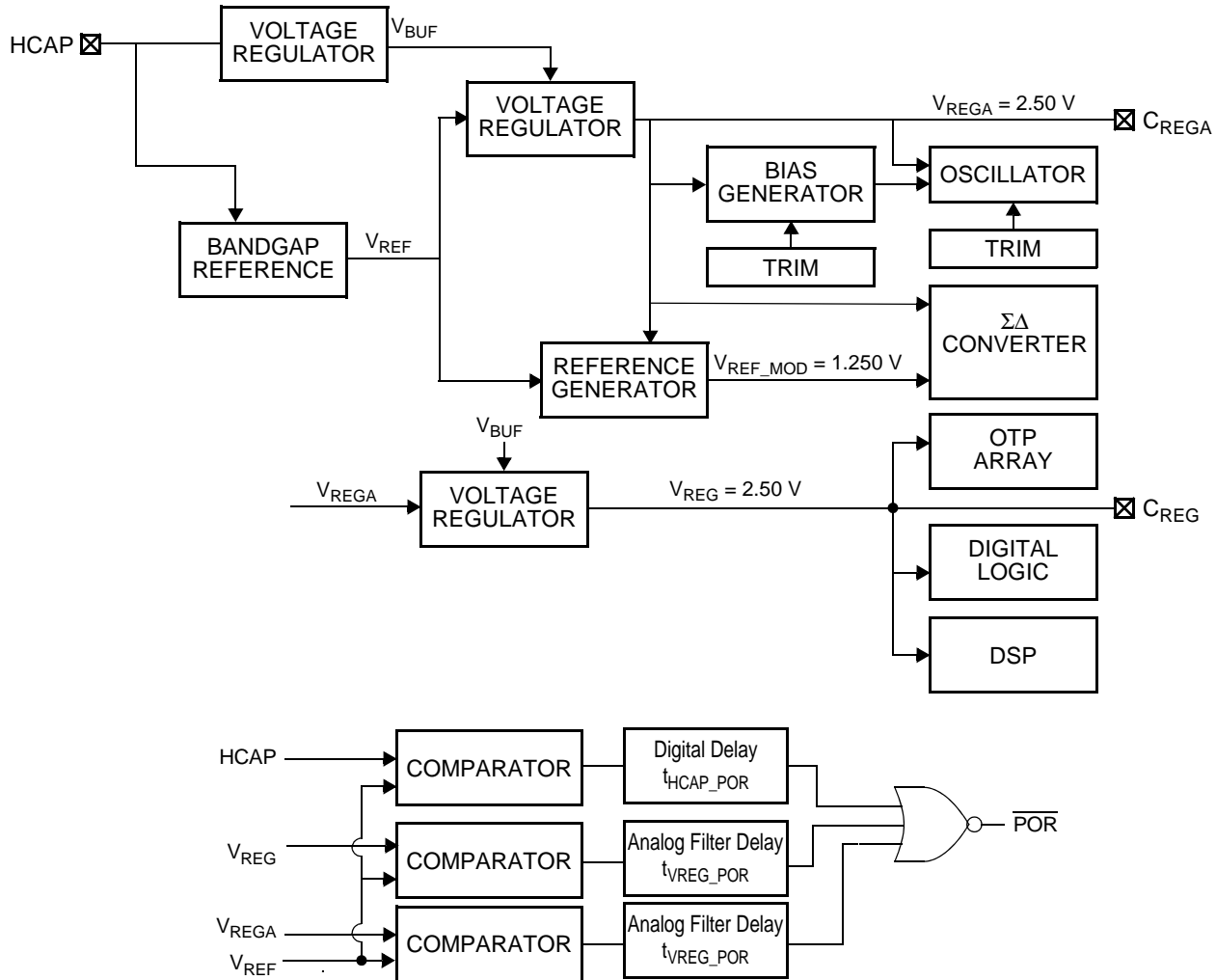


Figure 9. Voltage Regulation and Monitoring

3.3.1 C_{REG} and C_{REGA} Regulator Capacitor

The internal regulator requires an external capacitor between the C_{REG} pin and V_{SS} pin, and the C_{REGA} pin and V_{SSA} pin for stability. Figure 1 shows the recommended types and values for each of these capacitors.

3.3.2 V_{HCAP} Voltage Monitor

The device includes a circuit to monitor the voltage on the HCAP pin. If the voltage falls below the specified threshold in Section 2, the device will be reset within the reset delay time (t_{HCAP_POR}) specified in Section 2.7.

3.3.3 V_{REG} and V_{REGA} Under-Voltage Monitor

The device includes a circuit to monitor the internally regulated voltages (V_{REG} and V_{REGA}). If either of the internal regulator voltages fall below the specified thresholds in Section 2, the device will be reset within the reset delay time (t_{VREG_POR} , t_{VREGA_POR}) specified in Section 2.7.

3.3.4 V_{REG} and V_{REGA} Capacitance Monitor

A monitor circuit is incorporated to ensure predictable operation if the connection to the external C_{REG} or C_{REGA} capacitor becomes open. At a continuous rate specified in Section 2.7 ($t_{CAPTEST_RATE}$), both regulators are simultaneously disabled for a short duration ($t_{CAPTEST_TIME}$). If either of the external capacitors are not present, the associated regulator voltage will fall below the internal reset threshold, forcing a device reset.

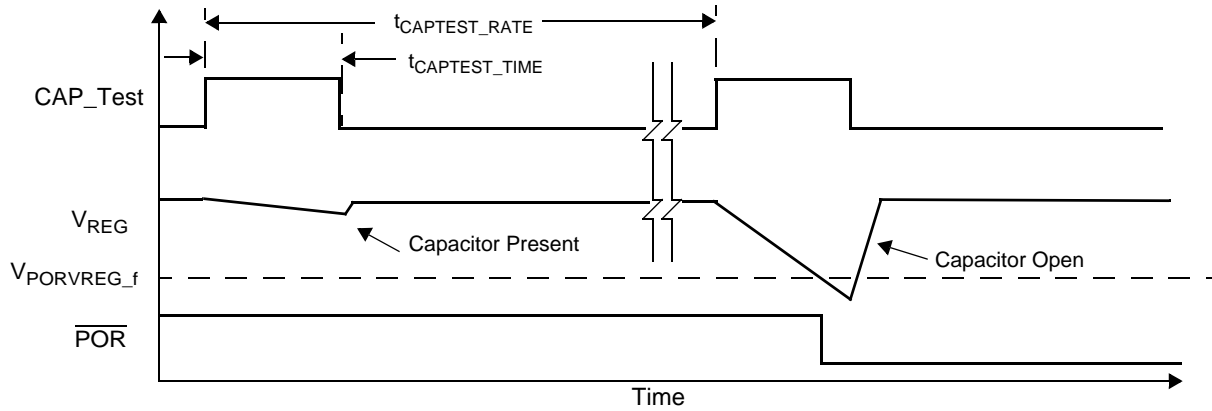


Figure 10. V_{REG} Capacitor Monitor

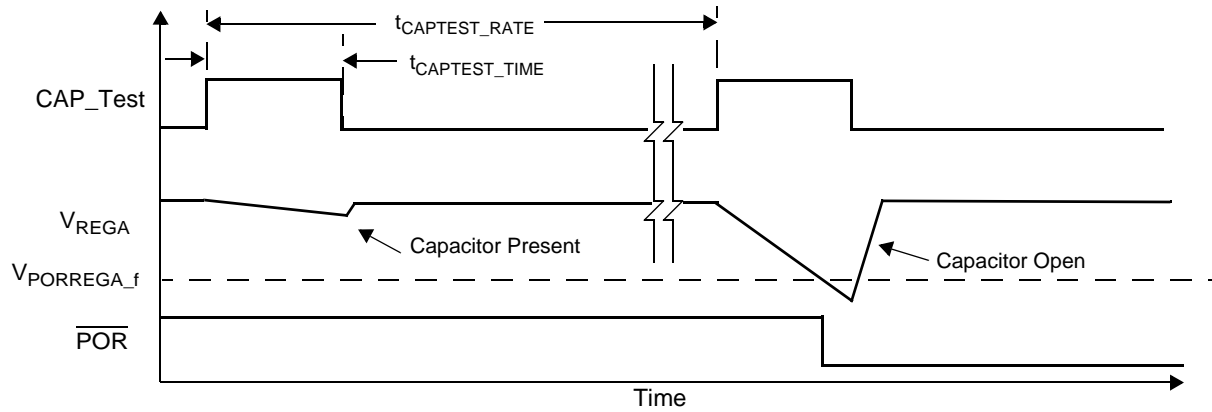


Figure 11. V_{REGA} Capacitor Monitor

3.4 Internal Oscillator

The device includes a factory trimmed oscillator as specified in Section 2.8.

3.5 Acceleration Signal Path

3.5.1 Transducer

The device transducer is an overdamped mass-spring-damper system described by the following transfer function:

$$H(s) = \frac{\omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}$$

where:

ξ = Damping Ratio

ω_n = Natural Frequency = $2 \cdot \pi \cdot f_n$

Reference [Section 2.8](#) for transducer parameters.

3.5.2 $\Sigma\Delta$ Converter

The sigma delta converter provides the interface between the g-cell and the DSP block. The output of the $\Sigma\Delta$ converter is a data stream at a nominal frequency of 1 MHz.

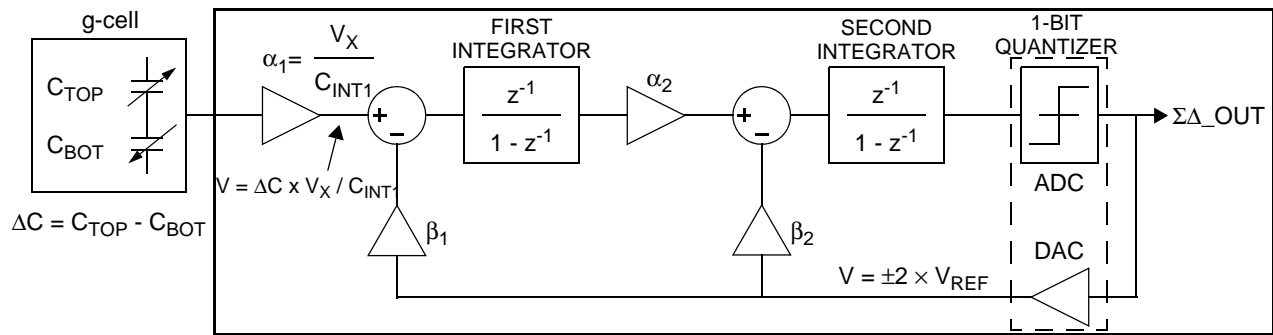


Figure 12. $\Sigma\Delta$ Converter Block Diagram

3.5.3 Digital Signal Processing Block

A digital signal processing (DSP) block is used to perform signal filtering and compensation operations. A diagram illustrating the signal processing flow within the DSP block is shown in [Figure 13](#).

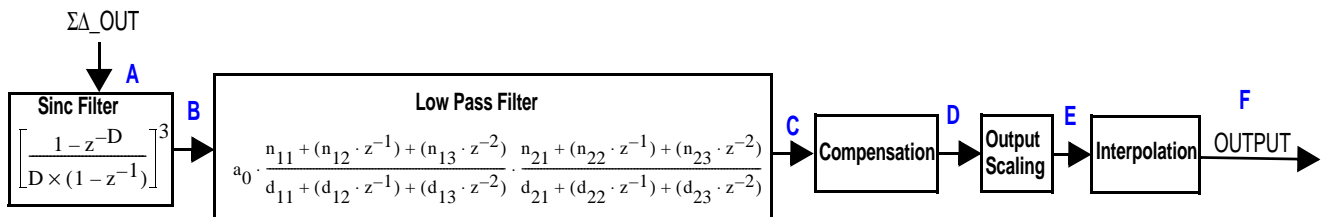


Figure 13. Signal Chain Diagram

Table 7. Signal Chain Characteristics

| | Description | Sample Time (μs) | Data Width (Bits) | Over Range (Bits) | Signal Width (Bits) | Signal Noise (Bits) | Signal Margin (Bits) | Typical Block Latency | Reference |
|---|-----------------------|------------------|-------------------|-------------------|---------------------|---------------------|----------------------|-----------------------|---------------------------------|
| A | $\Sigma\Delta$ | 1 | 1 | | 1 | | | 112/f _{osc} | Section 3.5.2 |
| B | SINC Filter | 16 | 20 | | 12 | 4 | | | Section 3.5.3.1 |
| C | Low Pass Filter | 16 | 26 | 1 | 12 | 4 | 9 | 24/f _{osc} | Section 3.5.3.2 |
| D | Compensation | 16 | 26 | 4 | 10 | 3 | 9 | | Section 3.5.3.3 |
| E | DSP Sampling | 16 | | | 10 | | | 4/f _{osc} | Section 3.5.3.5 |
| | 10-Bit Output Scaling | | | | | | | | |
| F | Interpolation | 1 | | | 10 | | | 64/f _{osc} | Section 3.5.3.5 |

3.5.3.1 Decimation Sinc Filter

The serial data stream produced by the $\Sigma\Delta$ converters is decimated and converted to parallel values by a 3rd order 16:1 sinc filter with a decimation factor of 16.

$$H(z) = \left[\frac{1 - z^{-16}}{16 \times (1 - z^{-1})} \right]^3$$

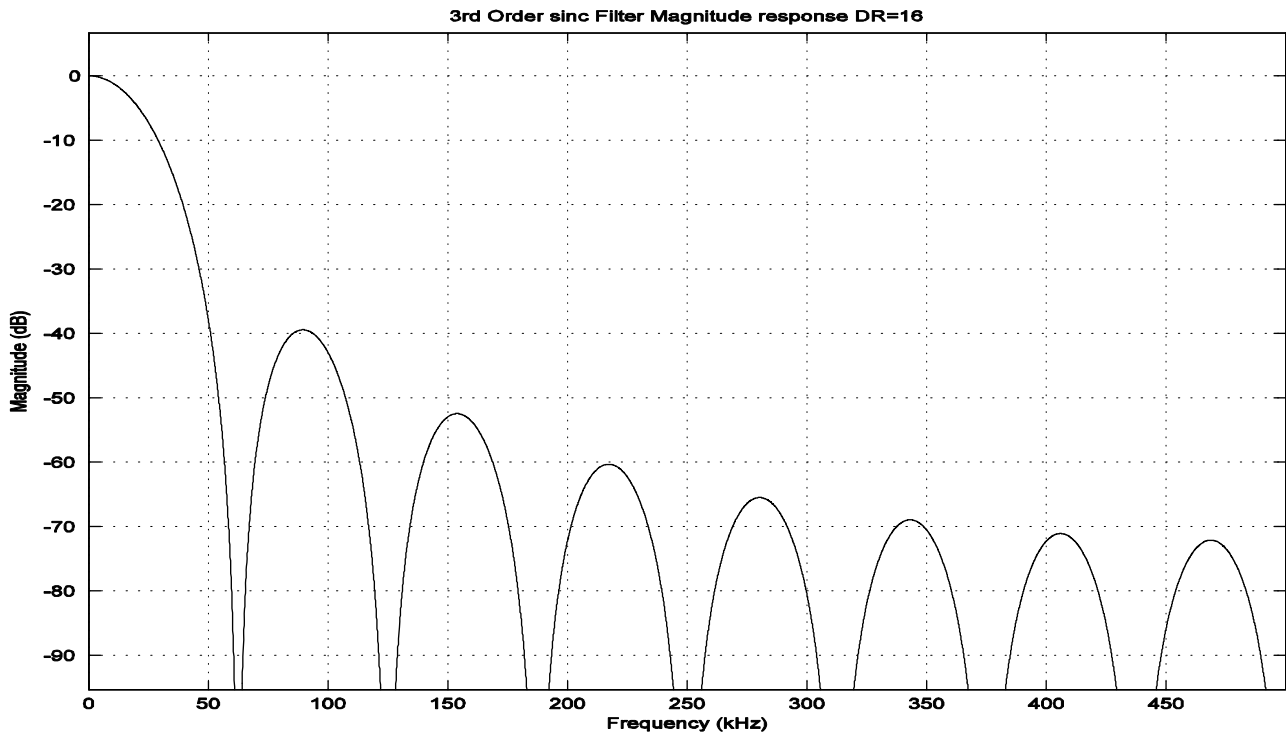


Figure 14. Sinc Filter Response, $t_S = 16 \mu s$

3.5.3.2 Low Pass Filter

Data from the Sinc filter is processed by an infinite impulse response (IIR) low pass filter.

$$H(z) = a_0 \cdot \frac{(n_{11} \cdot z^0) + (n_{12} \cdot z^{-1}) + (n_{13} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{12} \cdot z^{-1}) + (d_{13} \cdot z^{-2})} \cdot \frac{(n_{21} \cdot z^0) + (n_{22} \cdot z^{-1}) + (n_{23} \cdot z^{-2})}{(d_{11} \cdot z^0) + (d_{22} \cdot z^{-1}) + (d_{23} \cdot z^{-2})}$$

The device provides the option for one of three low-pass filters. The filter is selected with the LPF[1:0] bits in the TYPE register. The filter selection options are listed in [Section 3.1.2.1](#), [Table 8](#). Response parameters for the low-pass filter are specified in [Section 2.8](#). Filter characteristics are illustrated in the figures below.

Table 8. Low Pass Filter Coefficients

| Description | Filter Coefficients | | | | Group Delay |
|-------------|---------------------|-------------------|-----------------|--------------------|-----------------------|
| 180 Hz LPF | a ₀ | 0.000534069200512 | | | 4608/f _{osc} |
| | n ₁₁ | 0.25 | d ₁₁ | 1 | |
| | n ₁₂ | 0.499999985098839 | d ₁₂ | -1.959839582443237 | |
| | n ₁₃ | 0.25 | d ₁₃ | 0.960373640060425 | |
| | n ₂₁ | 1 | d ₂₁ | 1 | |
| | n ₂₂ | 0 | d ₂₂ | 0 | |
| | n ₂₃ | 0 | d ₂₃ | 0 | |
| 400 Hz LPF | a ₀ | 0.003135988372378 | | | 3392/f _{osc} |
| | n ₁₁ | 0.000999420881271 | d ₁₁ | 1.0 | |
| | n ₁₂ | 0.001998946070671 | d ₁₂ | -1.892452478408814 | |
| | n ₁₃ | 0.000999405980110 | d ₁₃ | 0.89558845758438 | |
| | n ₂₁ | 0.250004753470421 | d ₂₁ | 1.0 | |
| | n ₂₂ | 0.499986037611961 | d ₂₂ | -1.919075012207031 | |
| | n ₂₃ | 0.250009194016457 | d ₂₃ | 0.923072755336761 | |
| 800 Hz LPF | a ₀ | 0.011904109735042 | | | 1728/f _{osc} |
| | n ₁₁ | 0.003841564059258 | d ₁₁ | 1.0 | |
| | n ₁₂ | 0.007683292031288 | d ₁₂ | -1.790004611015320 | |
| | n ₁₃ | 0.003841534256935 | d ₁₃ | 0.801908731460571 | |
| | n ₂₁ | 0.250001862645149 | d ₂₁ | 1.0 | |
| | n ₂₂ | 0.499994158744812 | d ₂₂ | -1.836849451065064 | |
| | n ₂₃ | 0.250003993511200 | d ₂₃ | 0.852215826511383 | |

Note: Low Pass Filter Figures do not include g-cell frequency response.

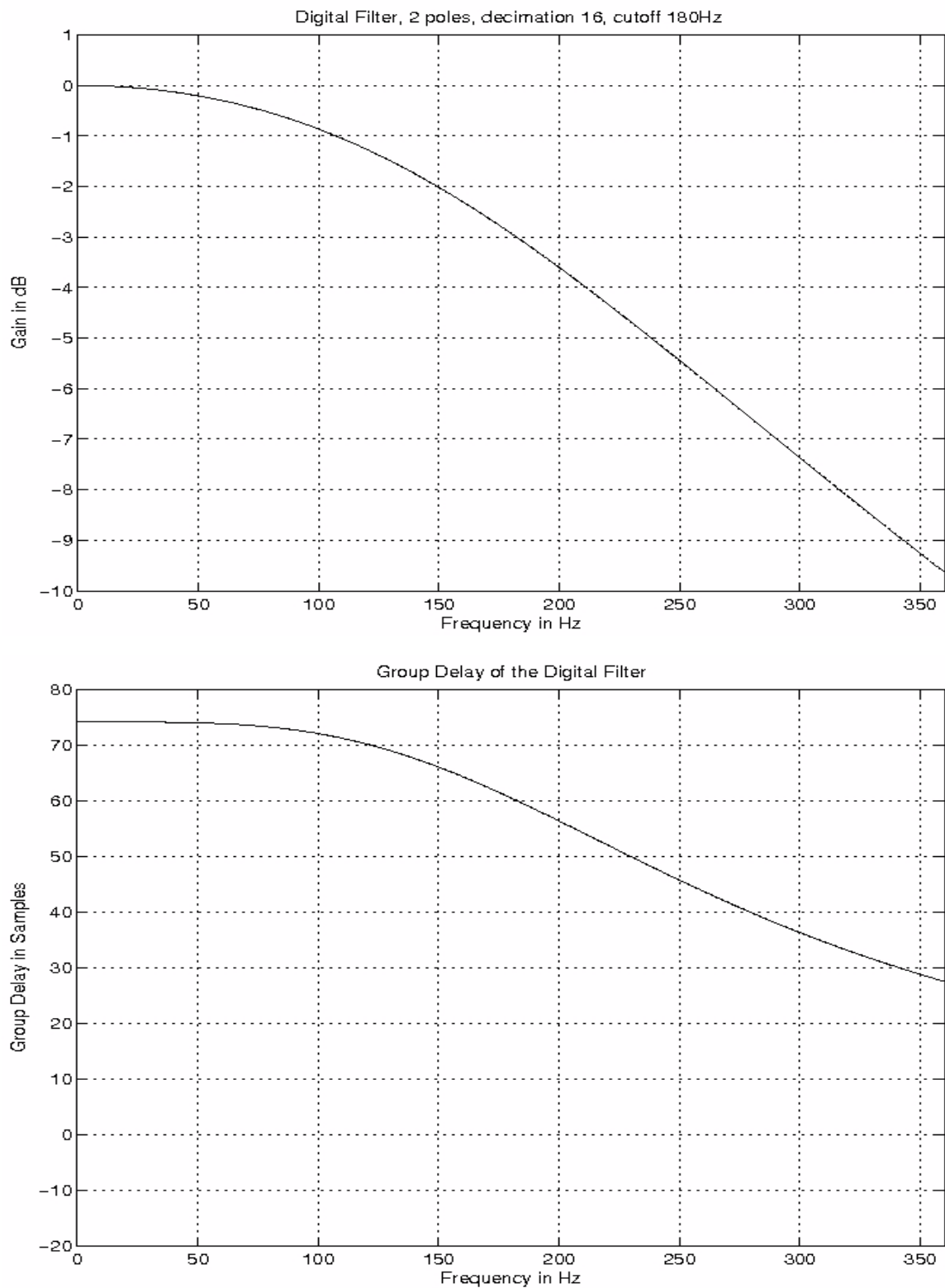


Figure 15. Low-Pass Filter Characteristics: $f_C = 180$ Hz, 2-Pole, $t_S = 16 \mu s$

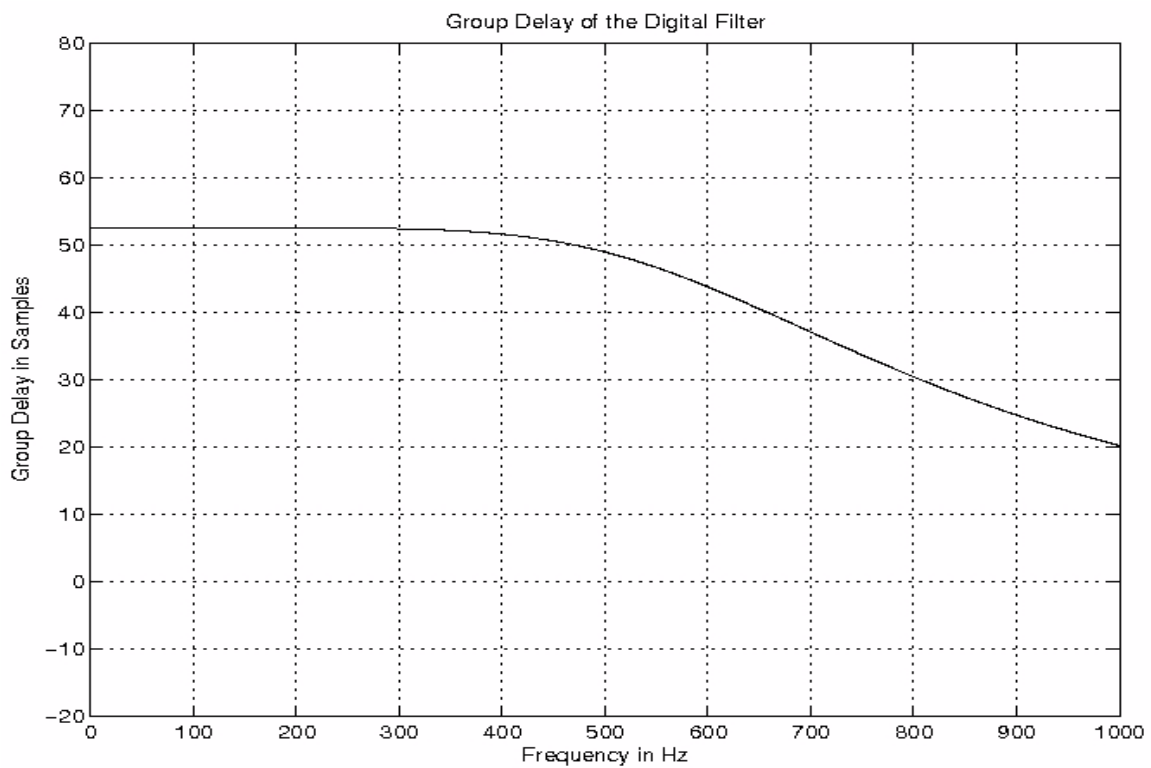
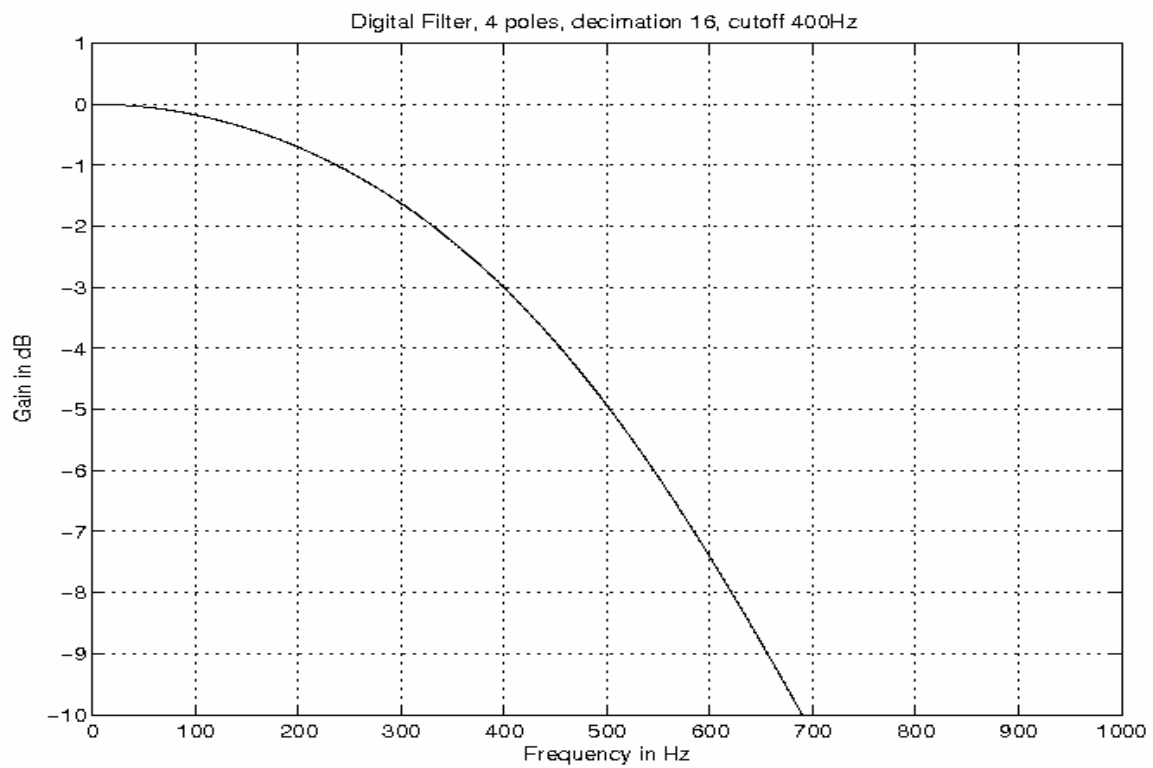


Figure 16. Low-Pass Filter Characteristics: $f_C = 400$ Hz, 4-Pole, $t_S = 16 \mu s$

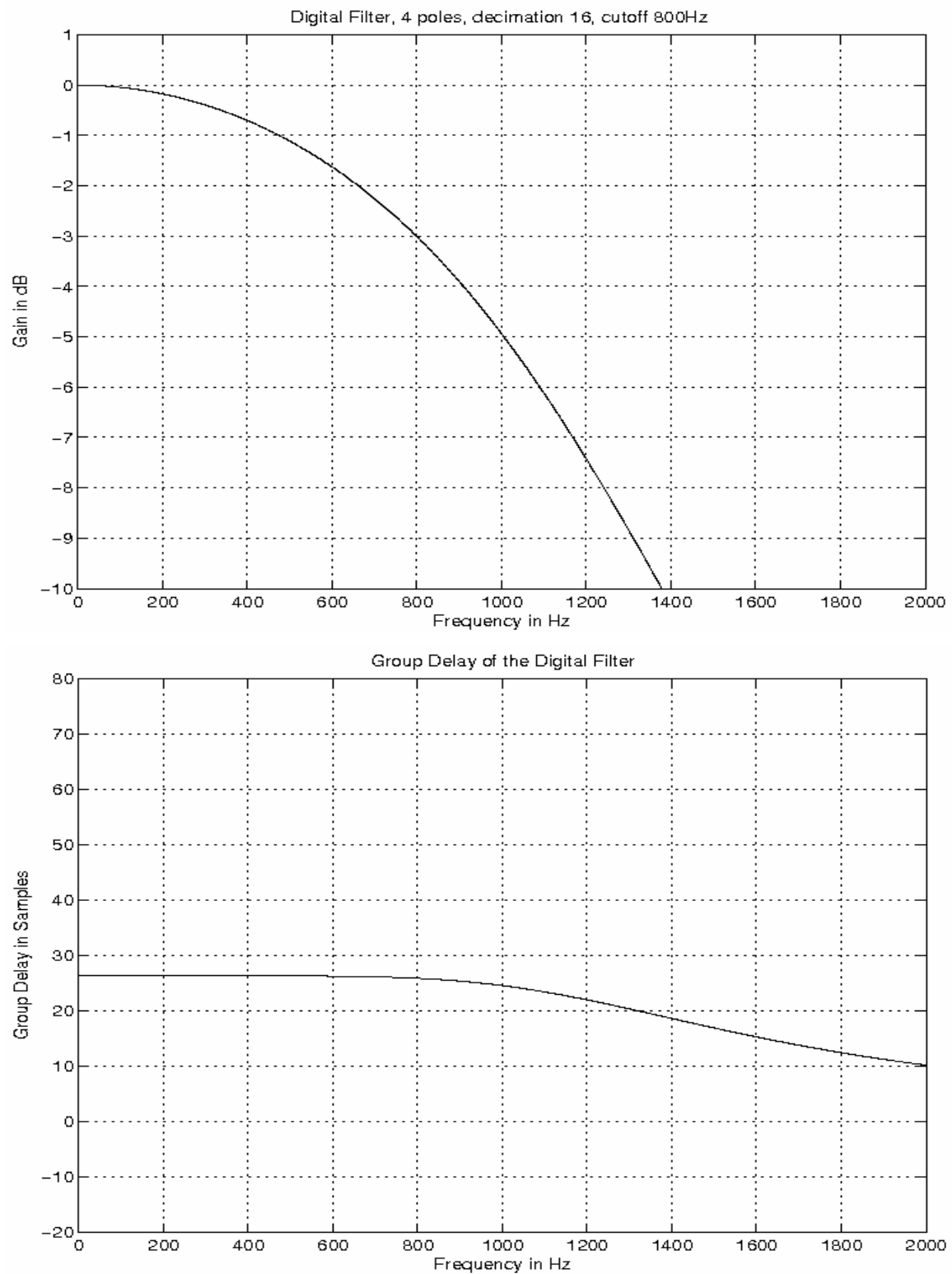


Figure 17. Low-Pass Filter Characteristics: $f_c = 800$ Hz, 4-Pole, $t_s = 16 \mu s$

3.5.3.3 Compensation

The device includes internal compensation circuitry to compensate for sensor offset, sensitivity and non-linearity.

3.5.3.4 Data Interpolation

The device includes 16 to 1 linear data interpolation to minimize the system sample jitter. Each result produced by the digital signal processing chain is delayed one sample time. On reception of an acceleration data request, the transmitted data is interpolated from the 2 previous samples, resulting in a latency of one sample time, and a maximum signal jitter of $\pm 1/16$ of a sample time. Reference [Figure 8](#) for more information regarding interpolation and data latency.

3.5.3.5 Output Scaling

The 26 bit digital output from the DSP is clipped and scaled to a 10-bit or 8-Bit word which covers the acceleration range of the device. [Figure 18](#) shows the method used to establish the acceleration data word from the 26-bit DSP output.

| Over Range | | | | Signal | | | | | | | | | | Noise | | | Margin | | | | | | |
|------------------|-----|-----|-----|--------|-----|-----|-----|-----|-----|-----|-----|------------------|------------------|------------------|-----|----|--------|-----|----|----|----|--|--|
| D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | ... | D2 | D1 | D0 | | |
| | | | | | | | | | | | | | | | | | | | | | | | |
| 10 Bit Data Word | | | | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | Using Truncation | | | | | | | | | |
| 9 Bit Data Word | | | | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | Using Truncation | | | | | | | | | | |
| 8 Bit Data Word | | | | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | Using Truncation | | | | | | | | | | | |

Figure 18. Output Scaling Diagram

3.5.3.6 PCM Output Function

The device provides the option for a PCM output function. The PCM output is activated if the PCM bit is set in the DEVCFG2 register. When the PCM function is enabled, a 4 MHz Pulse Code Modulated signal proportional to the upper 9 bits of the acceleration response is output onto the PCM pin. The PCM output is intended for test use only. A block diagram of the PCM output output is shown in [Figure 19](#).

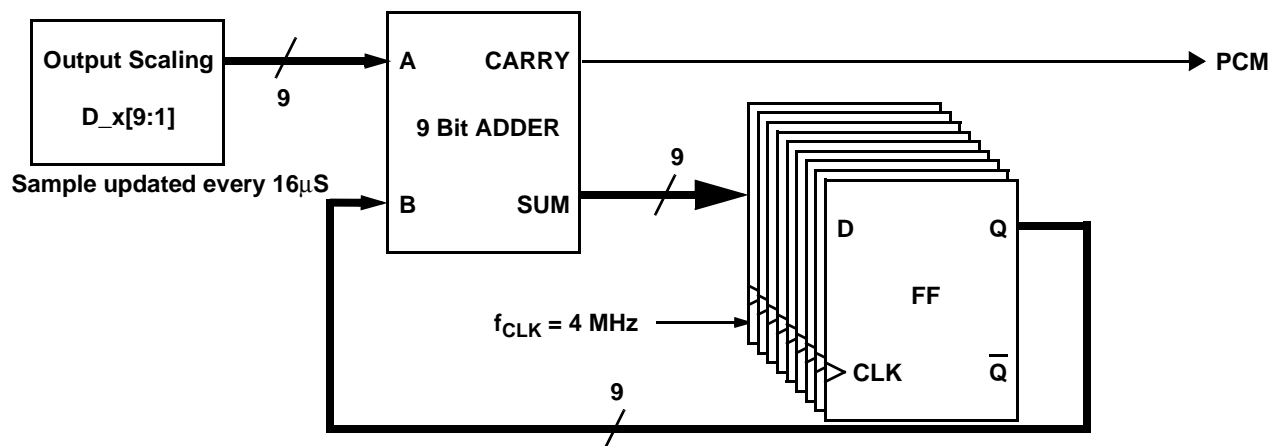


Figure 19. PCM Output Function Block Diagram

3.6 Device Initialization

Following power-up, under-voltage reset or reception of a DSI Clear Command, the device proceeds through an initialization process as described in the following tables:

Table 9. Power-up or Under-Voltage Reset Initialization Process

| # | Description | Time | S Flag | ST Flag | DSI Response |
|---|---|-----------------|--------|---------|---|
| 1 | Power up to a Known State | 0 | N/A | N/A | No Response |
| 3 | Read Fuse Array and Copy to Memory Array (Mirror Registers) | | 1 | 0 | No Response |
| 4 | Initialize DSI State Machine (the device is ready for DSI Messages) | t_{DSI_INIT} | 1 | 0 | DSI Read Acceleration Data Short response = zero. DSI Read Acceleration Data Long response = invalid data. |
| 5 | Initialize the DSP (Acceleration Data is Valid) | t_{DSP_INIT} | 0 | 0 | Normal |

Table 10. DSI Clear Command Initialization Process

| # | Description | Time | S Flag | ST Flag | DSI Response |
|---|---|-----------------|--------|---------|---|
| 1 | the device logic comes out of reset | 0 | 1 | 0 | No Response |
| 3 | Read Fuse Array and Copy to Memory Array (Mirror Registers) | | 1 | 0 | No Response |
| 4 | Initialize DSI State Machine (the device is ready for DSI Messages) | t_{DSI_INIT} | 1 | 0 | DSI Read Acceleration Data Short response = zero. DSI Read Acceleration Data Long response = invalid data. |
| 5 | Initialize the DSP (Acceleration Data is Valid) | t_{DSP_INIT} | 0 | 0 | Normal |

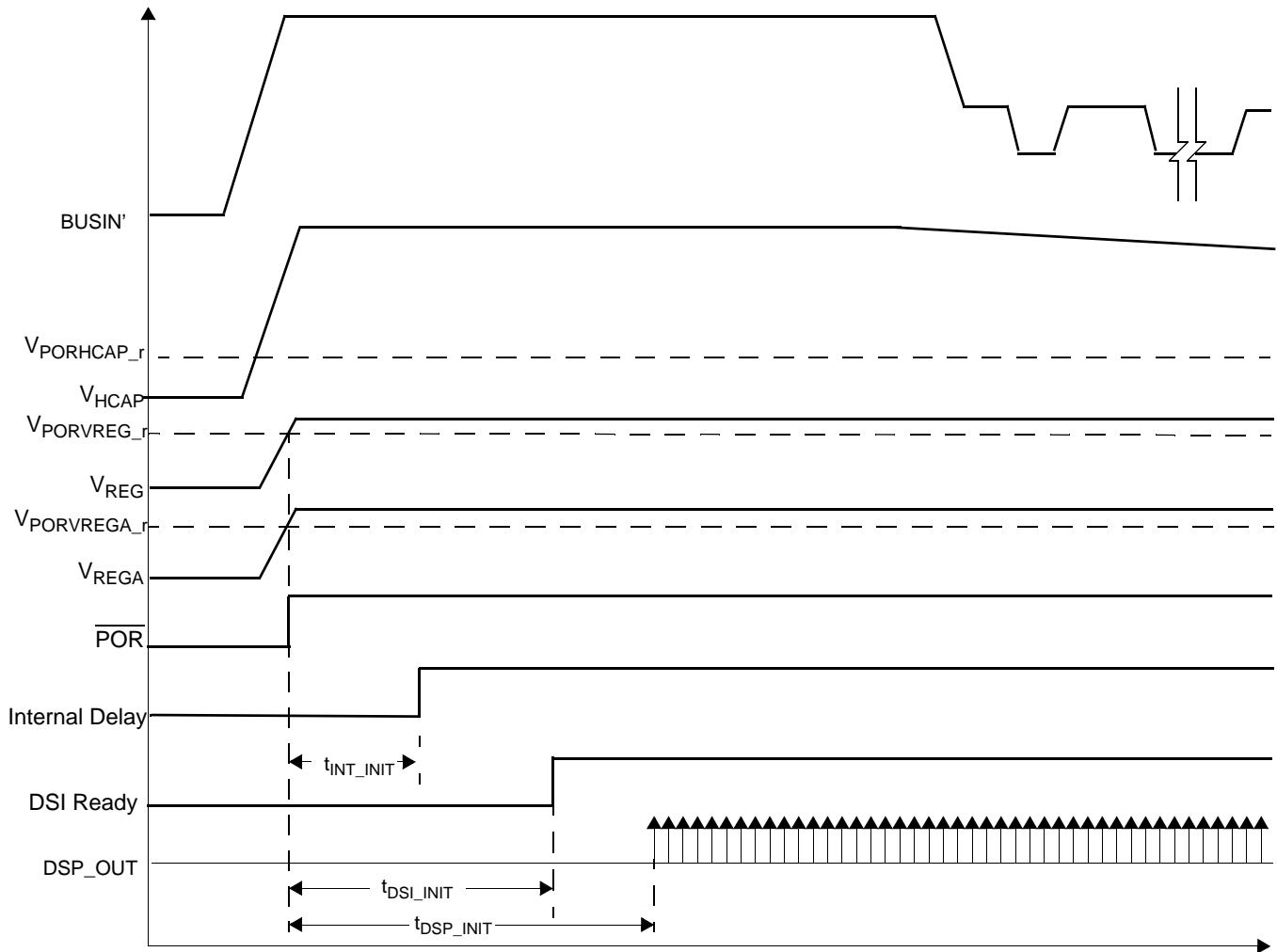


Figure 20. Initialization Timing

3.7 Overload Response

3.7.1 Overload Performance

The device is designed to operate within a specified range. However, acceleration beyond that range (overload) impacts the operating range output of the sensor. Acceleration beyond the range of the device can generate a DC shift at the output of the device that is dependent upon the overload frequency and amplitude. The device g-cell is overdamped, providing the optimal design for overload performance. However, the performance of the device during an overload condition is affected by many other parameters, including:

- g-cell damping
- Non-linearity
- Clipping limits
- Symmetry

Figure 21 shows the g-cell, Sigma Delta, and output clipping of the device over frequency. The relevant parameters are specified in Section 2.

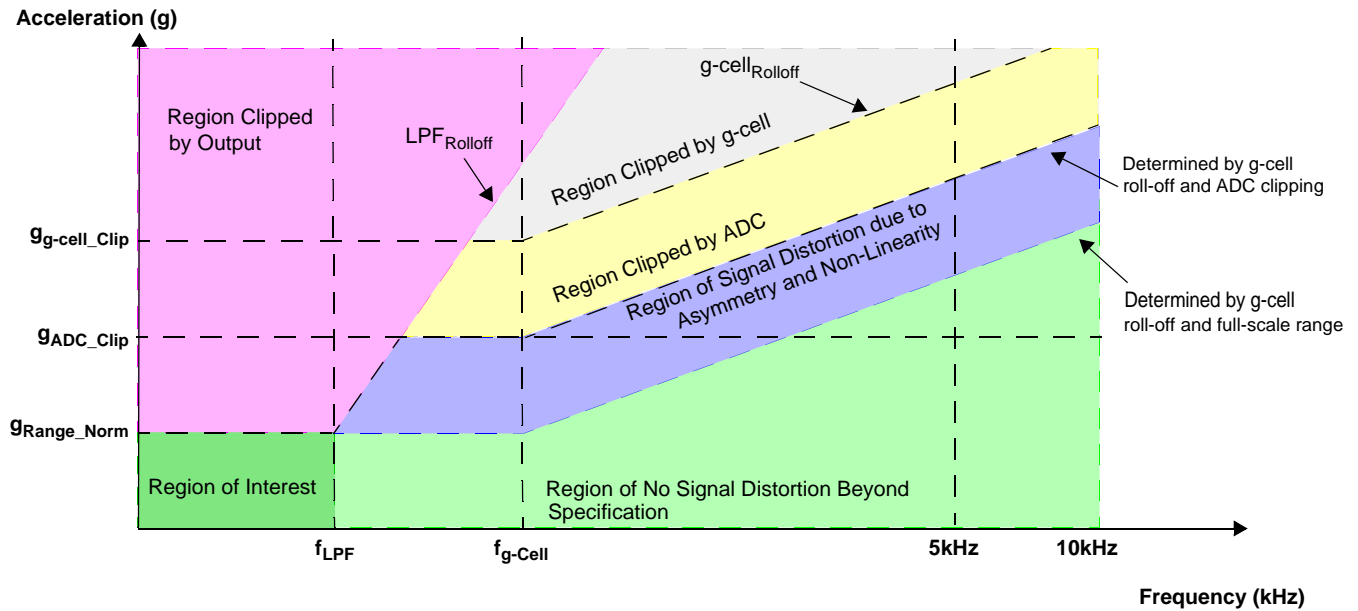


Figure 21. Output Clipping Vs. Frequency

3.7.2 Sigma Delta Overrange Response

Overrange conditions exist when the signal level is beyond the full-scale range of the device but within the computational limits of the DSP. The $\Sigma\Delta$ converter can saturate at levels above those specified in Section 2 ($G_{\text{ADC_CLIP}}$). The DSP operates predictably under all cases of overrange, although the signal may include residual high frequency components for some time after returning to the normal range of operation due to non-linear effects of the sensor.

4 DSI Protocol Layer

4.1 Communication Interface Overview

The device is compatible with the DSI Bus Standard V2.5.

4.1.1 DSI Physical Layer

Reference DSI Bus Standard V2.5, Section 3 for information regarding the physical layer.

4.1.2 DSI Data Link Layer

Reference DSI Bus Standard, V2.5, Section 4 for information regarding the DSI data link layer. The sections below describe the DSI data link layer features supported.

4.2 DSI Protocol

4.2.1 DSI Bus Commands

DSI Bus Commands are summarized in [Table 11](#). The device supports only the command formats specified in [Section 4.2.1](#). The device will ignore commands of any other format. If a CRC error is detected, or a reserved or un-implemented command is received, the device will not respond.

Following all messages, the device requires a minimum inter-frame separation (t_{IFS}). As long as the minimum inter-frame separation times defined in [Section 4.2.1](#) are met, all supported commands are guaranteed to be executed, and the device will be ready for the next message. The device will respond as appropriate during the subsequent DSI transfer. Exactly one response is attempted.

Table 11. DSI Bus Command Summary

| Command | | | | | | Command Format | Data | | | | | | | |
|---------|----|----|----|-----|------------------------|-----------------------|-----------------|-------|--------|--------|-------|-------|-------|-------|
| C3 | C2 | C1 | C0 | Hex | Description | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | \$0 | Initialization | Standard Long Only | NV | BS | Bnk[1] | Bnk[0] | PA[3] | PA[2] | PA[1] | PA[0] |
| 0 | 0 | 0 | 1 | \$1 | Request Status | Standard/Enhanced L/S | — | — | — | — | — | — | — | — |
| 0 | 0 | 1 | 0 | \$2 | Read Acceleration Data | Standard/Enhanced L/S | — | — | — | — | — | — | — | — |
| 0 | 0 | 1 | 1 | \$3 | Not Implemented | Not Implemented | Not Implemented | | | | | | | |
| 0 | 1 | 0 | 0 | \$4 | Request ID Information | Standard/Enhanced L/S | — | — | — | — | — | — | — | — |
| 0 | 1 | 0 | 1 | \$5 | Not Implemented | Not Implemented | Not Implemented | | | | | | | |
| 0 | 1 | 1 | 0 | \$6 | Not Implemented | Not Implemented | Not Implemented | | | | | | | |
| 0 | 1 | 1 | 1 | \$7 | Clear | Standard/Enhanced L/S | — | — | — | — | — | — | — | — |
| 1 | 0 | 0 | 0 | \$8 | Not Implemented | Not Implemented | Not Implemented | | | | | | | |
| 1 | 0 | 0 | 1 | \$9 | Read Write NVM | Standard/Enhanced L | WA[3] | WA[2] | WA[1] | WA[0] | RD[3] | RD[2] | RD[1] | RD[0] |
| 1 | 0 | 1 | 0 | \$A | Format Control | Standard/Enhanced L | R/W | FA[2] | FA[1] | FA[0] | FD[3] | FD[2] | FD[1] | FD[0] |
| 1 | 0 | 1 | 1 | \$B | Read Register Data | Standard/Enhanced L | 0 | 0 | 0 | 0 | RA[3] | RA[2] | RA[1] | RA[0] |
| 1 | 1 | 0 | 0 | \$C | Disable Self-Test | Standard/Enhanced L/S | — | — | — | — | — | — | — | — |
| 1 | 1 | 0 | 1 | \$D | Activate Self-Test | Standard/Enhanced L/S | — | — | — | — | — | — | — | — |
| 1 | 1 | 1 | 0 | \$E | Not Implemented | Not Implemented | Not Implemented | | | | | | | |
| 1 | 1 | 1 | 1 | \$F | Reverse Initialization | Not Implemented | Not Implemented | | | | | | | |

4.2.1.1 Initialization Command

The initialization command conforms to the description provided in Section 6.1.1 of the DSI Bus Standard V2.5. The initialization command is only supported as a standard long command. No other commands are recognized by the device until a valid standard long initialization command is received.

Table 12. Initialization Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|---------|---------|-------|-------|-------|-------|---------|------|------|------|---------|------|------|------|--------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| NV | BS | Bank[1] | Bank[0] | PA[3] | PA[2] | PA[1] | PA[0] | A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 0 | 4 bits |

Table 13. Initialization Command Bit Definitions

| Bit Field | Definition |
|-----------|--|
| C[3:0] | Initialization Command = '0000' |
| A[3:0] | DSI device address. This address is set to the preprogrammed device address following reset, or to '0000' if no preprogrammed address has been assigned. |
| PA[3:0] | DSI Address to be programmed. |
| Bank[1:0] | These bits select the bank address for the user writable data registers. Bank selection affects the Read/Write NVM command operation. Invalid combinations of B1 and B0 result in no response from the device to the associated initialization. Refer to Section 4.2.1.10 for further details regarding register programming and bank selection. |
| BS | Bus Switch state. This bit controls the state of the DSI bus switch. 1 - Close the bus switch. 0 - Do not close the bus switch. |
| NV | NVM Program Enable. This bit enables programming of the user-programmed OTP locations. Data to be programmed is transferred to the device during subsequent Read Write NVM commands. 1 - Enable OTP programming 0 - Disable OTP programming |

Figure 22 illustrates the sequence of operations performed following negation of internal power-on reset (POR) and execution of a DSI Initialization command. The BUSOUT node is tested for a bus short to high voltage condition, and the bus fault (BF) flag is set if an error condition is detected. If no bus fault condition is detected and the BS bit is set in the Initialization command message, the bus switch will be closed. The device implements a blanking time ($t_{DSI_BLANK_INIT}$) to allow for the bus voltage to recover following closure of the bus switch.

If the device has been preprogrammed, PA[3:0] and A[3:0] must match the preprogrammed address.

If no device address has been previously programmed into the OTP array, PA[3:0] contains the device address, and A[3:0] must be zero. If either addressing condition is not met, the device address is not assigned, the bus switch will remain open and the device will not respond to the Initialization command. If the addressing conditions are met, the new device address is assigned to A[3:0]. Once the device address is assigned, the new address (A[3:0]) is not protected by the User Programmable OTP Array CRC Verification. The User Programmable OTP array CRC is calculated and verified using the OTP programmed values of A[3:0] = '0000'.

Once initialized, the device will no longer recognize or respond to Initialization commands.

Table 14. Initialization Command Response

| Response | | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|-------|------|------|------|------|---------|---------|-------|-------|-------|-------|--------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| PA[3] | PA[2] | PA[1] | PA[0] | 0 | 0 | 0 | BF | NV | BS | Bank[1] | Bank[0] | PA[3] | PA[2] | PA[1] | PA[0] | 4 bits |

Table 15. Initialization Response Bit Definitions

| Bit Field | Definition |
|-----------|--|
| PA[3:0] | DSI device address. This field contains the device address. If the device is unprogrammed when the initialization command is issued, the device address is assigned. This field contains the programmed address. An Initialization command which attempts to assign a device address of zero is ignored. |
| Bnk[1:0] | These bits select the bank address for the user writable data registers. Bank selection affects the Read/Write NVM command operation. Invalid combinations of B1 and B0 result in no response from the device to the associated initialization. Refer to Section 4.2.1.10 for further details regarding register programming and bank selection. |
| BS | Bus Switch state. This bit controls the state of the bus switch: 1 - Close the bus switch 0 - Do not close the bus switch |
| NV | NVM Program Enable. This bit indicates if programming of the user-accessible OTP is enabled. 1 - OTP programming Enabled 0 - OTP programming Disabled |
| BF | This bit indicates the success or failure of the bus test performed as part of the Initialization command. 1 - Bus fault detected 0 - Bus test passed |

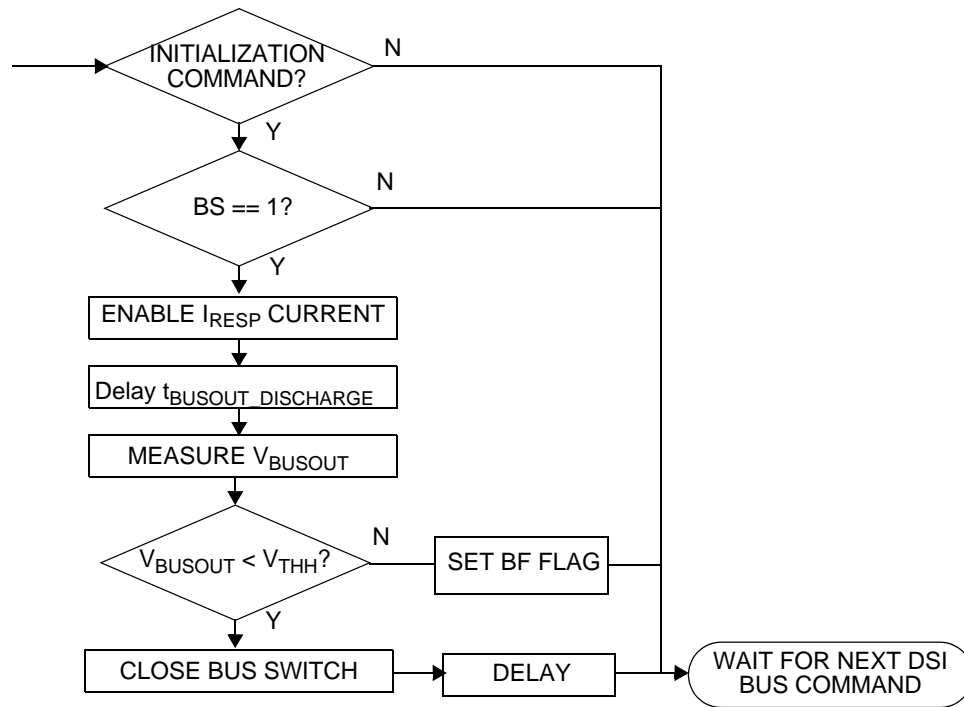


Figure 22. Initialization Sequence

4.2.1.2 Request Status Command

The Request Status command is supported in the following command formats:

- Standard Long Command
- Standard Short Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))
- Enhanced Short Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The device ignores the Request Status command if the DSI device address is set to the DSI Global Device Address of '0000'. The data bits D[7:0] in the command are only used in the CRC calculation.

Table 16. Request Status Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|------|------|------|------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| — | — | — | — | — | — | — | — | A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 1 | 0 to 8 bits |

Table 17. Request Status Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Request Status Command = '0001' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| D[7:0] | Used for CRC calculation only |

Table 18. Short Response - Request Status Command

| Response | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|------|------|------|------|------|------|-------|-------|------|------|-------------|
| D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | NV | U | ST | BS | AT[1] | AT[0] | S | 0 | 0 to 8 bits |

Table 19. Long Response - Request Status Command

| Data | | | | | | | | | | | | | | | CRC | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|-------|-------|------|-----|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | | D[0] |
| A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 0 | NV | U | ST | BS | AT[1] | AT[0] | S | 0 | 0 to 8 bits |

Table 20. Request Status Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| S | This bit indicates whether the device has detected an internal device error. 1 - Internal Error detected. 0 - No Internal Error detected Reference Table 59 for conditions that set the S bit. |
| AT[1:0] | Attribute bits located in Register DEVCFG1 (Reference Section 3.1.4.2) |
| BS | Bus Switch state. This bit controls the state of the bus switch: 1 - Close the bus switch 0 - Do not close the bus switch |
| ST | This bit indicates whether internal self-test circuitry is active 1 - Self-test active 0 - Self-test disabled |
| U | This bit is set if the voltage at HCAP is below the threshold specified in Section 2 . Refer to Section 3.3.2 for details. |
| NV | NVM Program Enable. This bit indicates whether programming of the user-programmable OTP locations is enabled. 1 - OTP programming Enabled 0 - OTP programming Disabled |
| A[3:0] | DSI device address. This field contains the device address. |
| | Shaded bits are transmitted to meet the response message length of the received message |

4.2.1.3 Read Acceleration Data Command

The Read Acceleration Data command is supported in the following command formats:

- Standard Long Command
- Standard Short Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))
- Enhanced Short Command as configured by the Form at Control Command (Reference [Section 4.2.1.11](#))

The device ignores the Request Status command if the DSI device address is set to the DSI Global Device Address of '0000'. The data bits D[7:0] in the command are only used in the CRC calculation.

Table 21. Read Acceleration Data Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|------|------|------|------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| — | — | — | — | — | — | — | — | A[3] | A[2] | A[1] | A[0] | 0 | 0 | 1 | 0 | 0 to 8 bits |

Table 22. Read Acceleration Data Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Read Acceleration Data Command = '0010' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| D[7:0] | Used for CRC calculation only |

Table 23. Short Response - Read Acceleration Data Command

| Response Length | Response | | | | | | | | | | | | | | | CRC |
|-----------------|-----------|-----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------------|
| | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| 8 | | | | | | | | AD[9] | AD[8] | AD[7] | AD[6] | AD[5] | AD[4] | AD[3] | AD[2] | 0 to 8 bits |
| 9 | | | | | | | AD[9] | AD[8] | AD[7] | AD[6] | AD[5] | AD[4] | AD[3] | AD[2] | AD[1] | |
| 10 | | | | | | | | | | | | | | | | |
| 11 | | | | | | | | | | | | | | | | |
| 12 | | | | | | | | | | | | | | | | |
| 13 | | | | | | | | | | | | | | | | |
| 14 | | | | | | | | | | | | | | | | |
| 15 | AT_OTP[1] | AT_OTP[0] | ST | 0 | S | AD[9] | AD[8] | AD[7] | AD[6] | AD[5] | AD[4] | AD[3] | AD[2] | AD[1] | AD[0] | |

Table 24. Long Response - Read Acceleration Data Command

| Response | | | | | | | | | | | | | | | CRC | |
|----------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | | D[0] |
| A[3] | A[2] | A[1] | A[0] | 0 | S | AD[9] | AD[8] | AD[7] | AD[6] | AD[5] | AD[4] | AD[3] | AD[2] | AD[1] | AD[0] | 0 to 8 bits |

Table 25. Read Acceleration Response Bit Definitions

| Bit Field | Definition |
|-------------|---|
| AD[9:0] | 10-bit acceleration result produced by the device. |
| S | This bit indicates whether the device has detected an internal device error. 1 - Internal Error detected. 0 - No Internal Error detected Reference Table 59 for conditions that set the S bit. |
| ST | This bit indicates whether internal self-test circuitry is active 1 - Self-test active 0 - Self-test disabled |
| A[3:0] | DSI device address. This field contains the device address. |
| AT_OTP[1:0] | Attribute bits located in Register DEVCFG1 (Reference Section 3.1.4.2) |
| | Shaded bits are transmitted to meet the response message length of the received message |

The device truncates the LSBs for Acceleration Data Responses of length less than 10. If the result of the truncation is 0, the minimum acceleration value is transmitted as defined in [Table 26](#).

Table 26. Acceleration Data Values

| 8-Bit Data Value | | 9-Bit Data Value | | 10-Bit Data Value | | Description |
|------------------|------|------------------|-------|-------------------|-------|-------------------------------------|
| Decimal | Hex | Decimal | Hex | Decimal | Hex | |
| 255 | 0xFF | 511 | 0x1FF | 1023 | 0x3FF | Maximum positive acceleration value |
| • | • | • | • | • | • | Positive acceleration values |
| • | • | • | • | • | • | |
| • | • | • | • | • | • | |
| 131 | 0x83 | 259 | 0x103 | 515 | 0x203 | |
| 130 | 0x82 | 258 | 0x102 | 514 | 0x202 | |
| 129 | 0x81 | 257 | 0x101 | 513 | 0x201 | Typical 0 g level |
| 128 | 0x80 | 256 | 0x100 | 512 | 0x200 | |
| 127 | 0x7F | 127 | 0x0FF | 511 | 0x1FF | Negative acceleration values |
| 126 | 0x7E | 126 | 0x0FE | 510 | 0x1FE | |
| 125 | 0x7D | 125 | 0x0FD | 509 | 0x1FD | |
| • | • | • | • | • | • | |
| • | • | • | • | • | • | |
| • | • | • | • | • | • | |
| 1 | 1 | 1 | 1 | 1 | 1 | Maximum negative acceleration value |
| 0 | 0 | 0 | 0 | 0 | 0 | Sensor Error |

4.2.1.4 DSI Command #3

DSI Command '0011' is not implemented. The device ignores all command formats with a command ID of '0011'.

4.2.1.5 Request ID Information Command

The Request ID Information command is supported in the following command formats:

- Standard Long Command
- Standard Short Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))
- Enhanced Short Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The device ignores the Request ID Information command if the DSI device address is set to the DSI Global Device Address of '0000'. The data bits D[7:0] in the command are only used in the CRC calculation.

Table 27. Request ID Information Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|------|------|------|------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| — | — | — | — | — | — | — | — | A[3] | A[2] | A[1] | A[0] | 0 | 1 | 0 | 0 | 0 to 8 bits |

Table 28. Request ID Information Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Request ID Information Data Command = '0100' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| D[7:0] | Used for CRC calculation only |

Table 29. Short Response - Request ID Information Command

| Response | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|------|------|------|------|------|------|-------|------|------|------|-------------|
| D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | V2 | V1 | V0 | 0 | DEVID | 1 | 0 | 0 | 0 to 8 bits |

Table 30. Long Response - Request ID Information Command

| Response | | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|-------|------|------|------|------|------|------|-------|------|------|------|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 0 | V[2] | V[1] | V[0] | 0 | DEVID | 1 | 0 | 0 | 0 to 8 bits |

Table 31. Request ID Response Bit Definitions

| Bit Field | Definition |
|--------------------------------|---|
| D[4:0] = {1'b0, DEVID, 3'b100} | Device Identifier: '00100', or '01100' DEVID: Bit 7 of the DEVCFG register |
| V[2:0] | Version ID. This field indicates the device / silicon revision of the device. |
| A[3:0] | DSI device address. This field contains the device address. |
| | Shaded bits are transmitted to meet the response message length of the received message |

4.2.1.6 DSI Command #5

DSI Command '0101' is not implemented. The device ignores all command formats with a command ID of '0101'.

4.2.1.7 DSI Command #6

DSI Command '0110' is not implemented. The device ignores all command formats with a command ID of '0110'.

4.2.1.8 Clear Command

The Clear command is supported in the following command formats:

- Standard Long Command
- Standard Short Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))
- Enhanced Short Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

When the device successfully decodes a Clear Command, and the address field matches either the assigned device address (PA[3:0]) or the DSI Global address of '0000', the bus switch is opened within T_{BSOPEN} , and the device logic is reset. Reference [Section 3.6](#) for the initialization sequence following a Clear Command. The data bits D[7:0] in the command are only used in the CRC calculation. There is no response to the Clear Command.

Table 32. Clear Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|------|------|------|------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| — | — | — | — | — | — | — | — | A[3] | A[2] | A[1] | A[0] | 0 | 1 | 1 | 1 | 0 to 8 bits |

Table 33. Clear Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Clear Command = '0111'. When a Clear Command is successfully decoded and the address field matches either the assigned device address or the DSI Global Device Address of '0000', the bus switch is opened within t_{BSOPEN} , and the device logic is reset. Reference Section 3.6 for the initialization sequence following a Clear Command. |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field or the Global Device Address of '0000'. Otherwise, the command is ignored. |
| D[7:0] | Used for CRC calculation only |

4.2.1.9 DSI Command #8

DSI Command '1000' is not implemented. The device ignores all command formats with a command ID of '1000'.

4.2.1.10 Write NVM Command

The Write NVM command is supported in the following command formats:

- Standard Long Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The device ignores the Write NVM command if the command is in any other format, or if the DSI device address is set to the DSI Global Device Address of '0000'.

The Write NVM command uses the nibble address definitions in [Table 2](#) and summarized in [Table 39](#).

Table 34. Write NVM Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|-------|-------|-------|-------|-------|-------|-------|-------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| WA[3] | WA[2] | WA[1] | WA[0] | RD[3] | RD[2] | RD[1] | RD[0] | A[3] | A[2] | A[1] | A[0] | 1 | 0 | 0 | 1 | 0 to 8 bits |

Table 35. Write NVM Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Write NVM Command = '1001' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| RD[3:0] | RD[3:0] contains the data to be written to the OTP location addressed by WA[3:0] when the NV bit is set. |
| WA[3:0] | WA[3:0] contains the nibble address of the OTP register to be written to when the NV bit is set. |

Table 36. Long Response - Write NVM Command (NV = 1)

| Data | | | | | | | | | | | | | | | CRC | |
|-------|-------|-------|-------|-------|-------|-------|-------|------|------|--------|--------|-------|-------|-------|-------|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | | D[0] |
| A[3] | A[2] | A[1] | A[0] | WA[3] | WA[2] | WA[1] | WA[0] | 1 | 1 | Bnk[1] | Bnk[0] | RD[3] | RD[2] | RD[1] | RD[0] | 0 to 8 bits |

Table 37. Long Response - Write NVM Command (NV = 0)

| Data | | | | | | | | | | | | | | | CRC | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | | D[0] |
| A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | A[3] | A[2] | A[1] | A[0] | 0 to 8 bits |

Table 38. Write NVM Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| Bnk[1:0] | These bits provide the bank address selected in the Initialization command. |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| RD[3:0] | RD[3:0] contains the contents of the registers addressed by WA[3:0] after the execution of the NVM write. |
| WA[3:0] | WA[3:0] contains the nibble address of the OTP register to be written to when the NV bit is set. |

Writes to OTP occur only if the NV bit is set. The NV bit is set by the Initialization Command (reference [Section 4.2.1.1](#)). If the NV bit is cleared when the command is executed, the mirror registers addressed by WA[3:0] are updated with the contents of RD[3:0] and the DSI Device Address is returned regardless of the WA[3:0] value. If the Write NVM command is a request to change the Device Address, the new Device Address is returned.

The DSI Bus idle voltage must exceed the minimum V_{PP} voltage when programming the OTP array. No internal verification of the VPP voltage is completed while writing is in process. To verify proper writes, it is recommended that the registers be read back after writes to verify proper contents. The total Execution time for the Write NVM command is t_{PROG_BIT} times the number of bits being programmed (1 - 4 bits). Inter-frame spacing between the Write NVM command and the subsequent DSI command must accommodate this timing.

Writes to the User Programmable OTP array using the Write NVM Command will update the mirror registers and result in a change to the CRC calculation regardless of the state of the NV bit and the LOCK_U bit. A CRC mismatch will only be detected if the LOCK_U bit is active (reference [Section 3.2.2](#)).

Table 39. OTP Register Nibble Address Assignments

| Bank Address | | Register Address (Nibble) | | | | Register | Description |
|--------------|--------|---------------------------|-------|-------|-------|--------------|---|
| Bnk[1] | Bnk[0] | WA[3] | WA[2] | WA[1] | WA[0] | | |
| x | x | 0 | 0 | 0 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| x | x | 0 | 0 | 0 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| x | x | 0 | 0 | 1 | 0 | | |
| x | x | 0 | 0 | 1 | 1 | | |
| x | x | 0 | 1 | 0 | 0 | | |
| x | x | 0 | 1 | 0 | 1 | | |
| 0 | 0 | 0 | 1 | 1 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 0 | 0 | 0 | 1 | 1 | 1 | DEVCFG2[7] | Only RD[3] is written to the LOCK_U bit |
| 0 | 0 | 1 | 0 | 0 | 0 | TYPE[7:6] | Only RD[3:2] is written to LPF[1:0] |
| 0 | 0 | 1 | 0 | 0 | 1 | DEVCFG[3:0] | RD[3] is written to DEVCFG[3] - UNUSED, RD[2:0] is written to CRC_U[2:0] |
| 0 | 0 | 1 | 0 | 1 | 0 | DEVCFG[7:4] | RD[3] is written to the DEVID bit, RD[2:0] is written to DEVCFG[6:4] - UNUSED |
| 0 | 0 | 1 | 0 | 1 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 0 | 0 | 1 | 1 | 0 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 0 | 0 | 1 | 1 | 0 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 0 | 0 | 1 | 1 | 1 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 0 | 0 | 1 | 1 | 1 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 0 | 1 | 0 | 1 | 1 | 0 | DEVCFG1[3:0] | RD[3:2] is written to UD00[1:0], RD[1:0] is written to AT[1:0] |
| 0 | 1 | 0 | 1 | 1 | 1 | DEVCFG2[3:0] | RD[3:0] is written to ADDR[3:0] |
| 0 | 1 | 1 | 0 | 0 | 0 | UD01[3:0] | RD[3:0] is written to UD01[3:0] |
| 0 | 1 | 1 | 0 | 0 | 1 | UD02[3:0] | RD[3:0] is written to UD02[3:0] |
| 0 | 1 | 1 | 0 | 1 | 0 | UD03[3:0] | RD[3:0] is written to UD03[3:0] |
| 0 | 1 | 1 | 0 | 1 | 1 | UD04[3:0] | RD[3:0] is written to UD04[3:0] |
| 0 | 1 | 1 | 1 | 0 | 0 | UD05[3:0] | RD[3:0] is written to UD05[3:0] |
| 0 | 1 | 1 | 1 | 0 | 1 | UD06[3:0] | RD[3:0] is written to UD06[3:0] |
| 0 | 1 | 1 | 1 | 1 | 0 | UD07[3:0] | RD[3:0] is written to UD07[3:0] |
| 0 | 1 | 1 | 1 | 1 | 1 | UD08[3:0] | RD[3:0] is written to UD08[3:0] |
| 1 | 0 | 0 | 1 | 1 | 0 | DEVCFG1[7:4] | RD[3:0] is written to UD00[5:2] |
| 1 | 0 | 0 | 1 | 1 | 1 | DEVCFG2[5] | Only RD[1] is written to the PCM bit |
| 1 | 0 | 1 | 0 | 0 | 0 | UD01[7:4] | RD[3:0] is written to UD01[7:4] |
| 1 | 0 | 1 | 0 | 0 | 1 | UD02[7:4] | RD[3:0] is written to UD02[7:4] |
| 1 | 0 | 1 | 0 | 1 | 0 | UD03[7:4] | RD[3:0] is written to UD03[7:4] |
| 1 | 0 | 1 | 0 | 1 | 1 | UD04[7:4] | RD[3:0] is written to UD04[7:4] |
| 1 | 0 | 1 | 1 | 0 | 0 | UD05[7:4] | RD[3:0] is written to UD05[7:4] |
| 1 | 0 | 1 | 1 | 0 | 1 | UD06[7:4] | RD[3:0] is written to UD06[7:4] |
| 1 | 0 | 1 | 1 | 1 | 0 | UD07[7:4] | RD[3:0] is written to UD07[7:4] |
| 1 | 0 | 1 | 1 | 1 | 1 | UD08[7:4] | RD[3:0] is written to UD08[7:4] |
| 1 | 1 | 0 | 1 | 1 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 0 | 1 | 1 | 1 | DEVCFG2[6] | Only RD[2] is written to the DEVCFG2[6] bit (UNUSED) |
| 1 | 1 | 1 | 0 | 0 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 0 | 0 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 0 | 1 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 0 | 1 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 1 | 0 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 1 | 0 | 1 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 1 | 1 | 0 | UNUSED | No Write to NVM executed, Normal Response: RD[3:0] = Device Address ADDR[3:0] |
| 1 | 1 | 1 | 1 | 1 | 1 | DEVCFG2[4] | Only RD[0] is written to DEVCFG2[4] |

4.2.1.11 Format Control Command

The Format Control command is supported in the following command formats:

- Standard Long Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The device ignores the Format Control command if the command is in any other format. The device supports the Format Control command with the DSI Global Address of '0000', but does not provide a response.

Table 40. Format Control Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|-------|-------|-------|-------|-------|-------|-------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| R/W | FA[2] | FA[1] | FA[0] | FD[3] | FD[2] | FD[1] | FD[0] | A[3] | A[2] | A[1] | A[0] | 1 | 0 | 1 | 0 | 0 to 8 bits |

Table 41. Format Control Command Bit Definitions

| Bit Field | Definition |
|-----------|--|
| C[3:0] | Format Control Command = '1010' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| FD[3:0] | Data to be written to the Format Control Register addressed by FA[2:0] if the R/W bit is set to '1'. |
| FA[2:0] | The Address of the Format Control Register to read or written. |
| R/W | Read/Write determines if the register at address FA[2:0] is to be read or written. 1 - Write FD[3:0] to the Format Control Register addressed by FA[2:0] 0 - Read the Format Control Register addressed by FA[2:0] |

Table 42. Long Response - Format Control Command

| Response | | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|-------|------|------|------|-------|-------|-------|-------|-------|-------|-------|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| A[3] | A[2] | A[1] | A[0] | 0 | 1 | 1 | 0 | R/W | FA[2] | FA[1] | FA[0] | FD[3] | FD[2] | FD[1] | FD[0] | 0 to 8 bits |

Table 43. Format Control Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| FD[3:0] | The contents of the Format Control Register addressed by FA[2:0]. |
| FA[2:0] | The Address of the Format Control Register that was read or written. |
| R/W | Read/Write indicates if the register at address FA[2:0] was read or written. 1 - FD[3:0] contains the data written to the Format Control Register addressed by FA[2:0] 0 - FD[3:0] contains the contents for the Format Control Register addressed by FA[2:0] |
| A[3:0] | DSI device address. This field contains the device address. |

The format control registers defined in the DSI Bus Standard V2.5 are shown in [Table 44](#). The reset values assigned to each register are also indicated.

Table 44. Format Control Register Values

| Format Control Register | Register Address | | | Reset Values | | | | DSI Standard Values | | | | Definition |
|----------------------------------|------------------|-------|-------|--------------|-------|-------|-------|---------------------|-------|-------|-------|----------------------------|
| | FA[2] | FA[1] | FA[0] | FD[3] | FD[2] | FD[1] | FD[0] | FD[3] | FD[2] | FD[1] | FD[0] | |
| CRC Polynomial - Low Nibble | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | CRC Polynomial = $X^4 + 1$ |
| CRC Polynomial - High Nibble | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| Seed - Low Nibble | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | Seed = '1010' |
| Seed - High Nibble | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| CRC Length (0 to 8) | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | CRC Length = 4 |
| Short Word Data Length (8 to 15) | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Short Command Length = 8 |
| Reserved | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | N/A |
| Format Selection | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | N/A |

The following restrictions apply to format control register operations:

- Writes to the CRC Length Register of values greater than 8 are ignored. The contents of the register are unchanged.
- Writes to the Short Word Data Length register of values less than 8 are ignored. The contents of the register are unchanged.

The contents of the Format Selection register determine whether the standard DSI values or the values in the format control registers are used. If the Format Selection register contains '1111', the Format Control register values are active. Any write to the Format Control registers will become active upon completion of the write. In this case, the response to a Format Control Command will maintain the format of the previous command resulting in an invalid response.

A write of '0000' to the Format Selection register activates the standard DSI values.

A write to the Format Selection register of any other value is ignored.

4.2.1.12 Read Register Data Command

The Read Register Data command is supported in the following command formats:

- Standard Long Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The device ignores the Register Data command if the command is in any other format, or if the DSI device address is set to the DSI Global Device Address of '0000'.

The read register command uses the byte address definitions shown in [Table 2](#). Readable registers along with their Byte addresses are shown in [Table 2](#).

Table 45. Read Register Data Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|-------|-------|-------|-------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| 0 | 0 | 0 | 0 | RA[3] | RA[2] | RA[1] | RA[0] | A[3] | A[2] | A[1] | A[0] | 1 | 0 | 1 | 1 | 0 to 8 bits |

Table 46. Read Register Data Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Read Register Data Command = '1011' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| RA[3:0] | RA[3:0] contains the byte address of the register to be read. |

Table 47. Long Response - Read Register Data Command

| Data | | | | | | | | | | | | | | | | CRC |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| A[3] | A[2] | A[1] | A[0] | RA[3] | RA[2] | RA[1] | RA[0] | RD[7] | RD[6] | RD[5] | RD[4] | RD[3] | RD[2] | RD[1] | RD[0] | 0 to 8 bits |

Table 48. Read Register Data Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| RD7:0] | RD[7:0] contains the data of the register addressed by RA[3:0]. |
| RA[3:0] | RA[3:0] contains the byte address of the register to be read. |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |

4.2.1.13 Disable Self-Test Command

The Disable Self-Test command is supported in the following command formats:

- Standard Long Command
- Standard Short Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))
- Enhanced Short Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The data bits D[7:0] in the command are only used in the CRC calculation. The device supports the Disable Self-Test command with the DSI Global Address of '0000', but does not provide a response.

The Disable Self-Test Command removes the voltage from the self-test plate of the transducer which results in the acceleration output value returning to the 0g offset value within $t_{ST_DEACT_xxx}$, as specified in [Section 2](#).

Table 49. Disable Self-Test Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|------|------|------|------|---------|------|------|------|---------|------|------|------|-------------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| — | — | — | — | — | — | — | — | A[3] | A[2] | A[1] | A[0] | 1 | 1 | 0 | 0 | 0 to 8 bits |

Table 50. Disable Self-Test Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Disable Self-Test Command = '1100' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| D[7:0] | Used for CRC calculation only |

Table 51. Short Response - Disable Self-Test Command

| Response | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|------|------|------|------|------|------|-------|-------|------|------|-------------|
| D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | NV | U | ST | BS | AT[1] | AT[0] | S | 0 | 0 to 8 bits |

Table 52. Long Response - Disable Self-Test Command

| Data | | | | | | | | | | | | | | | CRC | |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|-------|-------|------|-----|-------------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | | D[0] |
| A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 0 | NV | U | ST | BS | AT[1] | AT[0] | S | 0 | 0 to 8 bits |

Table 53. Disable Self-Test Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| S | This bit indicates whether the device has detected an internal device error. 1 - Internal Error detected. 0 - No Internal Error detected Reference Table 59 for conditions that set the S bit. |
| AT[1:0] | Attribute bits located in Register DEVCFG1 (Reference Section 3.1.4.2) |
| BS | Bus Switch state. This bit controls the state of the bus switch: 1 - Close the bus switch 0 - Do not close the bus switch |
| ST | This bit indicates whether internal self-test circuitry is active 1 - Self-test active 0 - Self-test disabled |
| U | This bit is set if the voltage at HCAP is below the threshold specified in Section 2 . Refer to Section 3.3.2 for details. |
| NV | NVM Program Enable. This bit indicates whether programming of the user-programmable OTP locations is enabled. 1 - OTP programming Enabled 0 - OTP programming Disabled |
| A[3:0] | DSI device address. This field contains the device address. |

A self-test lockout is activated when the device receives two consecutive Disable Self-Test commands. Once self-test lockout is activated, the internal self-test circuitry is disabled until one of the following conditions occurs:

- HCAP under-voltage
- A Clear command is received
- Internal regulator under-voltage resulting in a reset.
- A Frame Timeout resulting in a reset.

4.2.1.14 Enable Self-Test Command

The Enable Self-Test command is supported in the following command formats:

- Standard Long Command
- Standard Short Command
- Enhanced Long Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))
- Enhanced Short Command as configured by the Format Control Command (Reference [Section 4.2.1.11](#))

The data bits D[7:0] in the command are only used in the CRC calculation. The device ignores the Enable Self-Test command when it is sent to the DSI Global Address of '0000'.

The Enable Self-Test Command applies a voltage to the self-test plate of the transducer which results in a delta in the acceleration output value of $\Delta\text{DFLCT_xxx}$ within $t_{\text{ST_ACT_xxx}}$, as specified in [Section 2](#). This remains present until the Disable Self-Test command is received.

Activation of the self-test circuit is inhibited if the self-test locking has been activated. If self-test locking is activated, the internal self-test circuitry remains disabled, and the ST bit is cleared in the response. Self-test locking is described in [Section 4.2.1.13](#).

Table 54. Enable Self-Test Command

| Data | | | | | | | | Address | | | | Command | | | | CRC |
|------|------|------|------|------|------|------|------|---------|------|------|------|---------|------|------|------|--------|
| D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | A[3] | A[2] | A[1] | A[0] | C[3] | C[2] | C[1] | C[0] | |
| — | — | — | — | — | — | — | — | A[3] | A[2] | A[1] | A[0] | 1 | 1 | 0 | 1 | 4 bits |

Table 55. Enable Self-Test Command Bit Definitions

| Bit Field | Definition |
|-----------|---|
| C[3:0] | Enable Self-Test Command = '1101' |
| A[3:0] | DSI device address. This field contains the device address. This field must match the internal programmed address field. Otherwise, the command is ignored. |
| D[7:0] | Used for CRC calculation only |

Table 56. Short Response - Enable Self-Test Command

| Response | | | | | | | | | | | | | | | CRC |
|----------|-------|-------|-------|-------|------|------|------|------|------|------|-------|-------|------|------|--------|
| D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | NV | U | ST | BS | AT[1] | AT[0] | S | 0 | 4 bits |

Table 57. Long Response - Enable Self-Test Command

| Data | | | | | | | | | | | | | | | | CRC |
|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|-------|-------|------|------|--------|
| D[15] | D[14] | D[13] | D[12] | D[11] | D[10] | D[9] | D[8] | D[7] | D[6] | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] | |
| A[3] | A[2] | A[1] | A[0] | 0 | 0 | 0 | 0 | NV | U | ST | BS | AT[1] | AT[0] | S | 0 | 4 bits |

Table 58. Enable Self-Test Response Bit Definitions

| Bit Field | Definition |
|-----------|---|
| S | This bit indicates whether the device has detected an internal device error. 1 - Internal Error detected. 0 - No Internal Error detected Reference Table 59 for conditions that set the S bit. |
| AT[1:0] | Attribute bits located in Register DEVCFG1 (Reference Section 3.1.4.2) |
| BS | Bus Switch state. This bit controls the state of the bus switch: 1 - Close the bus switch 0 - Do not close the bus switch |
| ST | This bit indicates whether internal self-test circuitry is active 1 - Self-test active 0 - Self-test disabled |
| U | This bit is set if the voltage at HCAP is below the threshold specified in Section 2 . Refer to Section 3.3.2 for details. |
| NV | NVM Program Enable. This bit indicates whether programming of the user-programmable OTP locations is enabled. 1 - OTP programming Enabled 0 - OTP programming Disabled |
| A[3:0] | DSI device address. This field contains the device address. |

4.2.1.15 DSI Command #14

DSI Command '1110' is not implemented. The device ignores all command formats with a command ID of '1110'.

4.2.1.16 Reverse Initialization Command

The Reverse Initialization Command is not implemented. The device ignores all command formats with a command ID of '1111'. The device ignores all command received on the BUSOUT pin.

4.3 Exception Handling

Table 59 summarizes the exception conditions detected by the device and the response for each exception.

Table 59. Exception Handling

| Condition | | Description | S | ST | U | Response |
|--|-------------------|---|---|----|---|---|
| Exception | Self-Test Request | | | | | |
| Power On Reset | N/A | Power Applied Clear Command | 1 | 1 | 0 | – Reference Section 3.6 |
| V_{REG} Under-Voltage | N/A | $V_{REG} < V_{PORCREG_f}$ | | | | – Device held in Reset. – No response to DSI commands. – Bus switch open within t_{BSOPEN} . – Device must be re-initialized when V_{REG} returns above $V_{PORCREG_f}$ |
| V_{REGA} Under-Voltage | N/A | $V_{REGA} < V_{PORCREG_f}$ | | | | – Device held in Reset. – No response to DSI commands. – Bus switch open within t_{BSOPEN} . – Device must be re-initialized when V_{REGA} returns above $V_{PORCREGA_f}$ |
| V_{HCAP} Under-Voltage Transient | Disabled | $V_{HCAP} < V_{PORCREG_f}$ for less than t_{HCAP_POR} , ST Disabled | 0 | 0 | 1 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = normal. – Device does not need to be re-initialized if V_{HCAP} returns above $V_{PORHCAP_f}$ before t_{HCAP_POR} |
| | Enabled | $V_{HCAP} < V_{PORCREG_f}$ for less than t_{HCAP_POR} , ST Enabled | 0 | 1 | 1 | – DSI Read Acceleration Data Short response = self-test data. – DSI Read Acceleration Data Long response = self-test data. – Device does not need to be re-initialized if V_{HCAP} returns above $V_{PORHCAP_f}$ before t_{HCAP_POR} |
| V_{HCAP} Under-Voltage | N/A | $V_{HCAP} < V_{PORCREG_f}$ for longer than t_{HCAP_POR} | | | | – Device is Reset and will continue to Reset every t_{HCAP_POR} until V_{HCAP} returns above $V_{PORHCAP_f}$, or an internal supply under-voltage condition occurs. – No response to DSI commands. – Bus switch open within t_{BSOPEN} . – Device must be re-initialized when V_{HCAP} returns above $V_{PORHCAP_f}$ |
| Capacitor Test Failure | N/A | | | | | – Device is Reset and will continue to be reset every $t_{POR_CAPTEST}$ until the capacitor failure is removed. – No response to DSI commands. – Bus switch open within t_{BSOPEN} . – Device must be re-initialized when capacitor failure is removed. |
| DSI Frame Timeout | N/A | $V_{BUSIN} < V_{THF}$ for longer than t_{TO} | | | | – Device is Reset and will continue to be reset every t_{TO} until the BUSIN voltage returns above V_{THF} or a supply under-voltage condition occurs. – No response to DSI commands. – Bus switch open within t_{BSOPEN} . – Device must be re-initialized when V_{BUSIN} returns above V_{THF} |
| Fuse CRC Fault (Factory Array) | Disabled | CRC failure detected in factory programmed OTP array and the LOCK_F bit is set. ST Disabled | 1 | 0 | 0 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = normal. |
| | Enabled | CRC failure detected in factory programmed OTP array and the LOCK_F bit is set. ST Enabled | 1 | 1 | 0 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = self-test data. |
| Fuse CRC Fault (User Array) | Disabled | CRC failure detected in User programmed OTP array and the LOCK_U bit is set. ST Disabled | 1 | 0 | 0 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = normal. |
| | Enabled | CRC failure detected in User programmed OTP array and the LOCK_U bit is set. ST Enabled | 1 | 1 | 0 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = self-test data. |
| Temperature Out of Range | Disabled | Temperature out of range, ST Disabled. | 1 | 0 | 0 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = normal. |
| | Enabled | Temperature out of range, ST Enabled. | 1 | 1 | 0 | – DSI Read Acceleration Data Short response = zero. – DSI Read Acceleration Data Long response = self-test data. |
| Self-Test Enabled | Enabled | ST Enabled | 1 | 1 | 0 | – Internal self-test circuitry enabled. – DSI Read Acceleration Data Short response = self-test data. – DSI Read Acceleration Data Long response = self-test data. |
| Self-Test Lockout | Disabled | 2 consecutive Disable Self-Test DSI commands received. | 0 | 0 | 0 | – Internal self-test circuitry disabled. – Enable Self-Test DSI command does not enable Self-Test. Normal response to Enable Self-Test DSI command except the ST bit is not set. – DSI Clear command or Reset disables lockout. |

5 Package

5.1 Case Outline Drawing

Reference Freescale Case Outline Drawing # 98ASA00090D

http://www.freescale.com/files/shared/doc/package_info/98ASA00090D.pdf

5.2 Recommended Footprint

Reference Freescale Application Note AN3111, latest revision:

http://www.freescale.com/files/sensors/doc/app_note/AN3111.pdf

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