



## I<sup>2</sup>C Precision Altimeter

The MPL3115A2 employs a MEMS pressure sensor with an I<sup>2</sup>C interface to provide accurate Pressure or Altitude data. The sensor Pressure and Temperature outputs are digitized by a high resolution 24-bit ADC. Internal processing removes compensation tasks from the host MCU system. Multiple user-programmable, power saving, interrupt and autonomous data acquisition modes are available, including programmed acquisition cycle timing, and poll-only modes. Typical active supply current is 40  $\mu$ A per measurement-second for a stable 30 cm output resolution. Pressure output can be resolved with output in fractions of a Pascal, and Altitude can be resolved in fractions of a meter.

The MPL3115A2 is offered in a 5 mm by 3 mm by 1.1 mm LGA package and specified for operation from -40°C to 85°C. Package is surface mount with a stainless steel lid and is RoHS compliant.

### Features

- 1.95V to 3.6V Supply Voltage, internally regulated by LDO
- 1.6V to 3.6V Digital Interface Supply Voltage
- Fully Compensated internally
- Direct Reading, Compensated
  - Pressure: 20-bit measurement (Pascals)
  - Altitude: 20-bit measurement (meters)
  - Temperature: 12-bit measurement (°Celsius)
- Programmable Events
- Autonomous Data Acquisition
- Resolution down to 1 ft. / 30 cm
- 32 Sample FIFO
- Ability to log data up to 12 days using the FIFO
- 1 second to 9 hour data acquisition rate
- I<sup>2</sup>C digital output interface (operates up to 400 kHz)

### Application Examples

- High Accuracy Altimetry
- Smartphones/Tablets
- Personal Electronics Altimetry
- GPS Dead Reckoning
- GPS Enhancement for Emergency Services
- Map Assist, Navigation
- Weather Station Equipment

## MPL3115A2

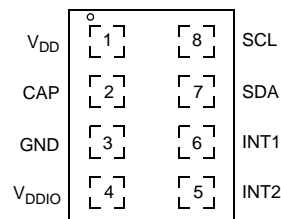
50 to 110 kPa



LGA PACKAGE

5.0 mm by 3.0 mm by 1.1 mm

### Top View



Pin Connections

### ORDERING INFORMATION

Device Name	Package Options	Case No.	# of Ports			Pressure Type			Digital Interface
			None	Single	Dual	Gauge	Differential	Absolute	
MPL3115A2	Tray	2153	•					•	•
MPL3115A2T1	Tape & Reel (1000)	2153	•					•	•

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# 1 Block Diagram and Pin Descriptions

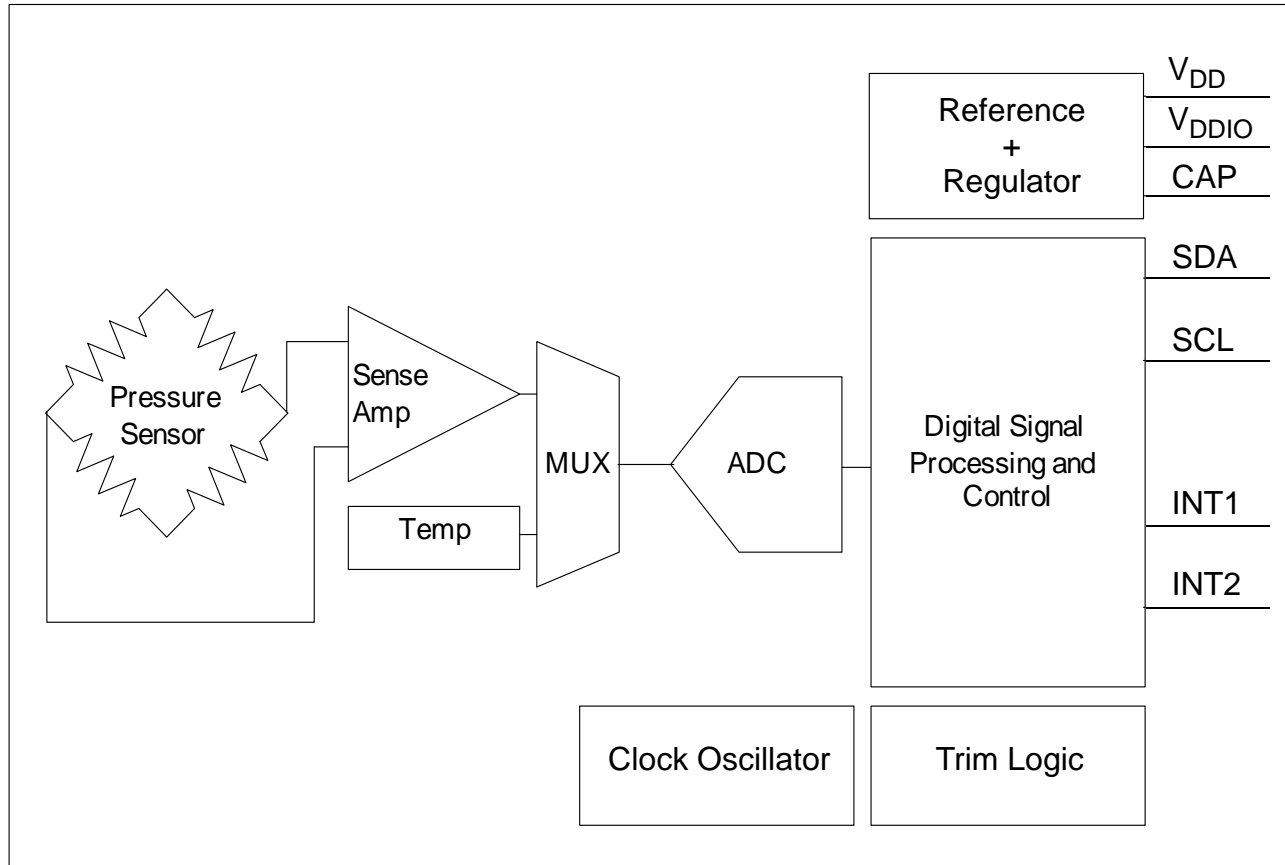
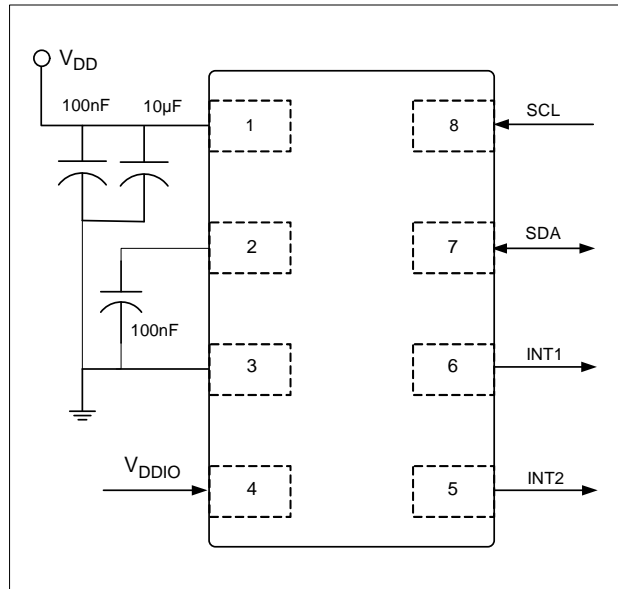


Figure 1. Block Diagram

Table 1. Pin Descriptions

Pin	Name	Function
1	V <sub>DD</sub>	V <sub>DD</sub> Power Supply Connection (1.95-3.6V)
2	CAP	External Capacitor
3	GND	Ground
4	V <sub>DDIO</sub>	Digital Interface Power Supply (1.62-3.6V)
5	INT2	Pressure Interrupt 2
6	INT1	Pressure Interrupt 1
7	SDA	I <sup>2</sup> C Serial Data
8	SCL	I <sup>2</sup> C Serial Clock



**Figure 2. Pin Connections**

The device power is supplied through the  $V_{DD}$  line. Power supply decoupling capacitors (100 nF ceramic plus 1  $\mu$ F bulk or 1  $\mu$ F ceramic) should be placed as near as possible to pin 1 of the device. A second 100 nF capacitor is used to bypass the internal regulator. The functions, threshold and the timing of the interrupt pins (INT1 and INT2) are user programmable through the I<sup>2</sup>C interface.

## 2 Mechanical and Electrical Specifications

### 2.1 Mechanical Characteristics

Table 2. Mechanical Characteristics @  $V_{DD} = 2.5V$ ,  $T = 25^{\circ}C$  unless otherwise noted<sup>(1)</sup>

Ref	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Pressure Sensor</b>							
1	$P_{FS}$	Measurement Range	Calibrated Range	50		110	kPa
			Operational Range	20		110	kPa
2		Pressure Reading Noise	1x Oversample <sup>(2)</sup>		19		Pa RMS
			128x Oversample <sup>(2)</sup>		1.5		Pa RMS
3		Pressure Absolute Accuracy	50 to 110 kPa over $0^{\circ}C$ to $50^{\circ}C$	-0.4		0.4	kPa
			50 to 110 kPa $-10^{\circ}C$ to $70^{\circ}C$		$\pm 0.4$		
4		Pressure Relative Accuracy	Relative accuracy during pressure change between 70 to 110 kPa @ at any constant Temperature between $-10^{\circ}C$ to $50^{\circ}C$		$\pm 0.05$		kPa
			Relative accuracy during changing temperature $-10^{\circ}C$ to $50^{\circ}C$ @ at any constant pressure between 50 kPa and 110 kPa		$\pm 0.1$		
5		Pressure/Altimeter Resolution <sup>(3)(4)(5)</sup>	Barometric Measurement Mode	0.25	1.5		Pa
			Altimeter Measurement Mode	0.0625	0.3		m
6		Output Data Rate	Output Data Rate in OST <sup>(6)</sup> Mode		100		Hz
			Output Data Rate of FIFO			1	Hz
<b>Temperature Sensor</b>							
7	$T_{FS}$	Measurement Range		-40		+85	$^{\circ}C$
8		Temperature Accuracy	@ $25^{\circ}C$		$\pm 1$		$^{\circ}C$
			Over Temperature Range		$\pm 3$		
9	$T_{OP}$	Operating Temperature Range		-40		+85	$^{\circ}C$
10		Board Mount Drift	After solder reflow		$\pm 0.15$		kPa
11		Long Term Drift	After a period of 1 year		$\pm 0.1$		kPa

1. Measured at  $25^{\circ}C$ , 110 kPa to 50 kPa.
2. FIFO mode used to minimize pressure reading noise vs. OST mode.
3. Smallest bit change in register represents minimum value change in Pascals or meters. Typical resolution to signify change in altitude is 0.3m.
4. At 128x Oversample Ratio.
5. Reference pressure = 101.325 kPa (Sea Level).
6. OST = One Shot Mode.

### 3 Electrical Characteristics

**Table 3. Electrical Characteristics @ VDD = 2.5V, T = 25°C unless otherwise noted.<sup>(1)</sup>**

Ref	Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
1	V <sub>DDIO</sub>	I/O Supply Voltage		1.62	1.8	3.6	V
2	V <sub>DD</sub>	Operating Supply Voltage		1.95	2.5	3.6	V
3	I <sub>DD</sub>	Integrated Current 1 update per second	Highest Speed Mode Oversample = 1		8.5		μA
4			Standard Mode Oversample = 16		40		
5			High Resolution Mode Oversample = 128		265		
6	I <sub>DDMAX</sub>	Max Current during Acquisition and Conversion	During Acquisition		2		mA
7	I <sub>DDSTBY</sub>	Supply Current Drain in STANDBY Mode	STANDBY Mode selected SBYB = 0		2		μA
8	V <sub>IH</sub>	Digital High Level Input Voltage SCL, SDA		0.75			V <sub>DDIO</sub>
9	V <sub>IL</sub>	Digital Low Level Input Voltage SCL, SDA				0.3	V <sub>DDIO</sub>
10	V <sub>OH</sub>	High Level Output Voltage INT1, INT2	I <sub>O</sub> = 500 μA	0.9			V <sub>DDIO</sub>
11	V <sub>OL</sub>	Low Level Output Voltage INT1, INT2	I <sub>O</sub> = 500 μA			0.1	V <sub>DDIO</sub>
12	V <sub>OLS</sub>	Low Level Output Voltage SDA	I <sub>O</sub> = 500 μA			0.1	V <sub>DDIO</sub>
14	T <sub>ON</sub>	Turn-on time <sup>(1)</sup>	Highest Speed Mode			60	ms
			Highest Resolution Mode			1000	
16	T <sub>OP</sub>	Operating Temperature Range		-40	25	+85	°C
<b>I<sup>2</sup>C Addressing</b>							
MPL3115A2 uses 7-bit addressing and does not acknowledge general call address 000 0000. Slave address has been set to 0x60 or 110 0000. 8-bit read is 0xC1, 8-bit write is 0xC0							

1. Time to obtain valid data from “STANDBY” mode to “ACTIVE” mode.

### 3.1 I<sup>2</sup>C Interface Characteristics

Table 4. I<sup>2</sup>C Slave Timing Values<sup>(1)</sup>

Ref	Symbol	Parameter	I <sup>2</sup> C			Unit
			Condition	Min	Max	
1	f <sub>SCL</sub>	SCL Clock Frequency	Pull-up = 1 kΩ, C <sub>b</sub> = 400 pF	0	400	KHz
2	f <sub>SCL</sub>	SCL Clock Frequency	Pull-up = 1 kΩ, C <sub>b</sub> = 20 pF	0	4	MHz
3	t <sub>BUF</sub>	Bus free time between STOP and START condition		1.3		μs
4	t <sub>HD;STA</sub>	Repeated START Hold Time		0.6		μs
5	t <sub>SU;STA</sub>	Repeated START Setup Time		0.6		μs
6	t <sub>SU;STO</sub>	STOP Condition Setup Time		0.6		μs
7	t <sub>HD;DAT</sub>	SDA Data Hold Time <sup>(2)</sup>		50 <sup>(3)</sup>	<sup>(4)</sup>	ns
8	t <sub>VD;DAT</sub>	SDA Valid Time <sup>(5)</sup>			0.9 <sup>(4)</sup>	ns
9	t <sub>VD;ACK</sub>	SDA Valid Acknowledge Time <sup>(6)</sup>			0.9 <sup>(4)</sup>	ns
10	t <sub>SU;DAT</sub>	SDA Setup Time		100 <sup>(7)</sup>		ns
11	t <sub>LOW</sub>	SCL Clock Low Time		1.3		μs
12	t <sub>HIGH</sub>	SCL Clock High Time		0.6		μs
13	t <sub>r</sub>	SDA and SCL Rise Time		20 + 0.1C <sub>b</sub> <sup>(8)</sup>	1000	ns
14	t <sub>f</sub>	SDA and SCL Fall Time <sup>(3) (6) (9) (10)</sup>		20 + 0.1C <sub>b</sub> <sup>(6)</sup>	300	ns
15	t <sub>SP</sub>	Pulse width of spikes that are suppressed by internal input filter			50	ns

1. All values referred to VIH(min) and VIL(max) levels.
2. t<sub>HD;DAT</sub> is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the VIH(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum t<sub>HD;DAT</sub> must be less than the maximum of t<sub>VD;DAT</sub> or t<sub>VD;ACK</sub> by a transition time. This device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal.
5. t<sub>VD;DAT</sub> = Time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
6. t<sub>VD;ACK</sub> = Time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
7. A fast mode I<sup>2</sup>C device can be used in a standard mode I<sup>2</sup>C system, but the requirement t<sub>SU;DAT</sub> 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t<sub>r(max)</sub> + t<sub>SU;DAT</sub> = 1000 + 250 = 1250 ns (according to the standard mode I<sup>2</sup>C specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
8. C<sub>b</sub> = Total capacitance of one bus line in pF.
9. The maximum t<sub>r</sub> for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t<sub>f</sub> is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t<sub>r</sub>.
10. In Fast Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

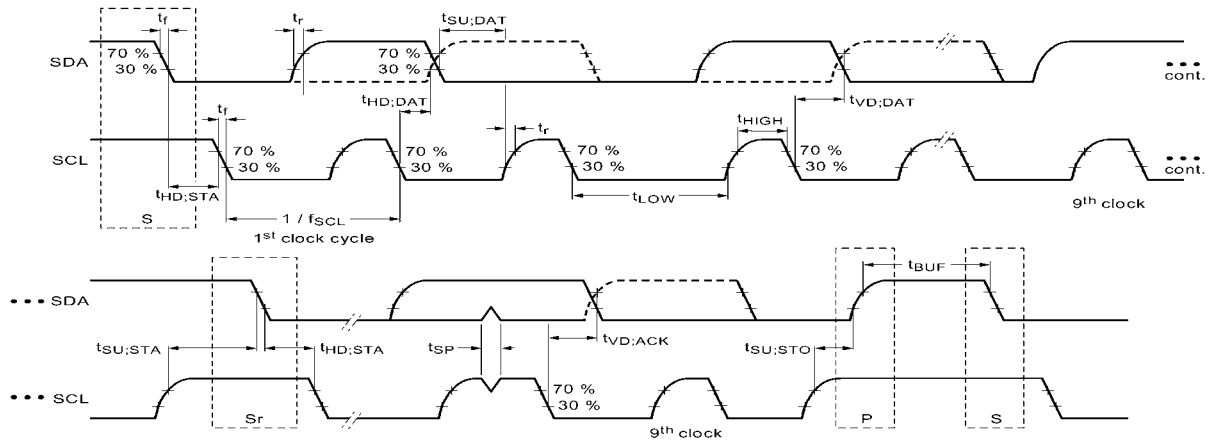


Figure 3. I<sup>2</sup>C Slave Timing Diagram

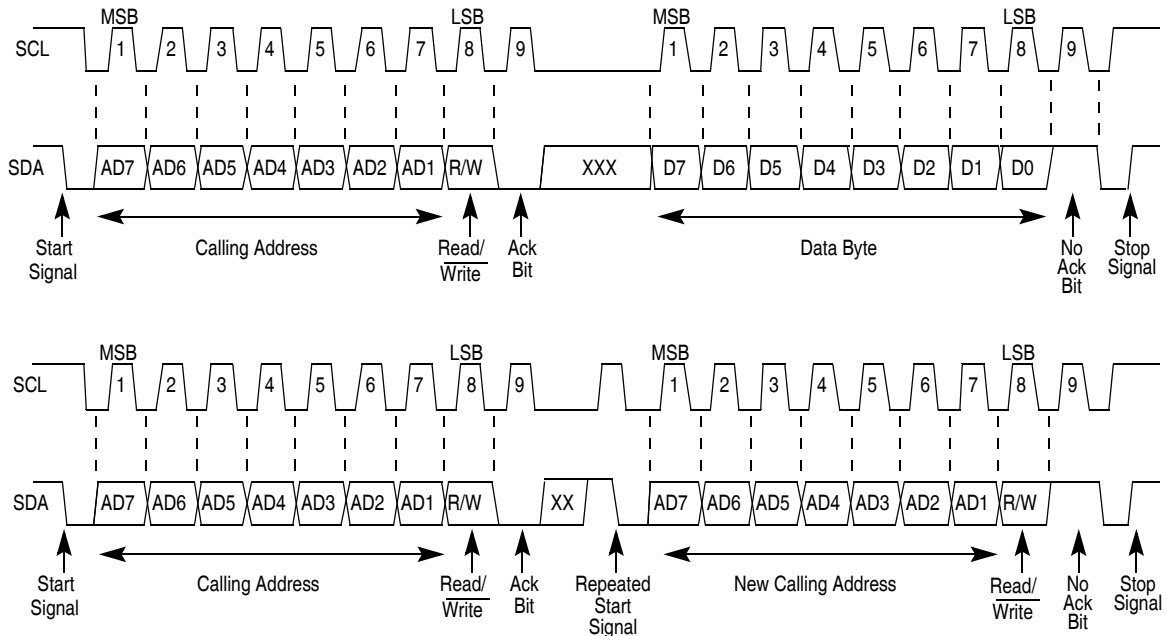


Figure 4. I<sup>2</sup>C Bus Transmission Signals

## 3.2 Absolute Maximum Ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 5. Maximum Ratings**

Characteristic	Symbol	Value	Unit
Maximum Applied Pressure	$P_{max}$	500	kPa
Supply Voltage	$V_{DD}$	-0.3 to 3.6	V
Interface Supply Voltage	$V_{DDIO}$	-0.3 to 3.6	V
Input Voltage on any Control Pin (SCL, SDA)	$V_{IN}$	-0.3 to $V_{DDIO} + 0.3$	V
Operating Temperature Range	$T_{OP}$	-40 to +85	°C
Storage Temperature Range	$T_{STG}$	-40 to +125	°C

**Table 6. ESD And Latch-up Protection Characteristics**

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latch-up Current at $T = 85^{\circ}\text{C}$	—	±100	mA



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part or cause the part to otherwise fail.



This is an ESD sensitive device, improper handling can cause permanent damage to the part.



## 4 Terminology

### 4.1 Resolution

The resolution of a pressure sensor is the minimum change of pressure that can be reliably measured. The usable resolution of the MPL3115A2 is programmable, enabling the user to choose a compromise between acquisition speed, power consumption, and resolution that best fits the application. To simplify the programming, the data is always reported in the same format with differing number of usable bits.

### 4.2 Accuracy

#### 4.2.1 Offset

An offset shift in the long term value of a pressure sensor is defined as without pressure stimulus. Offset error affects *absolute pressure* measurements but not *relative pressure* change measurements. An *absolute pressure measurement* is the pressure value in comparison to sea level. I.e. a measurement of total pressure seen (e.g 70 kPa), or total height (e.g 2000m) above sea level. A change in the offset will affect the pressure value or height seen above sea level as it shifts the sea level 'base reference'. An *absolute pressure measurement* is not the same as *relative pressure measurement*, where the pressure is compared when raising or lowering pressure in shorter intervals. This would be a walk up a hill, measuring the pressure and altitude difference from start to finish. In the relative case, the offset shifts are shared in the two absolute measurements and negate each other during the pressure calculation. For the MPL3115A2, the long term offset shift can be removed by adjusting the pressure or altitude offset correction. This adjustment is provided to override the factory programmed values to compensate for offsets introduced by manufacturing and mounting stresses. It is highly recommended that this is utilized to realize the full accuracy potential of the device.

#### 4.2.2 Linearity

Linearity compares the slope of the measurement data to that of an ideal transfer function. It refers to how well a transducer's output follows the equation  $P_{out} = P_{off} + \text{Sensitivity} \times P$  straight line equation over the operating pressure range. The method used by Freescale to give the linearity spec is the end-point straight line method measured at midrange pressure.

#### 4.2.3 Absolute Pressure

Absolute pressure sensors measure an external pressure relative to a zero-pressure reference (vacuum) sealed inside the reference chamber of the die during manufacturing. This standard allows comparison to a standard value set such that 14.7 psi = 101325 Pa = 1 atm at sea level pressure as a measurement target. The absolute pressure is used to determine altitude as it has a constant reference for comparison. Measurement at sea level can be compared to measurement at a mountain summit as they use the same vacuum reference. The conversion of absolute pressure to altitude in meters is calculated based on US Standard Atmosphere 1976 (NASA). Note that absolute pressure is not linear in nature to altitude. The compressibility of air makes this an exponential function. The value of altitude in quarter meters can be read directly from the MPL3115A2, or the value of pressure in 0.25 Pascal (Pa) units.

#### 4.2.4 Span

Span is the value of full scale output with offset subtracted, representing the full range of the pressure sensor. Ideally the span is a specification over a constant temperature. The MPL3115A2 uses internal temperature compensation to remove drift. Span accuracy is the comparison of the measured difference and the actual difference between the highest and lowest pressures in the specified range.

### 4.3 Pressure/Altitude

The MPL3115A2 device is a high accuracy pressure sensor with integrated data calculation and logging capabilities. The altitude calculations are based on the measured pressure, the user input of the equivalent sea level pressure (to compensate for local weather conditions) and the US Standard Atmosphere 1976 (NASA) to give the altitude readings. Pressure is given in Pascals (Pa), and fractions of a Pa. Altitude is given in meters (m) and fractions of a meter. The altitude is calculated from the pressure using the equation below:

$$h = 44330.77 \{ 1 - (p/p_0)^{0.1902632} \} + \text{OFF\_P (Register Value)}$$

Where  $p_0$  = sea level pressure (101325 Pa) and  $h$  is in meters.

## 4.4 Power Modes of Operation

### 4.4.1 Off

Unit is powered down and has no operating functionality.  $V_{DD}$  and  $V_{DDIO}$  are not powered.

### 4.4.2 STANDBY

The digital sections are operational and the unit is capable of receiving commands and delivering stored data. The analog sections are off. The part is waiting for CTRL\_REG1 to be configured and the part to enter active.

### 4.4.3 ACTIVE

Both analog and digital sections are running. The unit is capable of gathering new data, and accepting commands. MPL3115A2 is fully functional.

**Table 7. Mode of Operation Description**

Mode	I <sup>2</sup> C Bus State	VDD		Function Description
OFF	Powered Down	< 1.62V	< VDD + 0.3V	Device is powered off.
STANDBY	I <sup>2</sup> C Communication with device is possible	ON	STANDBY Register Set	Only POR and digital blocks are enabled. Analog subsystem is disabled.
ACTIVE	I <sup>2</sup> C Communication with device is possible	ON	STANDBY Register Cleared	All blocks are enabled (POR, digital, analog).

## 5 Functionality

The device is a low-power, high accuracy digital output altimeter, barometer and thermometer, packaged in a 3 x 5 x 1.1 mm form factor. The complete device includes a sensing element, analog and digital signal processing and an IC interface able to take the information from the sensing element and to provide a signal to the host through an I<sup>2</sup>C serial interface.

The device has two operational modes, one being barometer/pressure sensor and the other, an altimeter. Both modes include a thermometer temperature output function.

Balancing power consumption and sensitivity is programmable where the data oversampling ratio can be set to balance current consumption and noise/resolution. Serial Interface Communications is through an I<sup>2</sup>C interface thus making the device particularly suitable for direct interfacing with a microcontroller. The device features two independently programmable interrupt signals which can be set to signal when a new set of measured Pressure and Temperature data is available, simplifying data acquisition in the digital system that uses the device. The device may also be configured to generate an interrupt signal when to a user programmed set of conditions are met. Examples are: Interrupt can be triggered when a single new data acquisition is ready, when a desired number of samples are stored within the internal FIFO or when a change of Pressure or Temperature is detected.

In RAW mode, the FIFO must be disabled and all other functionality: Alarms, Deltas and other interrupts are disabled.

### 5.1 Factory Calibration

The device is factory calibrated for sensitivity, offset for both Temperature and Pressure measurements. Trim values are stored, on-chip, in Non-Volatile Memory (NVM). In normal use, further calibration is not necessary; however, in order to realize the highest possible accuracy, the device allows the user to override the factory set offset values after power-up. The user adjustments are stored in volatile registers. The factory calibration values are not affected, and are always used by default on power-up.

### 5.2 Barometer/Altitude Function

The mode of operation of the device can be selected as Pressure or Altitude. The internal sensor gives an absolute pressure signal. The absolute pressure signal is processed to provide a scaled pressure or an altitude, depending on the mode selected. The combination of a high performance sensor and the signal processing enable resolution of pressures below 1 Pa and altitude resolution of better than 1 Ft / 0.3m at sea level.

When in Pressure mode, all pressure related data is reported as 20-bit 2's complement data in Pascals. When in Altitude mode, all pressure data is converted to equivalent altitude, based on the US standard atmosphere and then stored as meters and fractions of a meter values.

## 5.2.1 Barometric Input

In order to accurately determine the altitude by pressure, facility is provided to input in the local barometric pressure correction. Default value is the standard atmospheric pressure value of 101,325 Pa.

## 5.3 Temperature Function

The unit contains a high resolution temperature sensor that provides data to the user via a 16-bit data register, as well as for internal compensation of the pressure sensor.

## 5.4 Autonomous Data Acquisition

The unit can be programmed to periodically capture Altitude/Pressure and Temperature data. Up to 32 data acquisitions can be stored in the internal FIFO. The interval between acquisitions is programmable from 1 second to 9 hours.

Data: (Up to 32 samples over 12 days). The unit can also be programmed to make a single reading and then go to standby mode.

## 5.5 FIFO

A 32 sample FIFO is incorporated to minimize the overhead of collecting multiple data samples. The FIFO stores both Temperature and Pressure/Altitude data. The device can be programmed to autonomously collect data at programmed intervals and store the data in the FIFO. FIFO interrupts can be triggered by watermark full or data contention (FIFO GATE) events.

## 5.6 External Interrupts

Two independent interrupt out pins are provided. The configuration of the pins are programmable (polarity, open drain or push-pull.) Any one of the internal interrupt sources can be routed to either pin.

### 5.6.1 Reach Target Threshold Pressure/Altitude

The interrupt flag is set on reaching the value stored in the Altitude target register. Additionally, a window value provides the ability to signal when the target is nearing from either above or below the value in the Altitude target register. When in barometer mode, these values represent pressures rather than altitudes.

Examples:

- Set Altitude alert to 3000m and window value to 100m, interrupt is asserted passing 2900m, 3000m, and 3100m.
- Set Pressure alert to 100.0 kPa and window value to 5 kPa, interrupt can be sent passing 95 kPa, 100 kPa and 105 kPa.

### 5.6.2 Reach Window Target Pressure Altitude

The interrupt flag is set when the temperature value is within the window defined by the following formula:

$$\text{Window} = P\_TGT_{\text{MSB,LSB}} \pm P\_WND_{\text{MSB,LSB}}$$

### 5.6.3 Reach Target Threshold Temperature

Interrupt flag is set on reaching the value stored in the Temperature target register. Additionally a window value provides ability to signal when the target is nearing from either above or below the value in the Temperature target register.

### 5.6.4 Reach Window Target Temperature

The interrupt flag is set when the temperature value is within the window defined by the following formula:

$$\text{Window} = T\_TGT \pm T\_WND$$

### 5.6.5 Pressure/Altitude Change

Interrupt flag is set if sequential Pressure/Altitude acquisitions exceed value stored in window value register.

### 5.6.6 Temperature Change

Interrupt flag is set if sequential Temperature acquisitions exceed the value stored in window value register.

## 5.7 Pressure/Altitude Change

Register shows change from last Pressure/Altitude sample.

## 5.8 Min/Max Data Value Storage

Registers record the minimum Pressure/Altitude and Temperature.

## 5.9 Digital Interface

The registers embedded inside the device are accessed through an I<sup>2</sup>C serial interface.

**Table 8. Serial Interface Pin Descriptions**

Name	Description
SCL	I <sup>2</sup> C Serial Clock
SDA	I <sup>2</sup> C Serial Data

There are two signals associated with the I<sup>2</sup>C bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pull-up resistors connected to V<sub>DD</sub> are expected for SDA and SCL. When the bus is free both the lines are high. The I<sup>2</sup>C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I<sup>2</sup>C standards

### 5.9.1 I<sup>2</sup>C Operation

The transaction on the bus is started through a start condition (START) signal. START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After START has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after START contains the slave address in the first 7 bits, and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master. The ninth clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If the master can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the master is ready for another byte and releases the clock line.

A low to high transition on the SDA line while the SCL line is high is defined as a stop condition (STOP). A data transfer is always terminated by a STOP. A master may also issue a repeated START during a data transfer. Device expects repeated STARTs to be used to randomly read from specific registers.

The standard 7-bit I<sup>2</sup>C slave address is 0x60 or 1100000. 8-bit read is 0xC1, 8-bit write is 0xC0.

Consult factory for alternate addresses.

## 6 Register Descriptions

Table 9. Register Address Map

Register Address	Name	Reset	Reset when STBY to Active	Type	Auto-Increment Address		Comment	
0x00	Sensor Status Register (STATUS) <sup>(1)(2)</sup>	0x00	Yes	R	0x01		Alias for DR_STATUS or F_STATUS	
0x01	Pressure Data Out MSB (OUT_P_MSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x02	0x01	Bits 12-19 of 20-bit real-time Pressure sample.	Root pointer to Pressure and Temperature FIFO data.
0x02	Pressure Data Out CSB (OUT_P_CSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x03		Bits 4-11 of 20-bit real-time Pressure sample	
0x03	Pressure Data Out LSB (OUT_P_LSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x04		Bits 0-3 of 20-bit real-time Pressure sample	
0x04	Temperature Data Out MSB (OUT_T_MSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x05		Bits 4-11 of 12-bit real-time Temperature sample	
0x05	Temperature Data Out LSB (OUT_T_LSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x00		Bits 1-3 of 12-bit real-time Temperature sample	
0x00/0x06	Sensor Status Register (DR_STATUS) <sup>(1)(2)</sup>	0x00	Yes	R	0x07		Data Ready status information	
0x07	Pressure Data Out Delta MSB (OUT_P_DELTA_MSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x08		Bits 12-19 of 20-bit Pressure change data	
0x08	Pressure Data Out Delta CSB (OUT_P_DELTA_CSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x09		Bits 4-11 of 20-bit Pressure change data	
0x09	Pressure Data Out Delta LSB (OUT_P_DELTA_LSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x0A		Bits 0-3 of 20-bit Pressure change data	
0x0A	Temperature Data Out Delta MSB (OUT_T_DELTA_MSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x0B		Bits 4-11 of 12-bit Temperature change data	
0x0B	Temperature Data Out Delta LSB (OUT_T_DELTA_LSB) <sup>(1)(2)</sup>	0x00	Yes	R	0x06		Bits 0-3 of 12-bit Temperature change data	
0x0C	Device Identification Register (WHO_AM_I)	0xC4	No	R	0x0D		Fixed Device ID Number	
0x0D/00	FIFO Status Register (F_STATUS) <sup>(1)(2)</sup>	0x00	Yes	R	0x0E		FIFO Status: No FIFO event detected	
0x0E/01	FIFO 8-bit Data Access (F_DATA)	0x00	Yes	R	0x0E		FIFO 8-bit data access	
0x0F	FIFO Setup Register (F_SETUP) <sup>(1)(3)</sup>	0x00	Yes	R/W	0x10		FIFO setup	
0x10	Time Delay Register (TIME_DLY) <sup>(1)(2)</sup>	0x00	Yes	R	0x11		Time since FIFO overflow	
0x11	System Mode Register (SYSMOD)	0x00	Yes	R	0x12		Current system mode	
0x12	Interrupt Source Register (INT_SOURCE) <sup>(1)</sup>	0x00	No	R	0x13		Interrupt status	
0x13	PT Data Configuration Register (PT_DATA_CFG) <sup>(1)(3)</sup>	0x00	No	R/W	0x14		Data event flag configuration	
0x14	BAR Input in MSB (BAR_IN_MSB) <sup>(1)(3)</sup>	0xC5	No	R/W	0x15		Barometer input for Altitude calculation bits 8-15	
0x15	BAR Input in LSB (BAR_IN_LSB) <sup>(1)(3)</sup>	0xE7	No	R/W	0x16		Barometer input for Altitude calculation bits 0-7	

**Table 9. Register Address Map**

0x16	Pressure Target MSB (P_TGT_MSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x17	Pressure/Altitude target value bits 8-15
0x17	Pressure Target LSB (P_TGT_LSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x18	Pressure/Altitude target value bits 0-7
0x18	Temperature Target (T_TGT) <sup>(1)(3)</sup>	0x00	No	R/W	0x19	Temperature target value
0x19	Pressure/Altitude Window MSB (P_WND_MSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x1A	Pressure/Altitude window value bits 8-15
0x1A	Pressure/Altitude Window LSB (P_WND_LSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x1B	Pressure/Altitude window value bits 0-7
0x1B	Temperature Window (T_WND) <sup>(1)(3)</sup>	0x00	No	R/W	0x1C	Temperature window value
0x1C	Minimum Pressure Data Out MSB (P_MIN_MSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x1D	Minimum Pressure/Altitude bits 12-19
0x1D	Minimum Pressure Data Out CSB (P_MIN_CSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x1E	Minimum Pressure/Altitude bits 4-11
0x1E	Minimum Pressure Data Out LSB (P_MIN_LSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x1F	Minimum Pressure/Altitude bits 0-3
0x1F	Minimum Temperature Data Out MSB (T_MIN_MSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x20	Minimum Temperature bits 8-15
0x20	Minimum Temperature Data Out LSB (T_MIN_LSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x21	Minimum Temperature bits 0-7
0x21	Maximum Pressure Data Out MSB (P_MAX_MSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x22	Maximum Pressure/Altitude bits 12-19
0x22	Maximum Pressure Data Out CSB (P_MAX_CSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x23	Maximum Pressure/Altitude bits 4-11
0x23	Maximum Pressure Data Out LSB (P_MAX_LSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x24	Maximum Pressure/Altitude bits 0-3
0x24	Maximum Temperature Data Out MSB (T_MAX_MSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x25	Maximum Temperature bits 8-15
0x25	Maximum Temperature Data Out LSB (T_MAX_LSB) <sup>(1)(3)</sup>	0x00	No	R/W	0x26	Maximum Temperature bits 0-7
0x26	Control Register 1 (CTRL_REG1) <sup>(1)(4)</sup>	0x00	No	R/W	0x27	Modes, Oversampling
0x27	Control Register 2 (CTRL_REG2) <sup>(1)(4)</sup>	0x00	No	R/W	0x28	Acquisition time step
0x28	Control Register 3 (CTRL_REG3) <sup>(1)(4)</sup>	0x00	No	R/W	0x29	Interrupt pin configuration
0x29	Control Register 4 (CTRL_REG4) <sup>(1)(4)</sup>	0x00	No	R/W	0x2A	Interrupt enables
0x2A	Control Register 5 (CTRL_REG5) <sup>(1)(4)</sup>	0x00	No	R/W	0x2B	Interrupt output pin assignment
0x2B	Pressure Data User Offset Register (OFF_P)	0x00	No	R/W	0x2C	Pressure data offset
0x2C	Temperature Data User Offset Register (OFF_T)	0x00	No	R/W	0x2D	Temperature data offset
0x2D	Altitude Data User Offset Register (OFF_H)	0x00	No	R/W	0x0C	Altitude data offset

1. Register contents are preserved when transitioning from "ACTIVE" to "STANDBY" mode.
2. Register contents are reset when transitioning from "STANDBY" to "ACTIVE" mode.
3. Register contents can be modified anytime in "STANDBY" or "ACTIVE" mode.
4. Modification of this register's contents can only occur when device in "STANDBY" mode except the SBYB and RST bit fields in CTRL\_REG1 register.

**Table 10. Register Address Map with FIFO Modes<sup>(1)</sup>**

Register Address	Name	Reset Value	Reset when STANDBY to ACTIVE	Type	Auto-Increment Address		Comment	
<b>Registers: Area A (F_Mode = 0, FIFO disabled)</b>								
<b>0x00/0x06</b>	Sensor Status Register ( <b>DR_STATUS</b> )	0x00	Yes	R	0x01		DR_STATUS	
<b>0x01</b>	Pressure Data Out MSB ( <b>OUT_P_MSB</b> )	0x00	Yes	R	0x02	0x01	Bits 12-19 of 20-bit real-time Pressure sample.	Root pointer to Pressure and Temperature FIFO data.
<b>0x02</b>	Pressure Data Out CSB ( <b>OUT_P_CSB</b> )	0x00	Yes	R	0x03		Bits 4-11 of 20-bit real-time Pressure sample	
<b>0x03</b>	Pressure Data Out LSB ( <b>OUT_P_LSB</b> )	0x00	Yes	R	0x04		Bits 0-3 of 20-bit real-time Pressure sample	
<b>0x04</b>	Temperature Data Out MSB ( <b>OUT_T_MSB</b> )	0x00	Yes	R	0x05		Bits 4-11 of 12-bit real-time Temperature sample	
<b>0x05</b>	Temperature Data Out LSB ( <b>OUT_T_LSB</b> )	0x00	Yes	R	0x00		Bits 0-3 of 12-bit real-time Temperature sample	
<b>Registers: Area A (F_Mode &gt; 0, FIFO in circular buffer or full stop mode)</b>								
<b>0x00/0x0D</b>	Sensor Status Register ( <b>F_STATUS</b> )	0x00	Yes	R	0x01		F_STATUS	
<b>0x01</b>	FIFO 8-bit Data Access ( <b>F_DATA</b> )	0x00	Yes	R	0x01		0x01	
<b>0x02</b>	Read to Reserved Area returns 00	0x00	N/A	—	0x03		—	
<b>0x03</b>	Read to Reserved Area returns 00	0x00	N/A	—	0x04		—	
<b>0x04</b>	Read to Reserved Area returns 00	0x00	N/A	—	0x05		—	
<b>0x05</b>	Read to Reserved Area returns 00	0x00	N/A	—	0x00		—	

- The Registers in Area A from 0x00 to 0x05 depend on the F\_MODE bit setting in FIFO Setup Register (F\_SETUP).  
 F\_MODE = 0, FIFO is disabled.  
 F\_MODE = 2'b01 is circular buffer.  
 F\_MODE = 2'b10 is full stop mode.

## 6.1 Sensor Status

### 6.1.1 Status (0x00)

**Table 11. Alias for DR\_Status (0x06) or F\_Status (0x0B)**

FIFO Data Enabled Mode Bit Setting	
F_MODE = 00 <sup>(1)</sup>	0x00 = DR_STATUS (0x06)
F_MODE > 00	0x00 = F_STATUS (0x0D)

- The F\_MODE is defined in Section 6.3.3

The aliases allow the STATUS register to be read easily before reading the current real-time data or the FIFO contents using register address auto-incrementing mechanism.

### 6.1.2 DR\_STATUS (0x06)

The STATUS register provides the acquisition status information on a per sample basis, and reflects real-time updates to the OUT\_P and OUT\_T registers

The same STATUS register can be read through an alternate address. The alias allows the STATUS register to be read easily before reading the current Pressure and Temperature data and delta Pressure and Temperature data or FIFO sample data using register address auto-incrementing mechanism.

### 6.1.2.1 Data Registers w/F\_MODE = 00 (FIFO Disabled)

When the FIFO subsystem data output register driver is disabled (F\_MODE = 00), the register indicates the real-time status information of the sample data.

**Table 12. DR\_STATUS Register**

	7	6	5	4	3	2	1	0
R	PTOW	POW	TOW	0	PTDR	PDR	TDR	0
W								
Reset	0	0	0	0	0	0	0	0

**Table 13. DR\_STATUS Bit Descriptions**

Name	Description
PTOW	Pressure/Altitude OR Temperature data overwrite. PTOW is set to 1 whenever new data is acquired before completing the retrieval of the previous set. This event occurs when the content of at least one data register (i.e. OUT_P, OUT_T) has been overwritten. PTOW is cleared when the high-bytes of the data (OUT_P_MSB or OUT_T_MSB) are read, when F_MODE is zero. PTOW is cleared by reading F_DATA register when F_MODE > 0. Default value: 0 0: No data overwrite has occurred 1: Previous Pressure/Temperature data was overwritten by new Pressure/Temperature data before it was read
POW	Pressure/Altitude data overwrite. POW is set to 1 whenever a new Pressure acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. POW is cleared anytime OUT_P_MSB register is read., F_MODE is zero. POW is cleared by reading F_DATA register when F_MODE > 0. Default value: 0 0: No data overwrite has occurred 1: Previous Pressure data was overwritten by new Pressure data before it was read
TOW	Temperature overwrite. TOW is set to 1 whenever a new Temperature acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. TOW is cleared anytime OUT_T_MSB register is read, when F_MODE is zero. TOW is cleared by reading F_DATA register when F_MODE > 0. Default value: 0 0: No data overwrite has occurred 1: Previous Temperature data was overwritten by new Temperature data before it was read
PTDR	Pressure/Altitude OR Temperature data ready. PTDR signals that a new acquisition for either Pressure or Temperature channels is available. PTDR is cleared anytime OUT_P_MSB or OUT_T_MSB register is read, when F_MODE is zero. PTDR is cleared by reading F_DATA register when F_MODE > 0. Default value: 0 0: No new set of data ready 1: A new set of data is ready
PDR	Pressure/Altitude new data available. PDR is set to 1 whenever a new Pressure data acquisition is completed, PDR is cleared anytime OUT_P_MSB register is read. PDR is cleared anytime OUT_P_MSB register is read, when F_MODE is zero. PDR is cleared by reading F_DATA register when F_MODE > 0. 0: No new Pressure data is available 1: A new set of Pressure data is ready
TDR	Temperature new Data Available. TDR is set to 1 whenever a Temperature data acquisition is completed. TDR is cleared anytime OUT_T_MSB register is read, when F_MODE is zero. TDR is cleared by reading F_DATA register when F_MODE > 0. 0: No new Temperature data ready 1: A new Temperature data is ready

**PDR** and **POW** flag generation is required for the Pressure event flag generator to be enabled (PDEFE = 1) in the PT Data Configuration Register (PT\_DATA\_CFG).

**TDR** and **TOW** flag generation is required for the Temperature event flag generator to be enabled (TDEFE = 1) in the PT Data Configuration Register (PT\_DATA\_CFG).

**PTDR** and **PTOW** flag generation requires the DREM event flag generator to be enabled in the PT Data Configuration Register (PT\_DATA\_CFG).



### 6.1.3 OUT\_P\_MSB (0x01), OUT\_P\_CSB (0x02), OUT\_P\_LSB (0x03), OUT\_T\_MSB (0x04), OUT\_T\_LSB (0x05)

Altitude 20-bit sample data and Temperature 12-bit sample data are expressed as 2's complement numbers. If RAW is selected, then the RAW value is stored in all 24 bits of OUT\_P\_MSB, OUT\_P\_CSB and OUT\_P\_LSB.

The Altitude data is arranged as 20-bit 2's complement value in meters. The data is stored as meters with the 16 bits of OUT\_P\_MSB and OUT\_P\_CSB and with fractions of a meter stored in bits 7-4 of OUT\_P\_LSB. Be aware that the fractional bits are not signed, therefore, they are not represented in 2's complement.

The Pressure is arranged as 20-bit data in Pascals. The first 18 bits are located in OUT\_P\_MSB, OUT\_P\_CSB and bits 7-6 of OUT\_P\_LSB. The 2 bits in position 5-4 of OUT\_P\_LSB represent the fractional component. Be aware that the fractional bits are not signed, therefore, they are not represented in 2's complement.

The Temperature data is arranged as 12-bit 2's complement value in degrees C. The 8 bits of OUT\_T\_MSB representing degrees and with fractions of a degree are stored in 4 bits in position 7-4 of OUT\_T\_LSB. Be aware that the fractional bits are not signed, therefore, they are not represented in 2's complement. If RAW is selected then the RAW value is stored in all 16 bits of OUT\_T\_MSB and OUT\_T\_LSB.

The sample data output registers store the current sample data if the FIFO data output register driver is disabled, but if the FIFO data output register driver is enabled, the sample data output registers point to the head of the FIFO buffer which contains the previous Pressure and Temperature data samples.

#### 6.1.3.1 Data Registers with F\_MODE = 00

The DR\_STATUS register, OUT\_P\_MSB, OUT\_P\_CSB, OUT\_P\_LSB, OUT\_T\_MSB, and OUT\_T\_LSB are stored in the auto-incrementing address range of 0x01 to 0x06 to reduce reading the status followed by 20-bit Pressure and 12-bit Temperature data to 6 bytes.

**Table 14. OUT\_P\_MSB Register**

	7	6	5	4	3	2	1	0
R	PD19	PD18	PD17	PD16	PD15	PD14	PD13	PD12
W								
Reset	0	0	0	0	0	0	0	0

**Table 15. OUT\_P\_CSB Register**

	7	6	5	4	3	2	1	0
R	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4
W								
Reset	0	0	0	0	0	0	0	0

**Table 16. OUT\_P\_LSB Register**

	7	6	5	4	3	2	1	0
R	PD3	PD2	PD1	PD0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

**Table 17. OUT\_T\_MSB Register**

	7	6	5	4	3	2	1	0
R	TD11	TD10	TD9	TD8	TD7	TD6	TD5	TD4
W								
Reset	0	0	0	0	0	0	0	0

**Table 18. OUT\_T\_LSB Register**

	7	6	5	4	3	2	1	0
R	TD3	TD2	TD1	TD0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

If the FIFO data output register driver is enabled (F\_MODE > 00), register 0x01 points to the FIFO read pointer, while registers 0x02, 0x03, 0x04, 0x05, return a value of zero when read.

### 6.1.4 OUT\_P\_DELTA\_MSB (0x07), OUT\_P\_DELTA\_CSB (0x08), OUT\_P\_DELTA\_LSB (0x09), OUT\_T\_DELTA\_MSB (0x0A), OUT\_T\_DELTA\_LSB (0x0B)

Differences from last Pressure/Altitude and Temperature samples output data expressed as 2's complement numbers.

The Altitude data is arranged as 20-bit 2's complement value in meters. Stored as meters with the 16 bits of OUT\_P\_DELTA\_MSB and OUT\_P\_DELTA\_CSB and with fractions of a meter stored in 4 bits in position 7-4 of OUT\_P\_DELTA\_LSB.

The Pressure is arranged as 20-bit data in Pascals. The first 18 bits are located in OUT\_P\_DELTA\_MSB, OUT\_P\_DELTA\_CSB and bits 7-6 of OUT\_P\_DELTA\_LSB. The 2 bits in position 5-4 of OUT\_P\_DELTA\_LSB represent the fractional component.

The Temperature data is arranged as 12-bit 2's complement value in degrees C. The 8 bits of OUT\_DELTA\_T\_DELTA\_MSB representing degrees and with fractions of a degree stored in 4 bits in position 7-4 of OUT\_DELTA\_T\_DELTA\_LSB.

In RAW mode, these values are calculated based on un-scaled value

**Note:** The OUT\_P\_DELTA\_LSB, OUT\_P\_DELTA\_MSB, OUT\_T\_DELTA registers store the difference data information regardless of the state of the FIFO data output register driver bit, F\_MODE > 00.

**Table 19. OUT\_P\_DELTA\_MSB Register**

	7	6	5	4	3	2	1	0
R	PDD19	PDD18	PDD17	PDD16	PDD15	PDD14	PDD13	PDD12
W								
Reset	0	0	0	0	0	0	0	0

**Table 20. OUT\_P\_DELTA\_CSB Register**

	7	6	5	4	3	2	1	0
R	PDD11	PDD10	PDD9	PDD8	PDD7	PDD6	PDD5	PDD4
W								
Reset	0	0	0	0	0	0	0	0

**Table 21. OUT\_P\_DELTA\_LSB Register**

	7	6	5	4	3	2	1	0
R	TDD3	TDD2	TDD1	TDD0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

**Table 22. OUT\_T\_DELTA\_MSB Register**

	7	6	5	4	3	2	1	0
R	TDD11	TDD10	TDD9	TDD8	TDD7	TDD6	TDD5	TDD4
W								
Reset	0	0	0	0	0	0	0	0

**Table 23. OUT\_T\_DELTA\_LSB Register**

	7	6	5	4	3	2	1	0
R	TDD3	TDD2	TDD1	TDD0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

## 6.2 Device ID

### 6.2.1 WHO\_AM\_I (0x0C)

Device identification register. This register contains the device identifier which is set to 0xC4 by default. The value is factory programmed. Consult factory for custom alternate values.

**Table 24. WHO\_AM\_I Register**

	7	6	5	4	3	2	1	0
R								
W								
Reset	(NVM data)	(NVM data)	(NVM data)	(NVM data)	(NVM data)	(NVM data)	(NVM data)	(NVM data)
	1	1	0	0	0	1	0	0

## 6.3 FIFO Setup

### 6.3.1 F\_STATUS (0x0D)

If the FIFO subsystem data output register driver is enabled, the status register indicates the current status information of the FIFO subsystem.

**Table 25. F\_STATUS**

	7	6	5	4	3	2	1	0
R	F_OVF	F_WMRK_FLAG	F_CNT5	F_CNT4	F_CNT3	F_CNT2	F_CNT1	F_CNT0
W								
Reset	0	0	0	0	0	0	0	0

**Table 26. FIFO Flag Event Descriptions**

F_OVF	F_WMRK_FLAG	Event Description
0	—	No FIFO overflow events detected.
1	—	FIFO overflow event detected.
—	0	No FIFO watermark events detected.
—	1	FIFO watermark event detected. FIFO sample count greater than watermark value.

The F\_OVF and F\_WMRK\_FLAG flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit flag in the interrupt source register (INT\_SOURCE) by reading the F\_STATUS register. Therefore the F\_OVF bit flag will remain asserted while the FIFO has overflowed and the F\_WMRK\_FLAG bit flag will remain asserted while the F\_CNT value is greater than then F\_WMRK value.

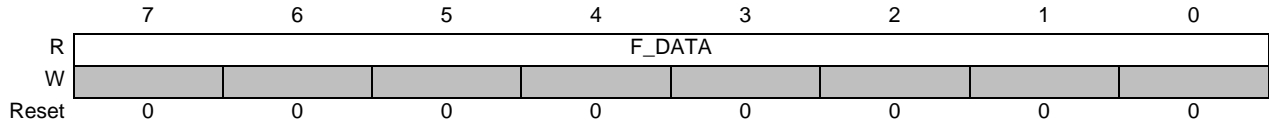
**Table 27. FIFO Sample Count Bit Descriptions**

Name	Description
F_CNT[5:0]	FIFO sample counter. F_CNT[5:0] bits indicate the number of samples currently stored in the FIFO buffer. Count 000000 indicates that the FIFO is empty. Default value: 00_0000. (000001 to 100000 indicates 1 to 32 samples stored in FIFO)

### 6.3.2 F\_DATA (0x0E)

F\_DATA is a read only address which provides access to 8-bit FIFO data. FIFO holds a maximum of 32 samples; a maximum of  $5 \times 32 = 160$  data bytes of samples can be read. When F\_MODE bit in FIFO SETUP (F\_SETUP) register is set to logic “1”, the F\_DATA pointer shares the same address location as OUT\_P\_MSB (0x01); therefore all accesses of the FIFO buffer data use the I<sup>2</sup>C address 0x01. Reads from the other data registers (0x02, 0x03, 0x04, 0x05) will return a value of 0x00. **Note:** The FIFO will **NOT** suspend to accumulate data during accessed to FIFO 8-bit data access (F\_DATA).

**Table 28. F\_DATA 8-bit Data Access Register**



**Table 29. Read Accesses through F\_DATA**

1 <sup>st</sup> read	OUT_P_MSB (oldest)
2 <sup>nd</sup> read	OUT_P_CSB (oldest)
3 <sup>rd</sup> read	OUT_P_LSB (oldest)
4 <sup>th</sup> read	OUT_T_MSB (oldest)
5 <sup>th</sup> read	OUT_T_LSB (oldest)
.	.
.	.
	OUT_T_MSB (oldest)
	0x00
	0x00

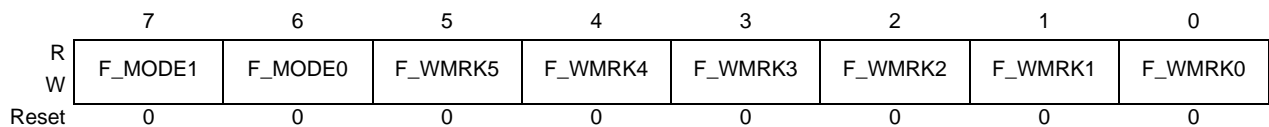
### 6.3.3 F\_SETUP (0x0F)

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data.

The FIFO update rate is dictated by the selected system acquisition rate.

When a byte is read from the FIFO buffer the oldest sample data in the FIFO buffer is returned and also deleted from the front of the FIFO buffer, while the FIFO sample count is decremented by one. It is assumed that the host application shall use the I<sup>2</sup>C BURST read transaction to dump the FIFO.

**Table 30. F\_SETUP Register**



**Table 31. F\_SETUP Bit Descriptions**

Name	Description
F_MODE[1:0] <sup>(1)(2)(3)</sup>	<p>FIFO buffer overflow mode. Default value: 0  <b>00:</b> FIFO is disabled  <b>01:</b> FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample  <b>10:</b> FIFO stops accepting new samples when overflowed  <b>11:</b> Not Used</p> <p>The FIFO is flushed whenever the FIFO is disabled, or transitioning from “STANDBY” mode to “ACTIVE” mode. Disabling the FIFO (F_MODE = 00) resets the F_OVF, F_WMRK_FLAG, F_CNT to zero.            A FIFO overflow event (i.e. F_CNT = 32) will assert the F_OVF flag and a FIFO sample count equal to the sample count watermark (i.e. F_WMRK) asserts the F_WMRK_FLAG event flag.</p>

**Table 31. F\_SETUP Bit Descriptions**

F_WMRK[5:0] <sup>(2)</sup>	FIFO Event Sample Count Watermark. Default value: 00_0000. These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag (F_WMK_FLAG) is raised when FIFO sample count F_CNT[5:0] value is equal to the F_WMRK[5:0] watermark. Setting the F_WMRK[5:0] to 00_0000 will disable the FIFO watermark event flag generation.
----------------------------	-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

1. This bit field can be written in ACTIVE mode.
2. This bit field can be written in STANDBY mode.
3. The FIFO mode (F\_MODE) cannot be switched between the two operational modes (01 & 10).

## 6.4 Time Delay Register

### 6.4.1 TIME\_DLY(0x10)

The time delay register contains the number of ticks of data sample time since the last byte of the FIFO was written. Starts increment on FIFO overflow or data wrap and clears when last byte of FIFO is read.

**Table 32. Time Delay Register**

	7	6	5	4	3	2	1	0
R	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
W								
Reset	0	0	0	0	0	0	0	0

## 6.5 System Mode Register

### 6.5.1 SYSMOD (0x11)

The system mode register indicates the current device operating mode. The System mode register also indicates the status of the NVM parity error and FIFO gate error flags.

**Table 33. SYSMOD Register**

	7	6	5	4	3	2	1	0
R	0		0	0	0	0	0	SYSMOD
W								
Reset	0	0	0	0	0	0	0	0

**Table 34. SYSMOD Bit Descriptions**

Name	Description
RESERVED	Reserved Bits 7-1, will always read 0.
SYSMOD	System mode. Default value: 0. 0: STANDBY mode 1: ACTIVE mode

## 6.6 System Interrupt Status

### 6.6.1 INT\_SOURCE (0x12)

Interrupt source register. The bits that are set (logic '1') indicate which function has asserted its interrupt and conversely, bits that are cleared (logic '0') indicate which function has not asserted its interrupt.

The setting of the bits is rising edge sensitive, the bit is set by a low to high state change and reset by reading the appropriate source register.

**Table 35. INT\_SOURCE Register**

	7	6	5	4	3	2	1	0
R	SRC_DRDY	SRC_FIFO	SRC_PW	SRC_TW	SRC_PTH	SRC_TTH	SRC_PCHG	SRC_TCHG
W								
Reset	0	0	0	0	0	0	0	0

**Table 36. INT\_SOURCE Bit Descriptions**

Name	Description
SRC_DRDY	Data ready interrupt status bit. Logic '1' indicates that Pressure/Temperature data ready interrupt is active indicating the presence of new data and/or a data overwrite, otherwise if it is a logic '0'. This bit is asserted when the PTOW and/or PTDR is set and the functional block interrupt has been enabled. This bit is cleared by reading the STATUS and Pressure/Temperature register.
SRC_FIFO	FIFO interrupt status bit. Logic '1' indicates that a FIFO interrupt event such as an overflow event has occurred. Logic '0' indicates that no FIFO interrupt event has occurred. This bit is cleared by reading the F_STATUS register. FIFO interrupt event generators: FIFO Overflow, or (Watermark: F_CNT = F_WMRK) and the functional block interrupt has been enabled.
SRC_PW	Altitude/Pressure alerter status bit near or equal to target Pressure/Altitude (near is within target value ± window value). Window value needs to be non zero for interrupt to trigger.
SRC_TW	Temperature alerter status bit near or equal to target temperature (near is within target value ± window value.) Window value needs to be non zero for interrupt to trigger.
SRC_PTH	Altitude/Pressure threshold interrupt. With the window set to a non zero value, the trigger will occur on crossing any of the thresholds: upper, center or lower. If the window is set to 0, it will only trigger on crossing the center threshold.
SRC_TTH	Temperature threshold interrupt. With the window set to a non zero value, the trigger will occur on crossing any of the thresholds: upper, center or lower. If the window is set to 0, it will only trigger on crossing the center threshold.
SRC_PCHG	Delta P interrupt status bit.
SRC_TCHG	Delta T interrupt status bit

## 6.7 Sensor Data

### 6.7.1 PT\_DATA\_CFG (0x13)

The PT\_DATA\_CFG register configures the Pressure data, Temperature data and event flag generator.

**Table 37. PT\_DATA\_CFG Register**

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	DREM	PDEFE	TDEFE
W								
Reset	0	0	0	0	0	0	0	0

**Table 38. PT\_DATA\_CFG Bit Descriptions**

Name	Description
DREM	Data ready event mode. If the DREM bit is set logic '1' and one or more of the data ready event flags (PDEFE, TDEFE) are enabled, then an event flag will be raise upon change in state of the data. If the DREM bit is cleared logic '0' and one or more of the data ready event flags are enabled, then an event flag will be raised whenever the system acquires a new set of data. Default value: 0. 0: Event detection disabled 1: Generate data ready event flag on new Pressure/Altitude and new Temperature data
PDEFE	Data event flag enable on new Pressure/Altitude data. Default value: 0 0: Event detection disabled 1: Raise event flag on new Pressure/Altitude data
TDEFE	Data event flag enable on new Temperature data. Default value: 0 0: Event detection disabled 1: Raise event flag on new Temperature data

## 6.8 Barometric Pressure Input

### 6.8.1 BAR\_IN\_MSB, BAR\_IN\_LSB (0x14, 0x15)

Barometric input for altitude calculations. Input is equivalent sea level pressure for measurement location.

Value is input in 2 Pa units.

Units are input as unsigned 16-bit integers. The default value is 101,325 Pa. The default value can be changed by writing to this register

**Table 39. BAR\_IN\_MSB Register**

	7	6	5	4	3	2	1	0
R	BAR[15]	BAR[14]	BAR[13]	BAR[12]	BAR[11]	BAR[10]	BAR[9]	BAR[8]
W								
Reset	1	1	0	0	0	1	0	1

Pressure/Altitude Target

**Table 40. BAR\_IN\_LSB Register**

	7	6	5	4	3	2	1	0
R	BAR[7]	BAR[6]	BAR[5]	BAR[4]	BAR[3]	BAR[2]	BAR[1]	BAR[0]
W								
Reset	1	1	1	0	0	1	1	1

## 6.9 Pressure/Altitude Target

### 6.9.1 P\_TGT\_MSB, P\_TGT\_LSB (0x16, 0x17)

Altitude/Pressure target value. This value works in conjunction with the window value (P\_WND\_MSB and P\_WND\_LSB).

In Altitude mode, the register value is 16-bit 2's compliment value in meters.

In Pressure mode, the value is 16-bit unsigned value in 2 Pa units.

**Notes:** A flag is set when the sensor reading falls within the window defined by  $P\_TGT\_(\text{MSB,LSB}) \pm P\_WND\_(\text{MSB,LSB})$ . If  $P\_WND\_(\text{MSB,LSB})$  is set to 0 then no flag is generated.

**Table 41. P\_TGT\_MSB Register**

	7	6	5	4	3	2	1	0
R	P_TGT15	P_TGT14	P_TGT13	P_TGT12	P_TGT11	P_TGT10	P_TGT9	P_TGT8
W								
Reset	0	0	0	0	0	0	0	0

**Table 42. P\_TGT\_LSB Register**

	7	6	5	4	3	2	1	0
R	P_TGT7	P_TGT6	P_TGT5	P_TGT4	P_TGT3	P_TGT2	P_TGT1	P_TGT0
W								
Reset	0	0	0	0	0	0	0	0

## 6.10 Temperature Target

### 6.10.1 T\_TGT (0x18)

Temperature target value input in 2's compliment value in °C.

Note: A flag is set when the sensor reading falls within the window defined by  $T\_TGT \pm T\_WND$ . If  $T\_WND$  is set to 0, then no alarm is generated.

**Table 43. T\_TGT Register**

	7	6	5	4	3	2	1	0
R	T_TGT7	T_TGT6	T_TGT5	T_TGT4	T_TGT3	T_TGT2	T_TGT1	T_TGT0
W								
Reset	0	0	0	0	0	0	0	0

## 6.11 Pressure/Altitude Window

### 6.11.1 P\_WND\_MSB, P\_WND\_LSB (0x19, 0x1A)

Pressure/Altitude window value. Unsigned 16-bit value of window value in meters or in 2 Pa units

Note: A flag is set when the sensor reading crosses the lower, center or upper level of the window from any direction.

**Table 44. P\_WND\_LSB Register**

	7	6	5	4	3	2	1	0
R	P_W15	P_W14	P_W13	P_W12	P_W11	P_W10	P_W9	P_W8
W								
Reset	0	0	0	0	0	0	0	0

**Table 45. P\_WND\_MSB Description**

	7	6	5	4	3	2	1	0
R	P_W7	P_W6	P_W5	P_W4	P_W3	P_W2	P_W1	P_W0
W								
Reset	0	0	0	0	0	0	0	0

## 6.12 Temperature Window

### 6.12.1 T\_WND (0x1B)

Temperature alarm window value. Unsigned 8-bit value °C.

Note: A flag is set when the sensor reading crosses the lower, center or upper level of the window from any direction.

**Table 46. T\_WND Register**

	7	6	5	4	3	2	1	0
R	T_W7	T_W6	T_W5	T_W4	T_W3	T_W2	T_W1	T_W0
W								
Reset	0	0	0	0	0	0	0	0

## 6.13 Minimum Pressure

### 6.13.1 P\_MIN\_MSB, P\_MIN\_CSB, P\_MIN\_LSB (0x1C, 0x1D, 0x1E)

Register with captured minimum Pressure/Altitude value.

The Altitude data is arranged as 20-bit 2's complement value in meters. Stored as meters with the 16 bits of P\_MIN\_MSB and P\_MIN\_CSB and with fractions of a meter stored in 4 bits in position 7-4 of P\_MIN\_LSB.

The Pressure is arranged as 20-bit data in Pascals. The first 18 bits are located in P\_MIN\_MSB, P\_MIN\_CSB and bits 7-6 of P\_MIN\_LSB. The 2 bits in position 5-4 of P\_MIN\_LSB represent the fractional component.

The register is cleared on power-up or manually by writing '0' to the registers

**Table 47. P\_MIN\_MSB Register**

	7	6	5	4	3	2	1	0
R	P_MIN19	P_MIN18	P_MIN17	P_MIN16	P_MIN15	P_MIN14	P_MIN13	P_MIN12
W								
Reset	0	0	0	0	0	0	0	0

**Table 48. P\_MIN\_CSB Register**

	7	6	5	4	3	2	1	0
R	P_MIN11	P_MIN10	P_MIN9	P_MIN8	P_MIN7	P_MIN6	P_MIN5	P_MIN4
W								
Reset	0	0	0	0	0	0	0	0

**Table 49. P\_MIN\_LSB Register**

	7	6	5	4	3	2	1	0
R	P_MIN3	P_MIN2	P_MIN1	P_MIN0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0



## 6.14 Maximum Pressure

### 6.14.1 P\_MAX\_MSB, P\_MAX\_CSB, P\_MAX\_LSB (0x21, 0x22, 0x23)

Register with captured maximum Pressure/Altitude value.

The Altitude data is arranged as 20-bit 2's compliment value in meters. Stored as meters with the 16 bits of P\_MAX\_MSB and P\_MAX\_CSB and with fractions of a meter stored in 4 bits in position 7-4 of P\_MAX\_LSB.

The Pressure is arranged as 20-bit data in Pascals. The first 18 bits are located in P\_MAX\_MSB, P\_MAX\_CSB and bits 7-6 of P\_MAX\_LSB. The 2 bits in position 5-4 of P\_MAX\_LSB represent the fractional component.

The register is cleared on power-up or manually by writing '0' to the registers.

**Table 50. P\_MAX\_MSB Register**

	7	6	5	4	3	2	1	0
R	P_MAX 19	P_MAX 18	P_MAX 17	P_MAX 16	P_MAX 15	P_MAX 14	P_MAX 13	P_MAX 12
W								
Reset	0	0	0	0	0	0	0	0

**Table 51. P\_MAX\_CSB Register**

	7	6	5	4	3	2	1	0
R	P_MAX 11	P_MAX 10	P_MAX 9	P_MAX 8	P_MAX 7	P_MAX 6	P_MAX 5	P_MAX 4
W								
Reset	0	0	0	0	0	0	0	0

**Table 52. P\_MAX\_LSB Register**

	7	6	5	4	3	2	1	0
R	P_MAX 3	P_MAX 2	P_MAX 1	P_MAX 0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

## 6.15 Minimum Temperature

### 6.15.1 T\_MIN\_MSB, T\_MIN\_LSB (0x1F, 0x20)

Register with captured minimum temperature value.

The Temperature data is arranged as 12-bit 2's compliment value in degrees C. The 8 bits of T\_MIN\_MSB representing degrees and with fractions of a degree stored in 4 bits in position 7-4 of T\_MIN\_LSB.

The register is cleared on power-up or manually by writing '0' to the registers.

**Table 53. T\_MIN\_MSB Register**

	7	6	5	4	3	2	1	0
R	T_MIN 11	T_MIN 10	T_MIN 9	T_MIN 8	T_MIN 7	T_MIN 6	T_MIN 5	T_MIN 4
W								
Reset	0	0	0	0	0	0	0	0

**Table 54. T\_MIN\_LSB Register**

	7	6	5	4	3	2	1	0
R	T_MIN 3	T_MIN 2	T_MIN 1	T_MIN 0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

## 6.16 Maximum Temperature

### 6.16.1 T\_MAX\_MSB, T\_MAX\_LSB (0x24, 0x25)

Register with captured maximum temperature value.

The Temperature data is arranged as 12-bit 2's compliment value in degrees C. The 8 bits of T\_MAX\_MSB representing degrees and with fractions of a degree stored in 4 bits in position 7-4 of T\_MAX\_LSB.

The register is cleared on power-up or manually by writing 0 to the registers

**Table 55. T\_MAX\_MSB Register**

	7	6	5	4	3	2	1	0
R	T_MAX 11	T_MAX 10	T_MAX 9	T_MAX 8	T_MAX 7	T_MAX 6	T_MAX 5	T_MAX 4
W								
Reset	0	0	0	0	0	0	0	0

**Table 56. T\_MAX\_LSB Register**

	7	6	5	4	3	2	1	0
R	T_MAX 3	T_MAX 2	T_MAX 1	T_MAX 0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

## 6.17 Control Registers

**Note:** Except for standby mode selection, the device must be in STANDBY mode to change any of the fields within CTRL\_REG1 (0x26).

### 6.17.1 CTRL\_REG1 (0x26)

**Table 57. CTRL\_REG1 Register**

	7	6	5	4	3	2	1	0
R	ALT	RAW	OS2	OS1	OS0	0	OST	SBYB
W						RST		
Reset	0	0	0	0	0	0	0	0

**Table 58. CTRL\_REG1 Bit Descriptions**

Name	Description
SBYB	This bit is sets the mode to ACTIVE, where the system will make measurements at periodic times based on the value of ST bits. Default value: 0 (STANDBY) 0: Part is in STANDBY mode 1: Part is ACTIVE
OST	OST bit will initiate a measurement immediately. If the ACTV bit is set, setting the OST bit will initiate an immediate measurement, but will not return to STANDBY mode until after the data is acquired. One Shot: When set and SBYB bit is 0, unit will make acquisition then return to STANDBY after new data is acquired.
RST	Software Reset. This bit is used to activate the software reset. The Boot mechanism can be enabled in STANDBY and ACTIVE mode. When the Boot bit is enabled the boot mechanism resets all functional block registers and loads the respective internal registers with default values. The system will automatically transition to STANDBY mode if not already in STANDBY mode before the software reset (re-BOOT process) can occur. Therefore, if the system was already in STANDBY mode, the reboot process will immediately begin; else if the system was in ACTIVE mode, the boot mechanism will automatically transition the system from ACTIVE mode to STANDBY mode, only then can the reboot process begin. The I <sup>2</sup> C communication system is reset to avoid accidental corrupted data access. At the end of the boot process the RST bit is de-asserted to 0. Reading this bit will return a value of zero. Default value: 0 0: Device reset disabled 1: Device reset enabled

**Table 58. CTRL\_REG1 Bit Descriptions**

OS[2:0]	Oversample Ratio. These bits select the oversampling ratio. Value is $2^{OS}$ . The default value is 000 for a ratio of 1.
RAW	RAW output mode. RAW bit will output ADC data with no post processing, except for oversampling. No scaling or offsets will be applied in the digital domain. The FIFO must be disabled and all other functionality: Alarms, Deltas, and other interrupts are disabled.
ALT	Altimeter-Barometer mode. Default value: 0 1: Part is in Altimeter Mode 0: Part is in Barometer mode

**Table 59. System Output Sample Rate Selection**

OS2	OS1	OS0	Oversample Ratio	Minimum Time Between Data Samples	Fastest OST Data Output Rate I <sup>2</sup> C <sup>(1)</sup>
0	0	0	1	2.5 ms	22.75 ms
0	0	1	2	5 ms	25.25 ms
0	1	0	4	10 ms	30.25 ms
0	1	1	8	20 ms	40.25 ms
1	0	0	16	40 ms	60.25 ms
1	0	1	32	80 ms	100.25 ms
1	1	0	64	160 ms	180.25 ms
1	1	1	128	320 ms	340.25ms

1. The fastest OST output rate is calculated by using a 4 byte I<sup>2</sup>C transaction. A write to CNTL\_REG\_1 followed by a 3 byte read of the OUT\_P at the specified OSR rate.

RAW bit overrides the ALT mode and forces to give uncompensated Pressure and Temperature data

### 6.17.2 CTRL\_REG2 (0x27)

**Table 60. CTRL\_REG2 Register**

	7	6	5	4	3	2	1	0
R	0	0	LOAD_OUTP	ALARM_SEL	ST[3]	ST[2]	ST[1]	ST[0]
W			UT					
Reset	0	0	0	0	0	0	0	0

**Table 61. CTRL\_REG2 Bit Descriptions**

Name	Description
ST[3:0]	Auto acquisition time step. Default value: 0 Step value is $2^{ST}$ : Giving a range of 1 second to $2^{15}$ seconds (9 hours)
ALARM_SEL	The bit selects the Target value for SRP_PW/SRC_PT and SRC_PTH/SRC_TTH Default value: 0 0: The values in P_TGT_MSB, P_TGT_LSB and T_TGT are used (Default) 1: The values in OUT_P/OUT_T are used for calculating the interrupts SRC_PW/SRC_TW and SRC_PTH/SRC_TTH.
LOAD_OUTPUT	This is to load the target values for SRC_PW/SRC_TW and SRC_PTH/SRC_TTH. Default value: 0 0: Do not load OUT_P/OUT_T as target values 1: The next values of OUT_P/OUT_T are used to set the target values for the interrupts. Note: 1. This bit must be set at least once if ALARM_SEL=1 2. To reload the next OUT_P/OUT_T as the target values clear and set again.

### 6.17.3 CTRL\_REG3 (Interrupt CTRL Register) (0x28)

Table 62. CTRL\_REG3 Register

	7	6	5	4	3	2	1	0
R	0		IPOL1	PP_OD1	0		IPOL2	PP_OD2
W								
Reset	0	0	0	0	0	0	0	0

Table 63. CTRL\_REG3 Description

Name	Description
IPOL1	The IPOL bit selects the polarity of the interrupt signal. When IPOL is '0' (default value) any interrupt event will signalled with a logical '0'. Interrupt Polarity active high, or active low on interrupt pad INT1. Default value: 0 0: Active low 1: Active high
PP_OD1	This bit configures the interrupt pin to Push-Pull or in Open Drain mode. The default value is 0 which corresponds to Push-Pull mode. The open drain configuration can be used for connecting multiple interrupt signals on the same interrupt line. Push-Pull/Open Drain selection on interrupt pad INT1. Default value: 0 0: Internal Pullup 1: Open drain
IPOL2	Interrupt Polarity active high, or active low on interrupt pad INT2. Default value: 0 0: Active low 1: Active high
PP_OD2	Push-Pull/Open Drain selection on interrupt pad INT2. Default value: 0 0: Internal Pull-up 1: Open drain

### 6.17.4 CTRL\_REG4 [Interrupt Enable Register] (0x29)

The corresponding functional block interrupt enable bit allows the functional block to route its event detection flags to the system's interrupt controller. The interrupt controller routes the enabled functional block interrupt to the INT1 or INT2 pin.

Table 64. CTRL\_REG4 Register

	7	6	5	4	3	2	1	0
R	INT_EN_DRDY	INT_EN_FIFO	INT_EN_PW	INT_EN_TW	INT_EN_PTH	INT_EN_TTH	INT_EN_PCHG	INT_EN_TCHG
W								
Reset	0	0	0	0	0	0	0	0

Table 65. Interrupt Enable Register Description

Interrupt Enable	Description
INT_EN_DRDY	Interrupt Enable. Default value: 0 0: Data Ready interrupt disabled 1: Data Ready interrupt enabled
INT_EN_FIFO	Interrupt Enable. Default value: 0 0: FIFO interrupt disabled 1: FIFO interrupt enabled
INT_EN_PW	Interrupt Enable. Default value: 0 0: Pressure window interrupt disabled 1: Pressure window interrupt enabled

**Table 65. Interrupt Enable Register Description**

INT_EN_TW	Interrupt Enable. Default value: 0 0: Temperature window interrupt disabled 1: Temperature window interrupt enabled.
INT_EN_PTH	Interrupt Enable. Default value: 0 0: Pressure Threshold interrupt disabled 1: Pressure Threshold interrupt enabled.
INT_EN_TTH	Interrupt Enable. Default value: 0 0: Temperature Threshold interrupt disabled 1: Temperature Threshold interrupt enabled.
INT_EN_PCHG	Interrupt Enable. Default value: 0 0: Pressure Change interrupt disabled 1: Pressure Change interrupt enabled.
INT_EN_TCHG	Interrupt Enable. Default value: 0 0: Temperature Change interrupt disabled 1: Temperature Change interrupt enabled.

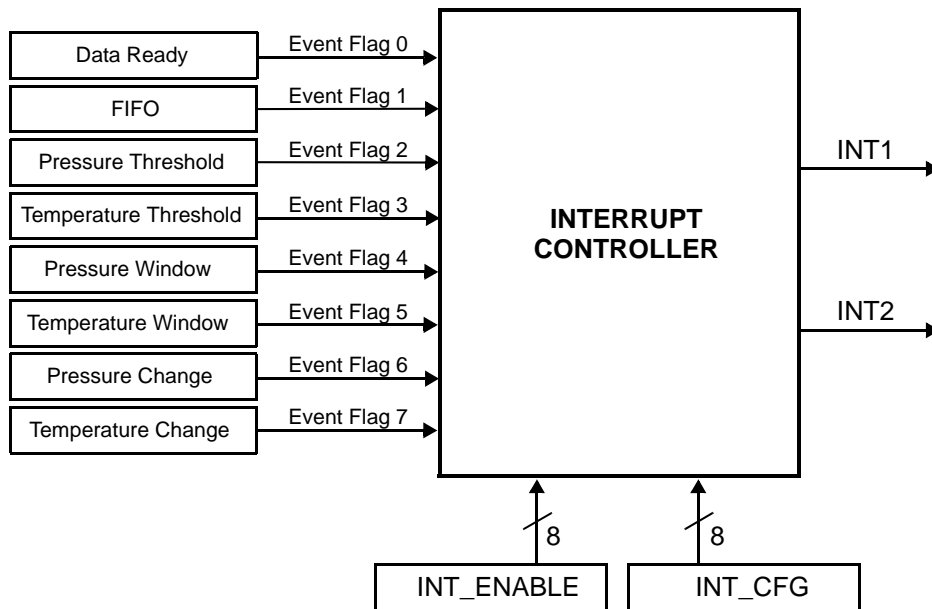
## 6.17.5 CTRL\_REG5 [Interrupt Configuration Register] (0x2A)

**Table 66. CTRL\_REG5 Register**

	7	6	5	4	3	2	1	0
R	INT_CFG_DRDY	INT_CFG_FIFO	INT_CFG_PW	INT_CFG_TW	INT_CFG_PTH	INT_CFG_TTH	INT_CFG_PCHG	INT_CFG_TCHG
W								
Reset	0	0	0	0	0	0	0	0

**Table 67. Interrupt Configuration Register Descriptions**

Interrupt Configuration	Description
INT_CFG_DRDY	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_FIFO	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_PW	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_TW	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_PTH	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_TTH	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_PCHG	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1
INT_CFG_TCHG	INT1/INT2 Configuration. Default value: 0 0: Interrupt is routed to INT2 pin; 1: Interrupt is routed to INT1



**Figure 5. Interrupt Controller Block Diagram**

The system's interrupt controller uses the corresponding bit field in the CTRL\_REG5 register to determine the routing table for the INT1 and INT2 interrupt pins. If the bit value is logic '0' the functional block's interrupt is routed to INT2, and if the bit value is logic '1' then the interrupt is routed to INT1. All interrupts routed to INT1 or INT2 are logically OR'd as illustrated in Figure 6, thus one or more functional blocks can assert an interrupt pin simultaneously; therefore a host application responding to an interrupt should read the INT\_SOURCE register to determine the appropriate sources of the interrupt.

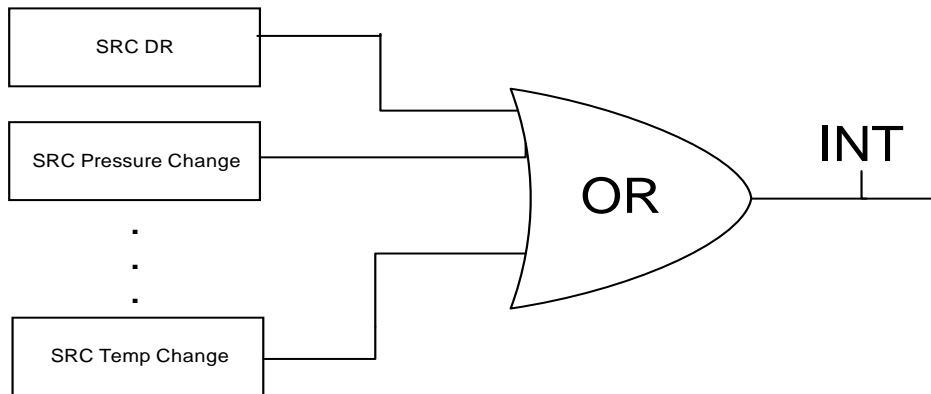


Figure 6. INT1/INT2 PIN Control Logic

## 6.18 Offset Correction

The 2's complement offset correction registers values are used to trim the temperature and pressure offsets of the factory trim settings that might occur over the life of the product.

The resolution of the pressure offset register is 4 Pa per bit.

### 6.18.1 OFF\_P (0x2B)

Pressure user accessible offset trim value expressed as an 8-bit 2's complement number. The user offset registers may be adjusted to enhance accuracy and optimize the system performance. Range is  $\pm 512$  Pa, 4 Pa per LSB.

Table 68. OFF\_P Register

	7	6	5	4	3	2	1	0
R	OFF_P7	OFF_P6	OFF_P5	OFF_P4	OFF_P3	OFF_P2	OFF_P1	OFF_P0
W								
Reset	0	0	0	0	0	0	0	0

Table 69. OFF\_P Description

Name	Description
OFF_P7-OFF_P0	Pressure offset trim value. Default value: 0000_0000.

### 6.18.2 OFF\_T (0x2C)

Temperature user accessible offset trim value expressed as an 8-bit 2's complement number. The user offset registers may be adjusted to enhance accuracy and optimize the system performance. Range is  $\pm 8^\circ$ , 0.0625°C per LSB.

Table 70. OFF\_T Register

	7	6	5	4	3	2	1	0
R	OFF_T7	OFF_T6	OFF_T5	OFF_T4	OFF_T3	OFF_T2	OFF_T1	OFF_T0
W								
Reset	0	0	0	0	0	0	0	0

Table 71. OFF\_Y Description

Name	Description
OFF_T7-OFF_T0	Temperature offset trim value. Default value: 0000_0000.

### 6.18.3 OFF\_H (0x2D)

Altitude Data User Offset Register (OFF\_H) is expressed as a 2's complement number in meters. The user offset register provides user adjustment to the vertical height of the Altitude output. The range of values are  $\pm 128$  meters.

**Table 72. OFF\_T Register**

	7	6	5	4	3	2	1	0
R	OFF_H7	OFF_H6	OFF_H5	OFF_H4	OFF_H3	OFF_H2	OFF_H1	OFF_H0
W								
Reset	0	0	0	0	0	0	0	0

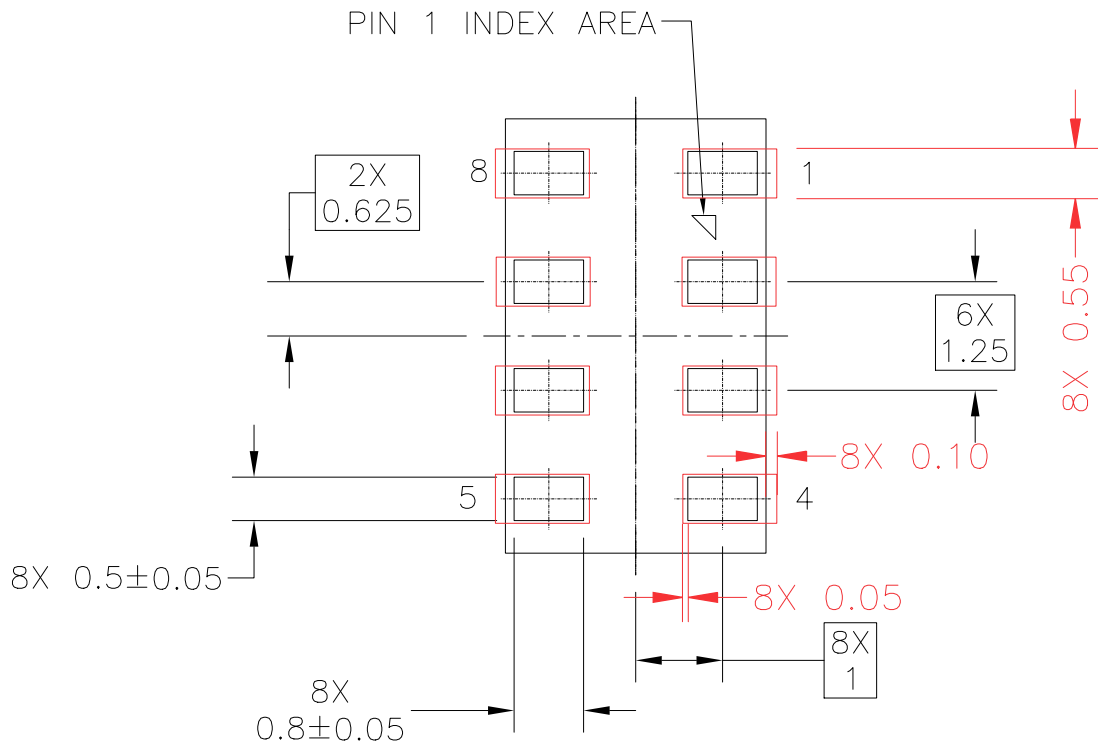
**Table 73. OFF\_Y Description**

Name	Description
OFF_H7-OFF_H0	Height offset trim value. Default value: 0000_0000.



## 7 Soldering/Landing Pad Information

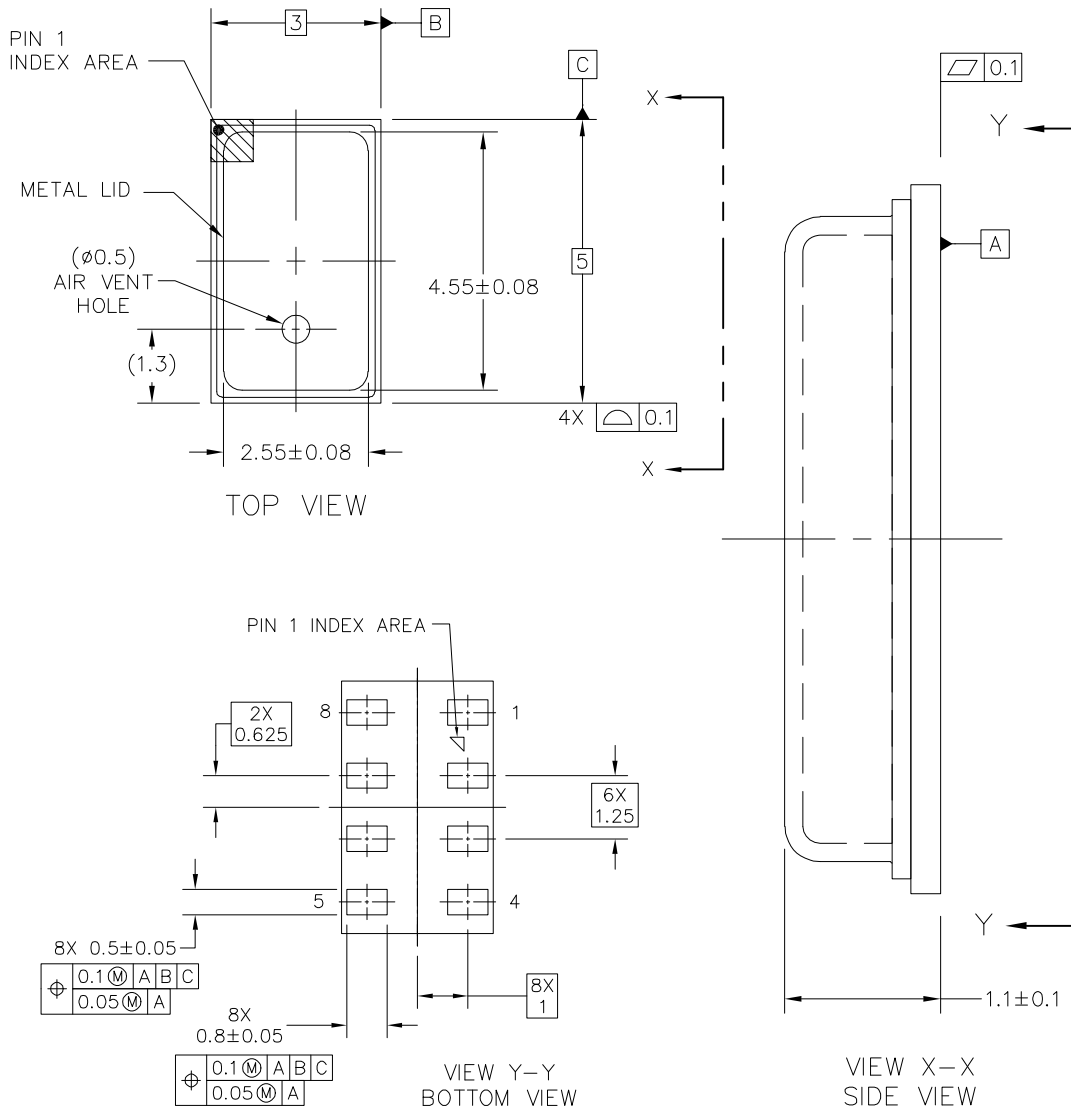
The LGA package is compliant with the RoHS standard.



BLACK for Package Outline  
RED for PCB Landing Pattern

Figure 7. MPL3115A2 Recommended PCB Landing Pattern.

# PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE: LGA 8 I/O, 3 X 5 X 1.25 PITCH, SENSOR 1.2MAX MM PKG		DOCUMENT NO: 98ASA00260D	REV: 0
		CASE NUMBER: 2153-01	17 AUG 2010
		STANDARD: NON-JEDEC	

**CASE 2053-01  
ISSUE 0  
LGA PACKAGE**

## PACKAGE DIMENSIONS

### NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
3. STYLE:  
PIN 1: VDD            PIN 5: INT2  
PIN 2: CAP            PIN 6: INT1  
PIN 3: GND            PIN 7: SDA  
PIN 4: VDDIO         PIN 8: SCL

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	<b>MECHANICAL OUTLINE</b>	PRINT VERSION NOT TO SCALE	
TITLE:            LGA 8 I/O, 3 X 5 X 1.25 PITCH, SENSOR 1.2MAX MM PKG	DOCUMENT NO: 98ASA00260D	REV: 0	
	CASE NUMBER: 2153-01	17 AUG 2010	
	STANDARD: NON-JEDEC		

**CASE 2053-01  
ISSUE 0  
LGA PACKAGE**

**MPL3115A2**

**Table 74. Revision History**

Revision number	Revision date	Description of changes
0	06/2011	• Initial Release
1	12/2011	<ul style="list-style-type: none"><li>• Added bullet and new row under Ordering Information on pg 1.</li><li>• Global change to register names 0x16, 0x17, 0x18, 0x19, 0x1A; changed ARM to TGT.</li><li>• Global change to bit names in registers 0x12 and 0x2A.</li><li>• Section 2.1, Table 1, changed Min and Max values for Pressure Absolute Accuracy.</li><li>• Table 3 changed units to ns for SDA Data Hold Time</li><li>• Added Figure 4. I<sup>2</sup>C Bus Transmission Signals</li><li>• Section 4.3: added equation</li><li>• Section 5: Added new paragraph. Added new equations in 5.6.1 and 5.6.2.</li><li>• Section 6: Added footnote to Table 11, changed TOW description in Table 12, updated paragraphs of Sections 6.1.3 and 6.1.4, Table 57 added sentence in RAW description column, Table 58 added column for Fastest OST Data Output I<sup>2</sup>C, updated Figure 5 and Figure 6.</li></ul>

## **How to Reach Us:**

### **Home Page:**

[www.freescale.com](http://www.freescale.com)

### **Web Support:**

<http://www.freescale.com/support>

### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor, Inc.  
Technical Information Center, EL516  
2100 East Elliot Road  
Tempe, Arizona 85284  
1-800-521-6274 or +1-480-768-2130  
[www.freescale.com/support](http://www.freescale.com/support)

### **Europe, Middle East, and Africa:**

Freescale Halbleiter Deutschland GmbH  
Technical Information Center  
Schatzbogen 7  
81829 Muenchen, Germany  
+44 1296 380 456 (English)  
+46 8 52200080 (English)  
+49 89 92103 559 (German)  
+33 1 69 35 48 48 (French)  
[www.freescale.com/support](http://www.freescale.com/support)

### **Japan:**

Freescale Semiconductor Japan Ltd.  
Headquarters  
ARCO Tower 15F  
1-8-1, Shimo-Meguro, Meguro-ku,  
Tokyo 153-0064  
Japan  
0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### **Asia/Pacific:**

Freescale Semiconductor China Ltd.  
Exchange Building 23F  
No. 118 Jianguo Road  
Chaoyang District  
Beijing 100022  
China  
+86 10 5879 8000  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### **For Literature Requests Only:**

Freescale Semiconductor Literature Distribution Center  
1-800-441-2447 or +1-303-675-2140  
Fax: +1-303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale, and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Xtrinsic is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2011. All rights reserved.

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

