

■ Features

- **5 x 8 and 5 x 11 dot matrix possible**
- **Low power operation support:**
 - 2.7 to 5.5V
- **Wide range of LCD driver power**
 - 3.0 to 10V
- **Correspond to high speed MPU bus interface**
 - 2 MHz (when $V_{cc} = 5V$)
- **4-bit or 8-bit MPU interface enabled**
- **80 x 8-bit display RAM (80 characters max.)**
- **13,200-bit character generator ROM for a total of 240 character fonts(5 x 8 dot or 5 x 11 dot)**
- **64 x 8-bit character generator RAM**
 - 8 character fonts (5 x 8 dot)
 - 4 character fonts (5 x 11 dot)
- **16-common x 40-segment liquid crystal display driver**
- **Programmable duty cycles**
 - 1/8 for one line of 5 x 8 dots with cursor
 - 1/11 for one line of 5 x 11 dots & cursor
 - 1/16 for two lines of 5 x 8 dots & cursor
- **Wide range of instruction functions:**
 - Display clear, cursor home, display on/off, cursor on/off, display character blink, cursor shift, display shift
- **Pin function compatibility with HD44780, KS0066 and SED1278**
- **Automatic reset circuit that initializes the controller/driver after power on**
- **Internal oscillator with external resistors**
- **Low power consumption**
- **QFP80 and Bare Chip available**

■ Description

The ST7066U dot-matrix liquid crystal display controller and driver LSI displays alphanumeric, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

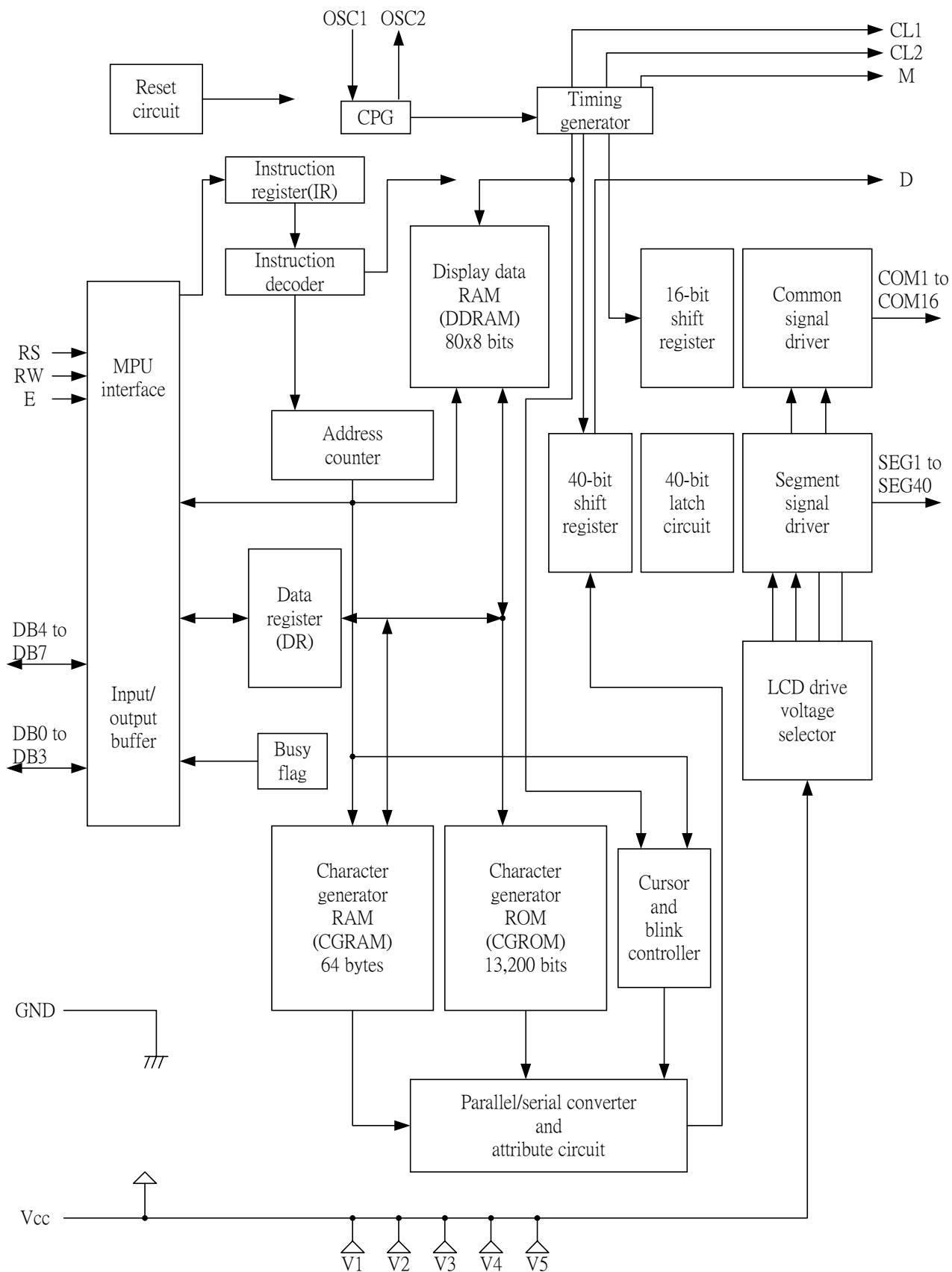
The ST7066U has pin function compatibility with the HD44780, KS0066 and SED1278 that allows the user to easily replace it with an ST7066U. The ST7066U character generator ROM is extended to generate

240 5x8(5x11) dot character fonts for a total of 240 different character fonts. The low power supply (2.7V to 5.5V) of the ST7066U is suitable for any portable battery-driven product requiring low power dissipation.

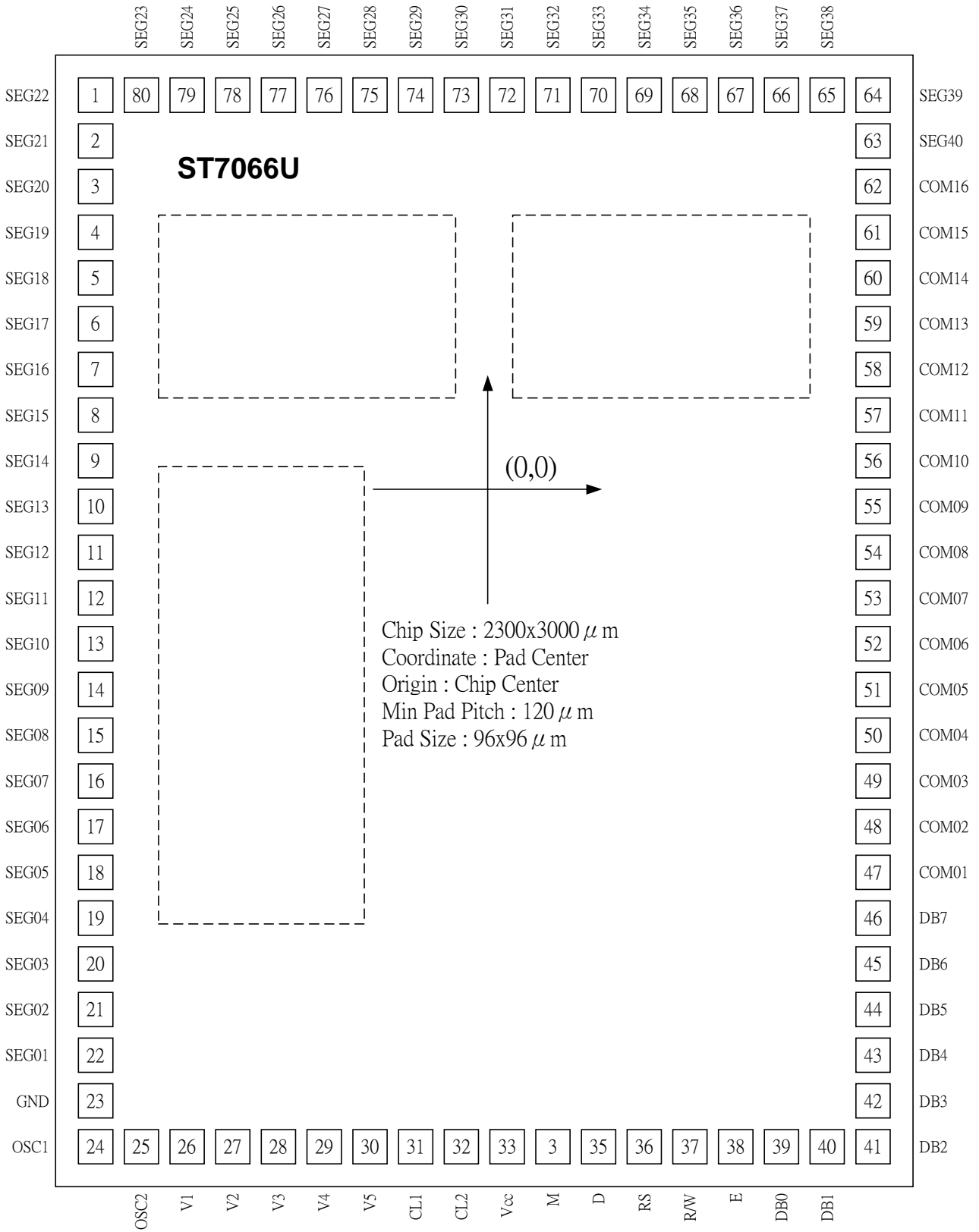
The ST7066U LCD driver consists of 16 common signal drivers and 40 segment signal drivers which can extend display size by cascading segment driver ST7065 or ST7063. The maximum display size can be either 80 characters in 1-line display or 40 characters in 2-line display. A single ST7066U can display up to one 8-character line or two 8-character lines.

| Product Name | Support Character |
|--------------|--------------------|
| ST7066U-0A | English / Japan |
| ST7066U-0B | English / European |
| ST7066U-0E | English / European |

■ Block Diagram



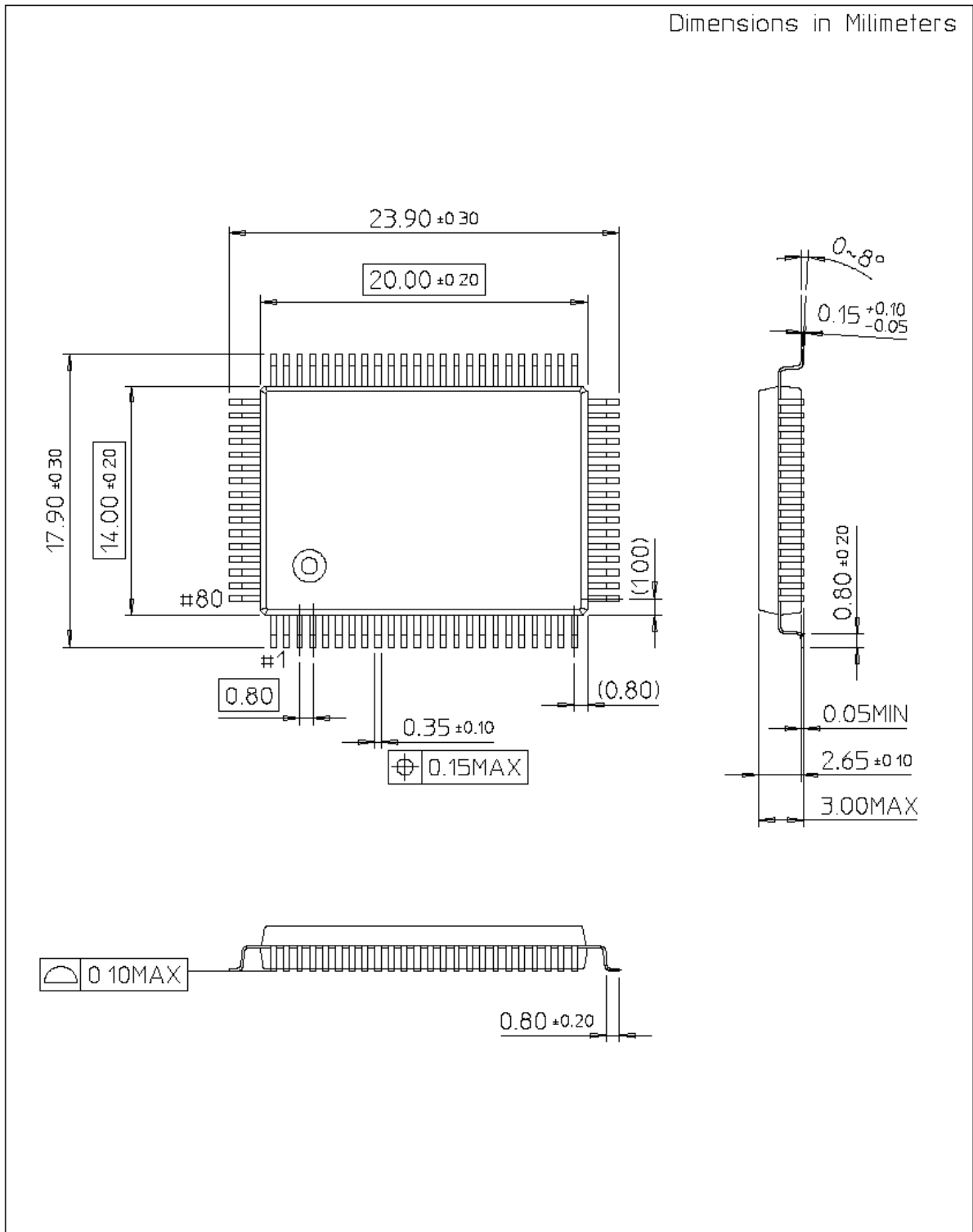
■ Pad Arrangement



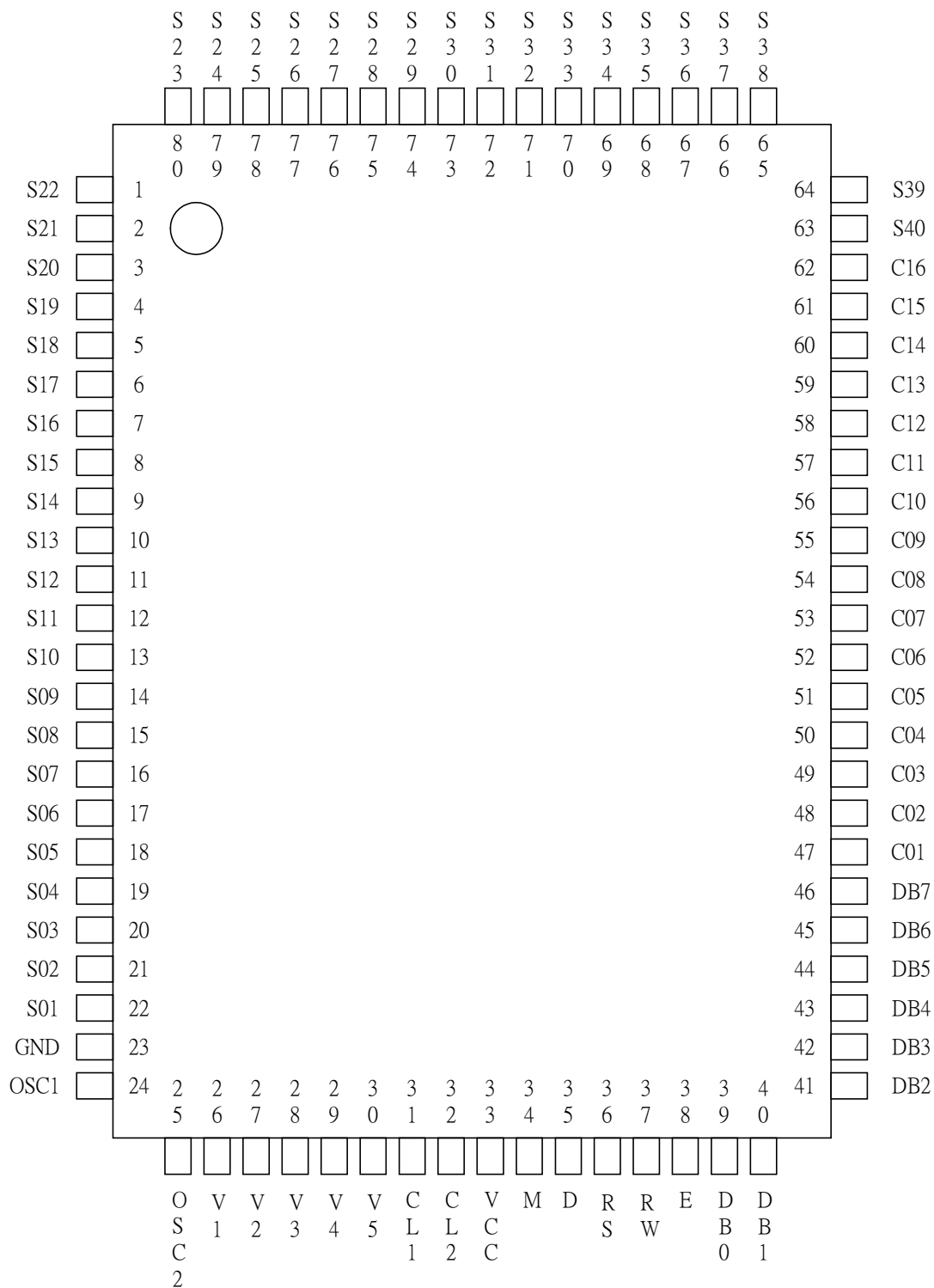
Substrate Connect to V_{DD}.

■ Package Dimensions

80-QFP-1420C



■ Pad Configuration(80 QFP)



■ Pad Location Coordinates

| Pad No. | Function | X | Y |
|---------|----------|-------|-------|
| 1 | SEG22 | -1040 | 1400 |
| 2 | SEG21 | -1040 | 1270 |
| 3 | SEG20 | -1040 | 1140 |
| 4 | SEG19 | -1040 | 1020 |
| 5 | SEG18 | -1040 | 900 |
| 6 | SEG17 | -1040 | 780 |
| 7 | SEG16 | -1040 | 660 |
| 8 | SEG15 | -1040 | 540 |
| 9 | SEG14 | -1040 | 420 |
| 10 | SEG13 | -1040 | 300 |
| 11 | SEG12 | -1040 | 180 |
| 12 | SEG11 | -1040 | 60 |
| 13 | SEG10 | -1040 | -60 |
| 14 | SEG9 | -1040 | -180 |
| 15 | SEG8 | -1040 | -300 |
| 16 | SEG7 | -1040 | -420 |
| 17 | SEG6 | -1040 | -540 |
| 18 | SEG5 | -1040 | -660 |
| 19 | SEG4 | -1040 | -780 |
| 20 | SEG3 | -1040 | -900 |
| 21 | SEG2 | -1040 | -1020 |
| 22 | SEG1 | -1040 | -1140 |
| 23 | GND | -1040 | -1270 |
| 24 | OSC1 | -1040 | -1400 |
| 25 | OSC2 | -910 | -1400 |
| 26 | V1 | -780 | -1400 |
| 27 | V2 | -660 | -1400 |
| 28 | V3 | -540 | -1400 |
| 29 | V4 | -420 | -1400 |
| 30 | V5 | -300 | -1400 |
| 31 | CL1 | -180 | -1400 |
| 32 | CL2 | -60 | -1400 |
| 33 | Vcc | 60 | -1400 |
| 34 | M | 180 | -1400 |
| 35 | D | 300 | -1400 |
| 36 | RS | 420 | -1400 |
| 37 | RW | 540 | -1400 |
| 38 | E | 660 | -1400 |
| 39 | DB0 | 780 | -1400 |
| 40 | DB1 | 910 | -1400 |

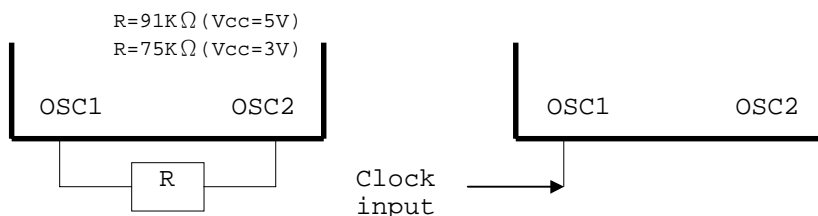
| Pad No. | Function | X | Y |
|---------|----------|------|-------|
| 41 | DB2 | 1040 | -1400 |
| 42 | DB3 | 1040 | -1270 |
| 43 | DB4 | 1040 | -1140 |
| 44 | DB5 | 1040 | -1020 |
| 45 | DB6 | 1040 | -900 |
| 46 | DB7 | 1040 | -780 |
| 47 | COM1 | 1040 | -660 |
| 48 | COM2 | 1040 | -540 |
| 49 | COM3 | 1040 | -420 |
| 50 | COM4 | 1040 | -300 |
| 51 | COM5 | 1040 | -180 |
| 52 | COM6 | 1040 | -60 |
| 53 | COM7 | 1040 | 60 |
| 54 | COM8 | 1040 | 180 |
| 55 | COM9 | 1040 | 300 |
| 56 | COM10 | 1040 | 420 |
| 57 | COM11 | 1040 | 540 |
| 58 | COM12 | 1040 | 660 |
| 59 | COM13 | 1040 | 780 |
| 60 | COM14 | 1040 | 900 |
| 61 | COM15 | 1040 | 1020 |
| 62 | COM16 | 1040 | 1140 |
| 63 | SEG40 | 1040 | 1270 |
| 64 | SEG39 | 1040 | 1400 |
| 65 | SEG38 | 910 | 1400 |
| 66 | SEG37 | 780 | 1400 |
| 67 | SEG36 | 660 | 1400 |
| 68 | SEG35 | 540 | 1400 |
| 69 | SEG34 | 420 | 1400 |
| 70 | SEG33 | 300 | 1400 |
| 71 | SEG32 | 180 | 1400 |
| 72 | SEG31 | 60 | 1400 |
| 73 | SEG30 | -60 | 1400 |
| 74 | SEG29 | -180 | 1400 |
| 75 | SEG28 | -300 | 1400 |
| 76 | SEG27 | -420 | 1400 |
| 77 | SEG26 | -540 | 1400 |
| 78 | SEG25 | -660 | 1400 |
| 79 | SEG24 | -780 | 1400 |
| 80 | SEG23 | -910 | 1400 |

■ Pin Function

| Name | Number | I/O | Interfaced with | Function |
|-----------------------|--------|-----|----------------------------|--|
| RS | 1 | I | MPU | Select registers. 0: Instruction register (for write) Busy flag: address counter (for read) 1: Data register (for write and read) |
| R/W | 1 | I | MPU | Select read or write. 0: Write 1: Read |
| E | 1 | I | MPU | Starts data read/write. |
| DB4 to DB7 | 4 | I/O | MPU | Four high order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. DB7 can be used as a busy flag. |
| DB0 to DB3 | 4 | I/O | MPU | Four low order bi-directional tristate data bus pins. Used for data transfer and receive between the MPU and the ST7066U. These pins are not used during 4-bit operation. |
| CL1 | 1 | O | Extension driver | Clock to latch serial data D sent to the extension driver |
| CL2 | 1 | O | Extension driver | Clock to shift serial data D |
| M | 1 | O | Extension driver | Switch signal for converting the liquid crystal drive waveform to AC |
| D | 1 | O | Extension driver | Character pattern data corresponding to each segment signal |
| COM1 to COM16 | 16 | O | LCD | Common signals that are not used are changed to non-selection waveform. COM9 to COM16 are non-selection waveforms at 1/8 duty factor and COM12 to COM16 are non-selection waveforms at 1/11 duty factor. |
| SEG1 to SEG40 | 40 | O | LCD | Segment signals |
| V1 to V5 | 5 | - | Power supply | Power supply for LCD drive $V_{CC} - V5 = 10\text{ V (Max)}$ |
| V _{CC} , GND | 2 | - | Power supply | V _{CC} : 2.7V to 5.5V, GND: 0V |
| OSC1, OSC2 | 2 | | Oscillation resistor clock | When crystal oscillation is performed, a resistor must be connected externally. When the pin input is an external clock, it must be input to OSC1. |

Note:

1. V_{CC}>=V1>=V2>=V3>=V4>=V5 must be maintained
2. Two clock options:



■ Function Description

● System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus or 8-bit bus is selected by DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is data register (DR), the other is instruction register(IR).

The data register(DR) is used as temporary data storage place for being written into or read from DDRAM/CGRAM, target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. So to speak, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically.

The Instruction register(IR) is used only to store instruction code transferred from MPU. MPU cannot use it to read instruction data.

To select register, use RS input pin in 4-bit/8-bit bus mode.

| RS | R/W | Operation |
|----|-----|---|
| L | L | Instruction Write operation (MPU writes Instruction code into IR) |
| L | H | Read Busy Flag(DB7) and address counter (DB0 ~ DB6) |
| H | L | Data Write operation (MPU writes data into DR) |
| H | H | Data Read operation (MPU reads data from DR) |

Table 1. Various kinds of operations according to RS and R/W bits.

● Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not High.

● Address Counter (AC)

Address Counter(AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 ~ DB6 ports.

● **Display Data RAM (DDRAM)**

Display data RAM (DDRAM) stores display data represented in 8-bit character codes. Its extended capacity is 80 x 8 bits, or 80 characters. The area in display data RAM (DDRAM) that is not used for display can be used as general data RAM. See Figure 1 for the relationships between DDRAM addresses and positions on the liquid crystal display.

The DDRAM address (A_{DD}) is set in the address counter (AC) as hexadecimal.

➤ **1-line display (N = 0) (Figure 2)**

When there are fewer than 80 display characters, the display begins at the head position. For example, if using only the ST7066U, 8 characters are displayed. See Figure 3.

When the display shift operation is performed, the DDRAM address shifts. See Figure 3.

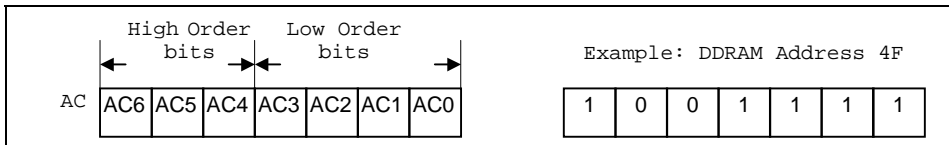


Figure 1 DDRAM Address

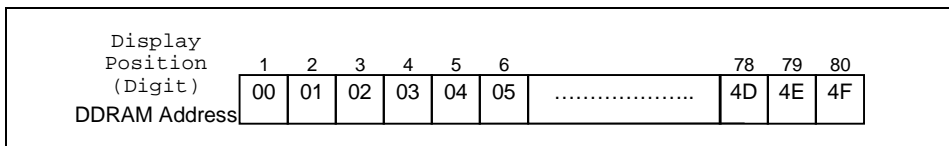


Figure 2 1-Line Display

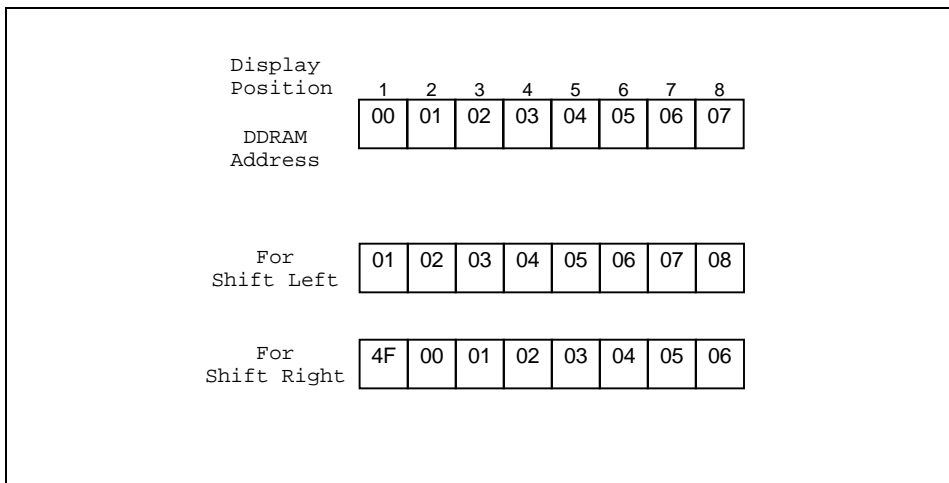


Figure 3 1-Line by 8-Character Display Example

➤ **2-line display (N = 1) (Figure 4)**

Case 1: When the number of display characters is less than 40×2 lines, the two lines are displayed from the head. Note that the first line end address and the second line start address are not consecutive. For example, when just the ST7066U is used, 8 characters \times 2 lines are displayed. See Figure 5.

When display shift operation is performed, the DDRAM address shifts. See Figure 5.

| | | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|-------|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | | 38 | 39 | 40 |
| DDRAM Address (hexadecimal) | 00 | 01 | 02 | 03 | 04 | 05 | | 25 | 26 | 27 |
| | 40 | 41 | 42 | 43 | 44 | 45 | | 65 | 66 | 67 |

Figure 4 2-Line Display

| | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 |

Figure 5 2-Line by 8-Character Display Example

Case 2: For a 16-character × 2-line display, the ST7066U can be extended using one 40-output extension driver. See Figure 6.

When display shift operation is performed, the DDRAM address shifts. See Figure 6.

| | | | | | | | | | | | | | | | | |
|------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Display Position | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| DDRAM Address | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F |
| | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F |
| For Shift Left | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 |
| | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 |
| For Shift Right | 27 | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E |
| | 67 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E |

Figure 6 2-Line by 16-Character Display Example

- **Character Generator ROM (CGROM)**

The character generator ROM generates 5 x 8 dot or 5 x 11 dot character patterns from 8-bit character codes. It can generate 240 5 x 8 dot character patterns. User-defined character patterns are also available by mask-programmed ROM.

- **Character Generator RAM (CGRAM)**

In the character generator RAM, the user can rewrite character patterns by program. For 5 x 8 dots, eight character patterns can be written, and for 5 x 11 dots, four character patterns can be written.

Write into DDRAM the character codes at the addresses shown as the left column of Table 4 to show the character patterns stored in CGRAM.

See Table 5 for the relationship between CGRAM addresses and data and display patterns. Areas that are not used for display can be used as general data RAM.

- **Timing Generation Circuit**

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interfering with each other. Therefore, when writing data to DDRAM, for example, there will be no undesirable interference, such as flickering, in areas other than the display area.

- **LCD Driver Circuit**

LCD Driver circuit has 16 common and 40 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 40 bit segment latch serially, and then it is stored to 40 bit shift latch. When each common is selected by 16 bit common register, segment data also output through segment driver from 40 bit segment latch. In case of 1-line display mode, COM1 ~ COM8 have 1/8 duty or COM1 ~ COM11 have 1/11 duty, and in 2-line mode, COM1 ~ COM16 have 1/16 duty ratio.

- **Cursor/Blink Control Circuit**

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

Table 4 Correspondence between Character Codes and Character Patterns (ROM Code: 0A)

NO.7066-0A

| b7-b4 b3-b0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM (1) | | | 0 | 1 | P | R | | | | 一 | 3 | 3 | 3 | 3 | |
| 0001 | (2) | | ! | 1 | A | 0 | a | a | | | 。 | 7 | 7 | 4 | 3 | 9 |
| 0010 | (3) | | " | 2 | B | R | b | r | | | 7 | 4 | 9 | × | p | e |
| 0011 | (4) | | # | 3 | C | S | c | s | | | 7 | 0 | 7 | E | S | o |
| 0100 | (5) | | \$ | 4 | D | T | d | t | | | 7 | 1 | 1 | + | μ | o |
| 0101 | (6) | | % | 5 | E | U | e | u | | | 。 | 7 | 6 | 1 | o | 0 |
| 0110 | (7) | | & | 6 | F | U | f | u | | | 9 | 0 | 二 | 3 | p | z |
| 0111 | (8) | | ' | 7 | G | W | g | w | | | 7 | 7 | 7 | 7 | g | π |
| 1000 | (1) | | (| 8 | H | X | h | x | | | 4 | 0 | * | U | 7 | z |
| 1001 | (2) | |) | 9 | I | Y | i | y | | | o | 7 | 7 | U | 7 | U |
| 1010 | (3) | | * | 0 | J | Z | j | z | | | z | 0 | 0 | U | U | 7 |
| 1011 | (4) | | + | 1 | K | C | k | c | | | * | 7 | U | U | * | π |
| 1100 | (5) | | , | < | L | * | l | l | | | o | 0 | 7 | 7 | o | π |
| 1101 | (6) | | - | = | N | J | n | j | | | a | z | z | U | U | + |
| 1110 | (7) | | . | > | N | ^ | n | ^ | | | 3 | U | U | ^ | π | |
| 1111 | (8) | | / | ? | 0 | L | o | e | | | U | U | 7 | ^ | 0 | |

Table 4(Cont.) (ROM Code: 0B)

NO.7066-0B

| b7-b4 b3-b0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM (1) | 士 | 田 | 0 | 0 | P | P | P | 0 | 0 | 0 | 1 | R | B | 0 | |
| 0001 | (2) | 三 | ! | 1 | A | 0 | a | a | 0 | 0 | 1 | 1 | J | + | 0 | |
| 0010 | (3) | 0 | " | 2 | B | R | b | r | 0 | 0 | 0 | * | 0 | 0 | 2 | |
| 0011 | (4) | L | # | 3 | C | B | c | c | 0 | 0 | 0 | 1 | P | W | E | |
| 0100 | (5) | 7 | * | 4 | D | T | d | t | 0 | 0 | 0 | 1 | d | 7 | 0 | |
| 0101 | (6) | L | % | 5 | E | U | e | u | 0 | 0 | 0 | 1 | ↑ | Δ | 7 | |
| 0110 | (7) | Y | % | 6 | F | U | f | u | 0 | 0 | 0 | 1 | ↓ | 0 | 7 | |
| 0111 | (8) | J | ' | 7 | G | W | g | w | 0 | 0 | 0 | 1 | * | Δ | L | |
| 1000 | (1) | J | () | 8 | H | X | h | x | 0 | 0 | 0 | 1 | * | 0 | K | |
| 1001 | (2) | L | > | 9 | I | Y | i | y | 0 | 0 | 1 | 1 | 1 | 1 | Δ | |
| 1010 | (3) | * | * | : | J | Z | j | z | 0 | 0 | 0 | 1 | 7 | 1 | μ | |
| 1011 | (4) | J | + | : | K | L | k | l | 1 | 1 | 0 | 0 | L | 7 | 0 | |
| 1100 | (5) | 三 | * | < | L | N | l | n | 1 | 1 | 0 | 0 | U | 0 | 0 | |
| 1101 | (6) | 0 | - | = | M | J | m | j | 1 | 1 | 0 | 0 | * | * | 7 | |
| 1110 | (7) | 0 | . | > | N | n | n | n | Δ | 0 | 0 | 1 | 0 | 0 | 0 | |
| 1111 | (8) | 0 | / | ? | 0 | L | 0 | 0 | Δ | 0 | 0 | 1 | 0 | 0 | 0 | |

Table 4(Cont.) (ROM Code: 0E)

NO.7066-0E

| b7-b4 b3-b0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|----------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | CG RAM (1) | | | 0 | 1 | P | R | O | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0001 | (2) | ! | 1 | A | 0 | a | 9 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0010 | (3) | " | 2 | B | R | b | r | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0011 | (4) | # | 3 | C | S | c | s | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0100 | (5) | \$ | 4 | D | T | d | t | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0101 | (6) | % | 5 | E | U | e | u | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0110 | (7) | & | 6 | F | V | f | v | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 0111 | (8) | ' | 7 | G | W | g | w | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1000 | (1) | (| 8 | H | X | h | x | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1001 | (2) |) | 9 | I | Y | i | y | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1010 | (3) | * | : | J | Z | j | z | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1011 | (4) | + | ; | K | L | k | l | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1100 | (5) | , | < | L | * | l | l | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1101 | (6) | - | = | M | I | m | i | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1110 | (7) | . | > | N | < | n | > | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 1111 | (8) | / | ? | O | L | o | e | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |

| Character Code (DDRAM Data) | | | | | | | CGRAM Address | | | | | Character Patterns (CGRAM Data) | | | | | | | | | |
|-----------------------------|----|----|----|----|----|----|---------------|----|----|----|----|---------------------------------|----|----|----|----|----|----|----|----|----|
| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | b5 | b4 | b3 | b2 | b1 | b0 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 1 |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | | | | | | | | |
| 0 | 0 | 0 | 0 | - | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | - | - | - | 1 | 1 | 1 | 1 | 0 |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 1 | | | | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 1 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 1 | 1 | | | | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 0 | | | | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 1 | | | | | | | | |
| | | | | | 0 | 0 | 1 | | | | 0 | 0 | 1 | | | | | | | | |
| 0 | 0 | 1 | 0 | 0 | 0 | | | | | | | | | | | | | | | | |

Table 5 Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
 2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bits will light up the 8th line regardless of the cursor presence.
 3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
 4. As shown Table 5, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
 5. 1 for CGRAM data corresponds to display selection and 0 to non-selection.
- “-“: Indicates no effect.

■ Instructions

There are four categories of instructions that:

- Designate ST7066U functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Others

Instruction Table:

| Instruction | Instruction Code | | | | | | | | | | Description | Description Time (270KHz) | |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------------|--|---------|
| | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | | | |
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM. and set DDRAM address to "00H" from AC | 1.52 ms |
| Return Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. | 1.52 ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets cursor move direction and specifies display shift. These operations are performed during data write and read. | 37 us |
| Display ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:entire display on C=1:cursor on B=1:cursor position on | 37 us |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x | Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. | 37 us |
| Function Set | 0 | 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x | DL:interface data is 8/4 bits N:number of line is 2/1 F:font size is 5x11/5x8 | 37 us |
| Set CGRAM address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set CGRAM address in address counter | 37 us |
| Set DDRAM address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Set DDRAM address in address counter | 37 us |
| Read Busy flag and address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | | Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read. | 0 us |
| Write data to RAM | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Write data into internal RAM (DDRAM/CGRAM) | 37 us |
| Read data from RAM | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | Read data from internal RAM (DDRAM/CGRAM) | 37 us |

Note:

Be sure the ST7066U is not in the busy state (BF = 0) before sending an instruction from the MPU to the ST7066U. If an instruction is sent without checking the busy flag, the time between the first instruction and next instruction will take much longer than the instruction time itself. Refer to Instruction Table for the list of each instruction execution time.

■ Instruction Description

● Clear Display

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

● Return Home

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | x |

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

● Entry Mode Set

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S |

Set the moving direction of cursor and display.

- **I/D : Increment / decrement of DDRAM address (cursor or blink)**
 When I/D = "High", cursor/blink moves to right and DDRAM address is increased by 1.
 When I/D = "Low", cursor/blink moves to left and DDRAM address is decreased by 1.
 * CGRAM operates the same as DDRAM, when read from or write to CGRAM.
- **S: Shift of entire display**
 When DDRAM read (CGRAM read/write) operation or S = "Low", shift of entire display is not performed. If S = "High" and DDRAM write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

| S | I/D | Description |
|---|-----|--------------------------------|
| H | H | Shift the display to the left |
| H | L | Shift the display to the right |

● **Display ON/OFF**

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B |

Control display/cursor/blink ON/OFF 1 bit register.

- **D : Display ON/OFF control bit**
When D = "High", entire display is turned on.
When D = "Low", display is turned off, but display data is remained in DDRAM.
- **C : Cursor ON/OFF control bit**
When C = "High", cursor is turned on.
When C = "Low", cursor is disappeared in current display, but I/D register remains its data.
- **B : Cursor Blink ON/OFF control bit**
When B = "High", cursor blink is on, that performs alternate between all the high data and display character at the cursor position.
When B = "Low", blink is off.

● **Cursor or Display Shift**

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | x | x |

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data. During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line. Note that display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifted individually. When display shift is performed, the contents of address counter are not changed.

| S/C | R/L | Description | AC Value |
|-----|-----|--|----------|
| L | L | Shift cursor to the left | AC=AC-1 |
| L | H | Shift cursor to the right | AC=AC+1 |
| H | L | Shift display to the left. Cursor follows the display shift | AC=AC |
| H | H | Shift display to the right. Cursor follows the display shift | AC=AC |

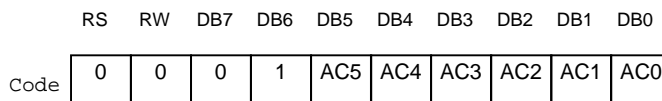
● **Function Set**

| | | | | | | | | | | |
|------|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| Code | 0 | 0 | 0 | 0 | 1 | DL | N | F | x | x |

- **DL : Interface data length control bit**
 When DL = "High", it means 8-bit bus mode with MPU.
 When DL = "Low", it means 4-bit bus mode with MPU. So to speak, DL is a signal to select 8-bit or 4-bit bus mode.
 When 4-bit bus mode, it needs to transfer 4-bit data by two times.
- **N : Display line number control bit**
 When N = "Low", it means 1-line display mode.
 When N = "High", 2-line display mode is set.
- **F : Display font type control bit**
 When F = "Low", it means 5 x 8 dots format display mode
 When F = "High", 5 x 11 dots format display mode.

| N | F | No. of Display Lines | Character Font | Duty Factor |
|---|---|----------------------|----------------|-------------|
| L | L | 1 | 5x8 | 1/8 |
| L | H | 1 | 5x11 | 1/11 |
| H | x | 2 | 5x8 | 1/16 |

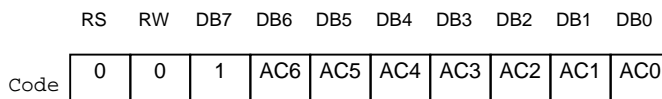
● **Set CGRAM Address**



Set CGRAM address to AC.

This instruction makes CGRAM data available from MPU.

● **Set DDRAM Address**



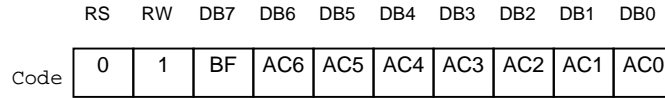
Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH".

In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

● **Read Busy Flag and Address**

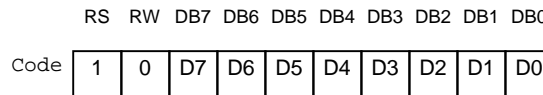


When BF = “High”, indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted.

The address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR.

After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1.

● **Write Data to CGRAM or DDRAM**

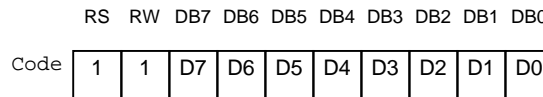


Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

● **Read Data from CGRAM or DDRAM**



Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data that read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

* In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

■ Reset Function

Initializing by Internal Reset Circuit

An internal reset circuit automatically initializes the ST7066U when the power is turned on. The following instructions are executed during the initialization. The busy flag (BF) is kept in the busy state until the initialization ends (BF = 1). The busy state lasts for 40 ms after VCC rises to 4.5 V.

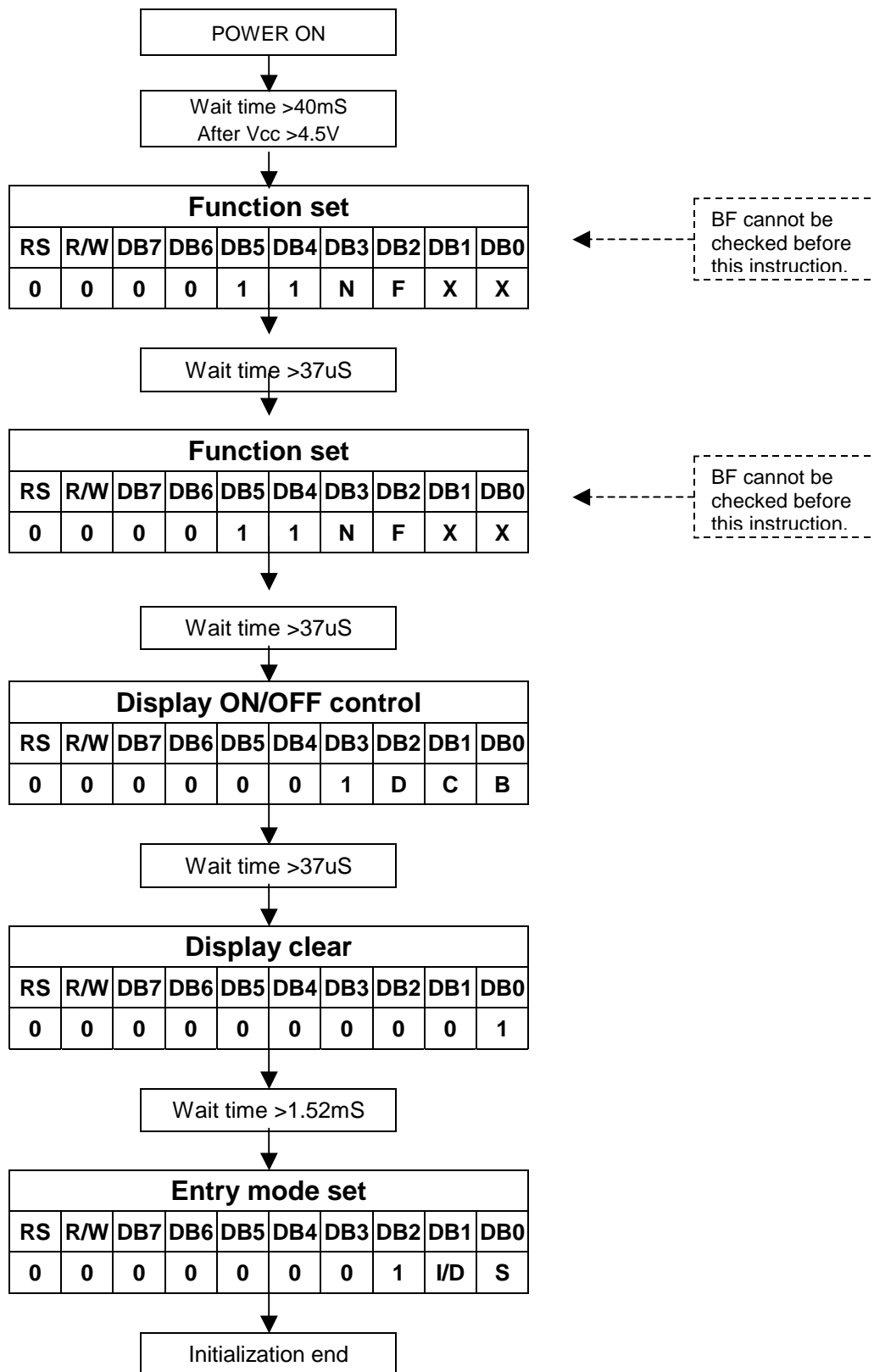
1. Display clear
2. Function set:
 - DL = 1; 8-bit interface data
 - N = 0; 1-line display
 - F = 0; 5x8 dot character font
3. Display on/off control:
 - D = 0; Display off
 - C = 0; Cursor off
 - B = 0; Blinking off
4. Entry mode set:
 - I/D = 1; Increment by 1
 - S = 0; No shift

Note:

If the electrical characteristics conditions listed under the table Power Supply Conditions Using Internal Reset Circuit are not met, the internal reset circuit will not operate normally and will fail to initialize the ST7066U. For such a case, initialization must be performed by the MPU as explain by the following figure.

■ Initializing by Instruction

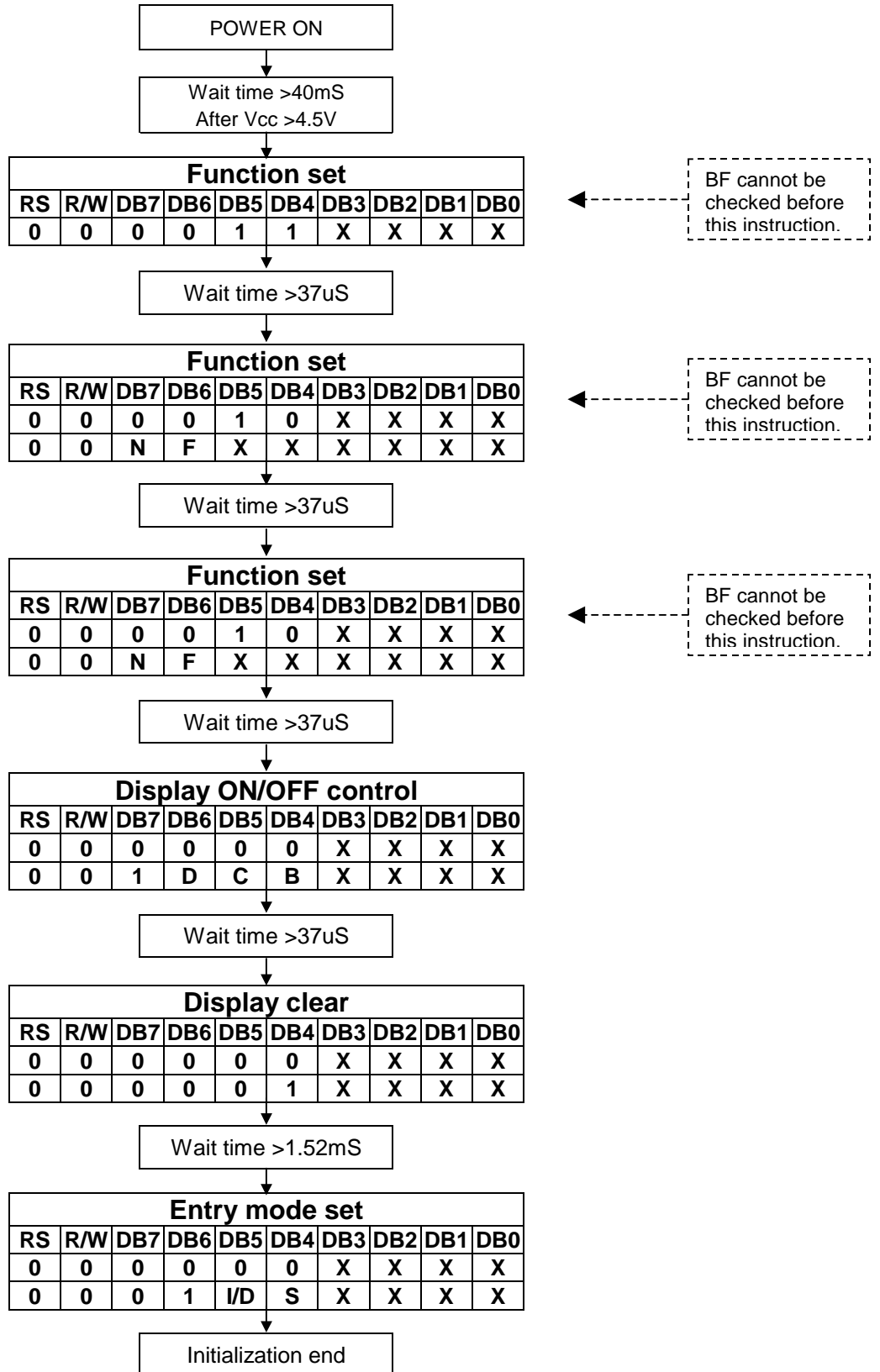
- 8-bit Interface (fosc=270KHz)



➤ Initial Program Code Example For 8051 MPU(8 Bit Interface):

```
-----  
INITIAL_START:  
    CALL    DELAY40mS  
  
    MOV     A,#38H          ;FUNCTION SET  
    CALL    WRINS_NOCHK    ;8 bit,N=1,5*7dot  
    CALL    DELAY37uS  
  
    MOV     A,#38H          ;FUNCTION SET  
    CALL    WRINS_NOCHK    ;8 bit,N=1,5*7dot  
    CALL    DELAY37uS  
  
    MOV     A,#0FH         ;DISPLAY ON  
    CALL    WRINS_CHK  
    CALL    DELAY37uS  
  
    MOV     A,#01H         ;CLEAR DISPLAY  
    CALL    WRINS_CHK  
    CALL    DELAY1.52mS  
  
    MOV     A,#06H         ;ENTRY MODE SET  
    CALL    WRINS_CHK      ;CURSOR MOVES TO RIGHT  
    CALL    DELAY37uS  
  
-----  
MAIN_START:  
  
    XXXX  
    XXXX  
    XXXX  
    XXXX  
    .  
    .  
    .  
    .  
  
-----  
WRINS_CHK:  
    CALL    CHK_BUSY  
WRINS_NOCHK:  
    CLR     RS              ;EX:Port 3.0  
    CLR     RW              ;EX:Port 3.1  
    SETB    E               ;EX:Port 3.2  
    MOV     P1,A            ;EX:Port 1=Data Bus  
    CLR     E  
    MOV     P1,#FFH        ;For Check Busy Flag  
    RET  
  
-----  
CHK_BUSY:                                ;Check Busy Flag  
    CLR     RS  
    SETB    RW  
    SETB    E  
    JB     P1.7,$  
    CLR     E  
    RET
```


● 4-bit Interface (fosc=270KHz)

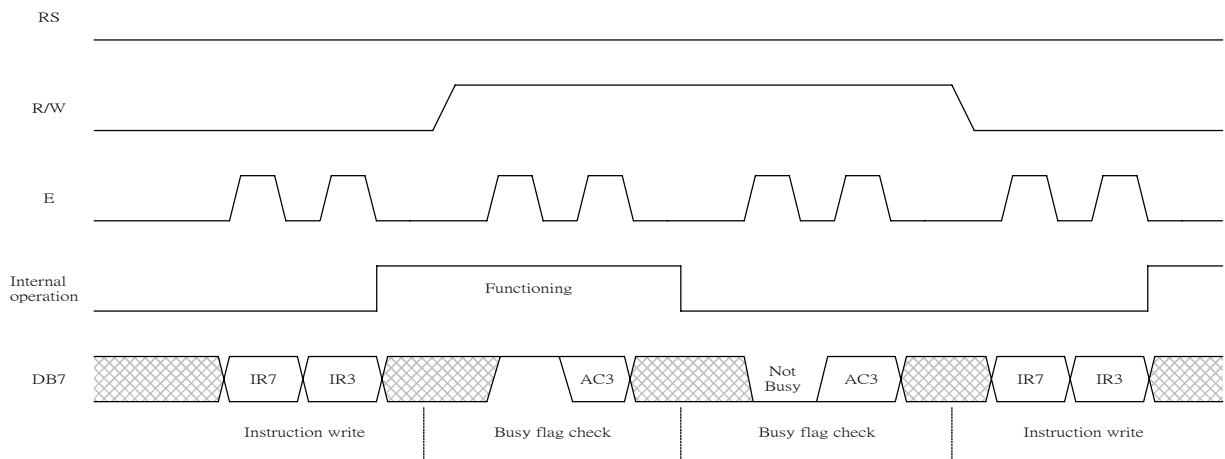


■ Interfacing to the MPU

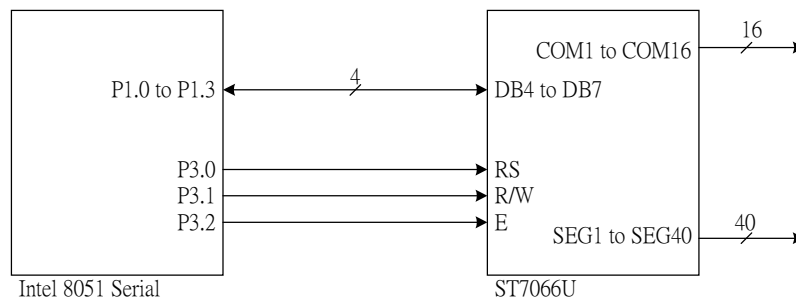
The ST7066U can send data in either two 4-bit operations or one 8-bit operation, thus allowing interfacing with 4- or 8-bit MPU.

- **For 4-bit interface data, only four bus lines (DB4 to DB7) are used for transfer.** Bus lines DB0 to DB3 are disabled. The data transfer between the ST7066U and the MPU is completed after the 4-bit data has been transferred twice. As for the order of data transfer, the four high order bits (for 8-bit operation, DB4 to DB7) are transferred before the four low order bits (for 8-bit operation, DB0 to DB3). The busy flag must be checked (one instruction) after the 4-bit data has been transferred twice. Two more 4-bit operations then transfer the busy flag and address counter data.

➤ Example of busy flag check timing sequence

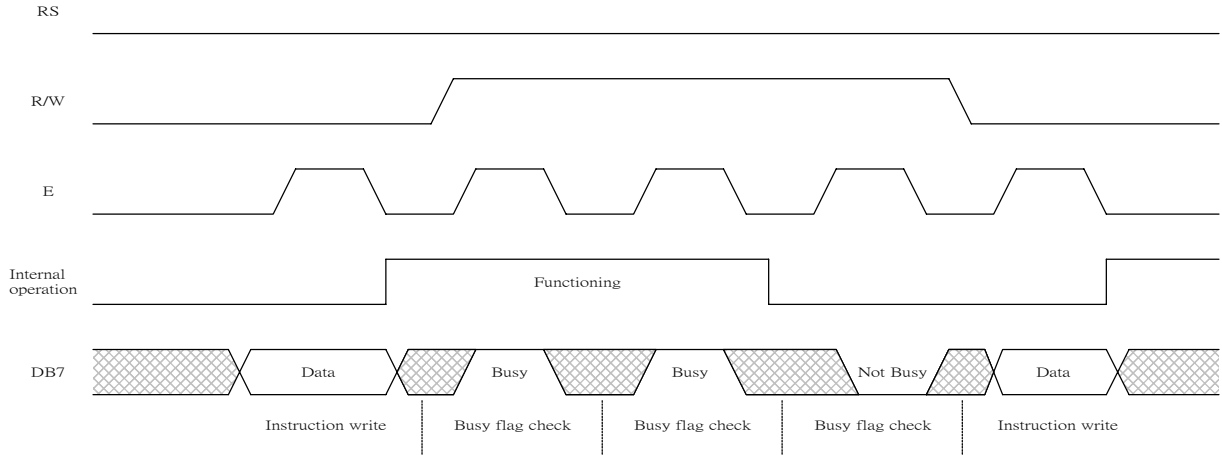


➤ Intel 8051 interface

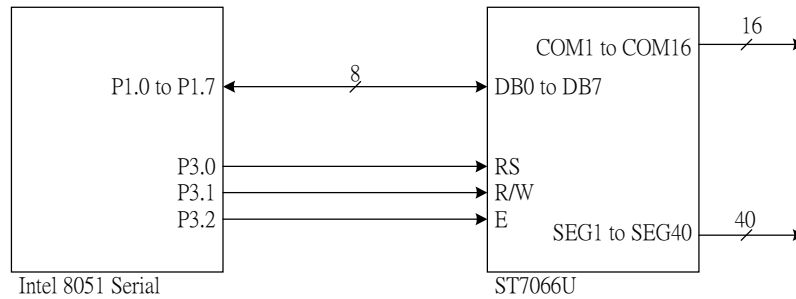


- For 8-bit interface data, all eight bus lines (DB0 to DB7) are used.

➤ Example of busy flag check timing sequence



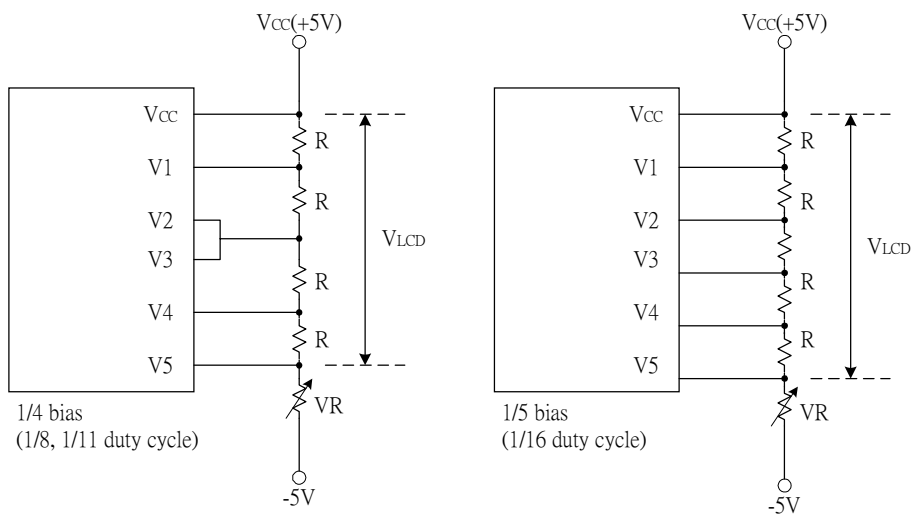
➤ Intel 8051 interface



Supply Voltage for LCD Drive

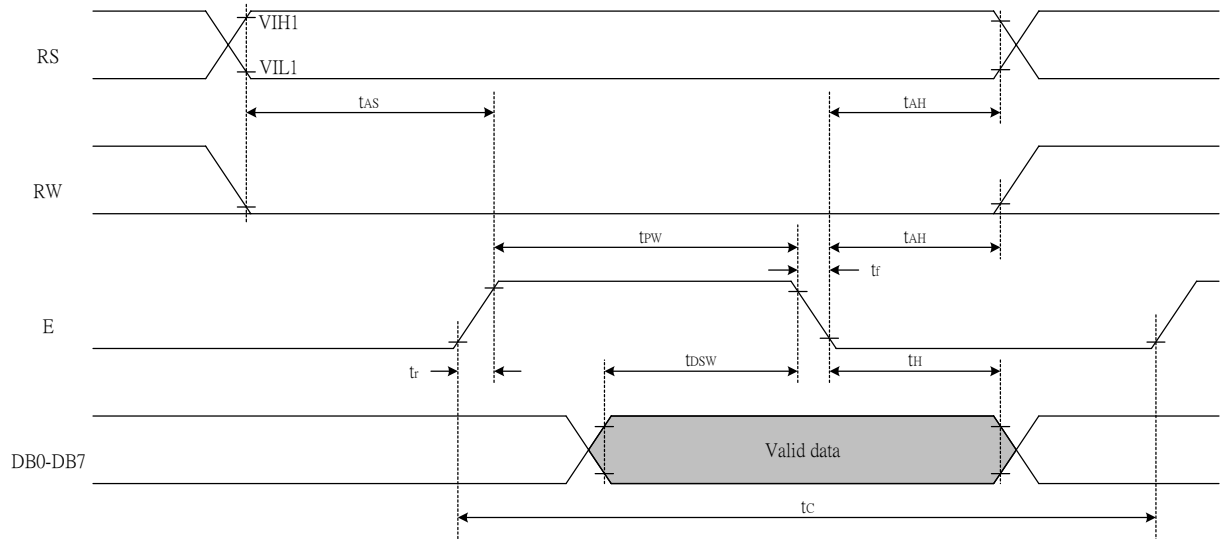
There are different voltages that supply to ST7066U's pin (V1 - V5) to obtain LCD drive waveform. The relations of the bias, duty factor and supply voltages are shown as below:

| Supply Voltage | Duty Factor | |
|----------------|-----------------------|-----------------------|
| | 1/8, 1/11 | 1/16 |
| | Bias | |
| V1 | $V_{cc} - 1/4V_{LCD}$ | $V_{cc} - 1/5V_{LCD}$ |
| V2 | $V_{cc} - 1/2V_{LCD}$ | $V_{cc} - 2/5V_{LCD}$ |
| V3 | $V_{cc} - 1/2V_{LCD}$ | $V_{cc} - 3/5V_{LCD}$ |
| V4 | $V_{cc} - 3/4V_{LCD}$ | $V_{cc} - 4/5V_{LCD}$ |
| V5 | $V_{cc} - V_{LCD}$ | $V_{cc} - V_{LCD}$ |

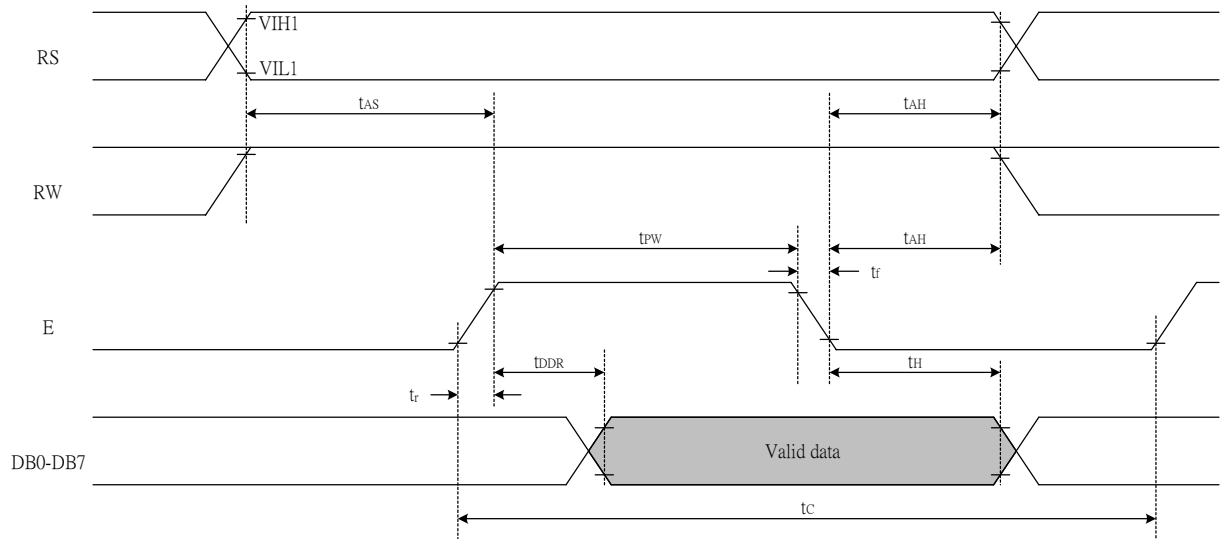


■ Timing Characteristics

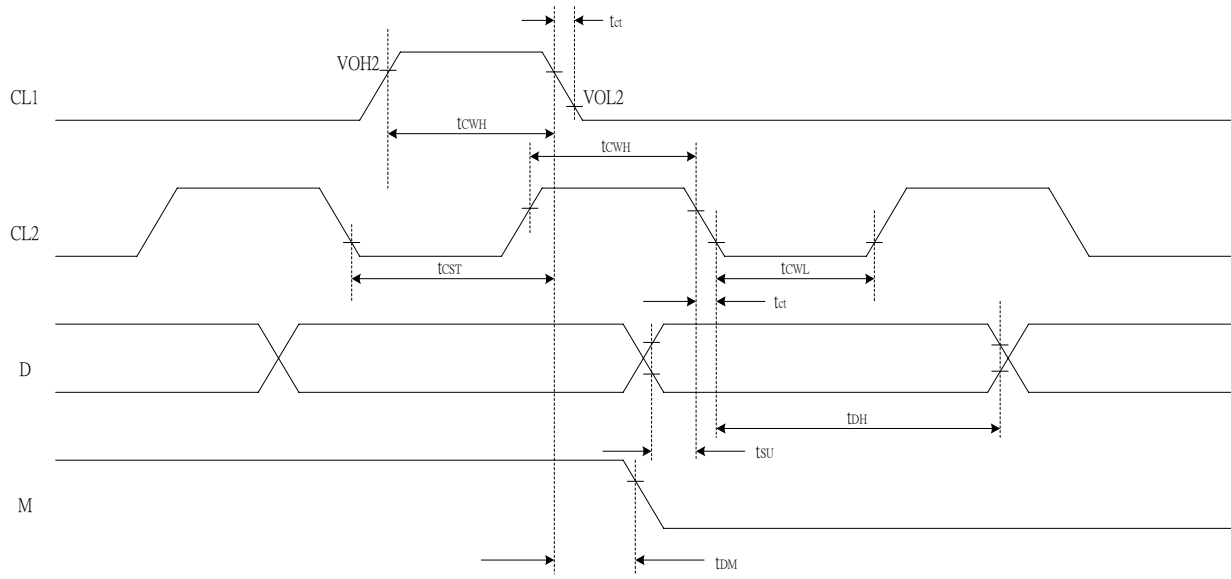
- Writing data from MPU to ST7066U



- Reading data from ST7066U to MPU



● Interface Timing with External Driver



■ AC Characteristics

(TA = 25°C, VCC = 2.7V)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|--|-----------------------|-----------------|------|------|------|------|
| <i>Internal Clock Operation</i> | | | | | | |
| f _{OSC} | OSC Frequency | R = 75KΩ | 190 | 270 | 350 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f _{EX} | External Frequency | - | 125 | 270 | 410 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T _R , T _F | Rise/Fall Time | - | - | - | 0.2 | μs |
| <i>Write Mode (Writing data from MPU to ST7066U)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 460 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS, RW, E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS, RW, E | 10 | - | - | ns |
| T _{DSW} | Data Setup Time | Pins: DB0 - DB7 | 80 | - | - | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Read Mode (Reading Data from ST7066U to MPU)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 480 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS, RW, E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS, RW, E | 10 | - | - | ns |
| T _{DDR} | Data Setup Time | Pins: DB0 - DB7 | - | - | 320 | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Interface Mode with LCD Driver(ST7065)</i> | | | | | | |
| T _{CWH} | Clock Pulse with High | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CWL} | Clock Pulse with Low | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CST} | Clock Setup Time | Pins: CL1, CL2 | 500 | - | - | ns |
| T _{SU} | Data Setup Time | Pin: D | 300 | - | - | ns |
| T _{DH} | Data Hold Time | Pin: D | 300 | - | - | ns |
| T _{DM} | M Delay Time | Pin: M | 0 | - | 2000 | ns |

■ AC Characteristics

(TA = 25°C, VCC = 5V)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|--|-----------------------|-----------------|------|------|------|------|
| <i>Internal Clock Operation</i> | | | | | | |
| f _{OSC} | OSC Frequency | R = 91KΩ | 190 | 270 | 350 | KHz |
| <i>External Clock Operation</i> | | | | | | |
| f _{EX} | External Frequency | - | 125 | 270 | 410 | KHz |
| | Duty Cycle | - | 45 | 50 | 55 | % |
| T _R , T _F | Rise/Fall Time | - | - | - | 0.2 | μs |
| <i>Write Mode (Writing data from MPU to ST7066U)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 140 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 10 | - | - | ns |
| T _{DSW} | Data Setup Time | Pins: DB0 - DB7 | 40 | - | - | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Read Mode (Reading Data from ST7066U to MPU)</i> | | | | | | |
| T _C | Enable Cycle Time | Pin E | 1200 | - | - | ns |
| T _{PW} | Enable Pulse Width | Pin E | 140 | - | - | ns |
| T _R , T _F | Enable Rise/Fall Time | Pin E | - | - | 25 | ns |
| T _{AS} | Address Setup Time | Pins: RS,RW,E | 0 | - | - | ns |
| T _{AH} | Address Hold Time | Pins: RS,RW,E | 10 | - | - | ns |
| T _{DDR} | Data Setup Time | Pins: DB0 - DB7 | - | - | 100 | ns |
| T _H | Data Hold Time | Pins: DB0 - DB7 | 10 | - | - | ns |
| <i>Interface Mode with LCD Driver(ST7065)</i> | | | | | | |
| T _{CWH} | Clock Pulse with High | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CWL} | Clock Pulse with Low | Pins: CL1, CL2 | 800 | - | - | ns |
| T _{CST} | Clock Setup Time | Pins: CL1, CL2 | 500 | - | - | ns |
| T _{SU} | Data Setup Time | Pin: D | 300 | - | - | ns |
| T _{DH} | Data Hold Time | Pin: D | 300 | - | - | ns |
| T _{DM} | M Delay Time | Pin: M | 0 | - | 2000 | ns |

■ Absolute Maximum Ratings

| Characteristics | Symbol | Value |
|-----------------------|-----------|-------------------------------|
| Power Supply Voltage | V_{CC} | -0.3 to +7.0 |
| LCD Driver Voltage | V_{LCD} | $V_{CC}-10.0$ to $V_{CC}+0.3$ |
| Input Voltage | V_{IN} | -0.3 to $V_{CC}+0.3$ |
| Operating Temperature | T_A | -40°C to + 90°C |
| Storage Temperature | T_{STO} | -55°C to + 125°C |

■ DC Characteristics

($T_A = 25^\circ\text{C}$, $V_{CC} = 2.7\text{ V} - 4.5\text{ V}$)

| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|------------|---|---|---------------|------|-------------|---------------|
| V_{CC} | Operating Voltage | - | 2.7 | - | 4.5 | V |
| V_{LCD} | LCD Voltage | $V_{CC}-V_5$ | 3.0 | - | 10.0 | V |
| I_{CC} | Power Supply Current | $f_{OSC} = 270\text{KHz}$ $V_{CC}=3.0\text{V}$ | - | 0.1 | 0.25 | mA |
| V_{IH1} | Input High Voltage (Except OSC1) | - | $0.7V_{CC}$ | - | V_{CC} | V |
| V_{IL1} | Input Low Voltage (Except OSC1) | - | - 0.3 | - | 0.6 | V |
| V_{IH2} | Input High Voltage (OSC1) | - | $0.7V_{CC}$ | - | V_{CC} | V |
| V_{IL2} | Input Low Voltage (OSC1) | - | - | - | $0.2V_{CC}$ | V |
| V_{OH1} | Output High Voltage (DB0 - DB7) | $I_{OH} = -0.1\text{mA}$ | $0.75 V_{CC}$ | - | - | V |
| V_{OL1} | Output Low Voltage (DB0 - DB7) | $I_{OL} = 0.1\text{mA}$ | - | - | $0.2V_{CC}$ | V |
| V_{OH2} | Output High Voltage (Except DB0 - DB7) | $I_{OH} = -0.04\text{mA}$ | $0.8V_{CC}$ | - | V_{CC} | V |
| V_{OL2} | Output Low Voltage (Except DB0 - DB7) | $I_{OL} = 0.04\text{mA}$ | - | - | $0.2V_{CC}$ | V |
| R_{COM} | Common Resistance | $V_{LCD} = 4\text{V}$, $I_d = 0.05\text{mA}$ | - | 2 | 20 | $K\Omega$ |
| R_{SEG} | Segment Resistance | $V_{LCD} = 4\text{V}$, $I_d = 0.05\text{mA}$ | - | 2 | 30 | $K\Omega$ |
| I_{LEAK} | Input Leakage Current | $V_{IN} = 0\text{V}$ to V_{CC} | -1 | - | 1 | μA |
| I_{PUP} | Pull Up MOS Current | $V_{CC} = 3\text{V}$ | -10 | -50 | -120 | μA |

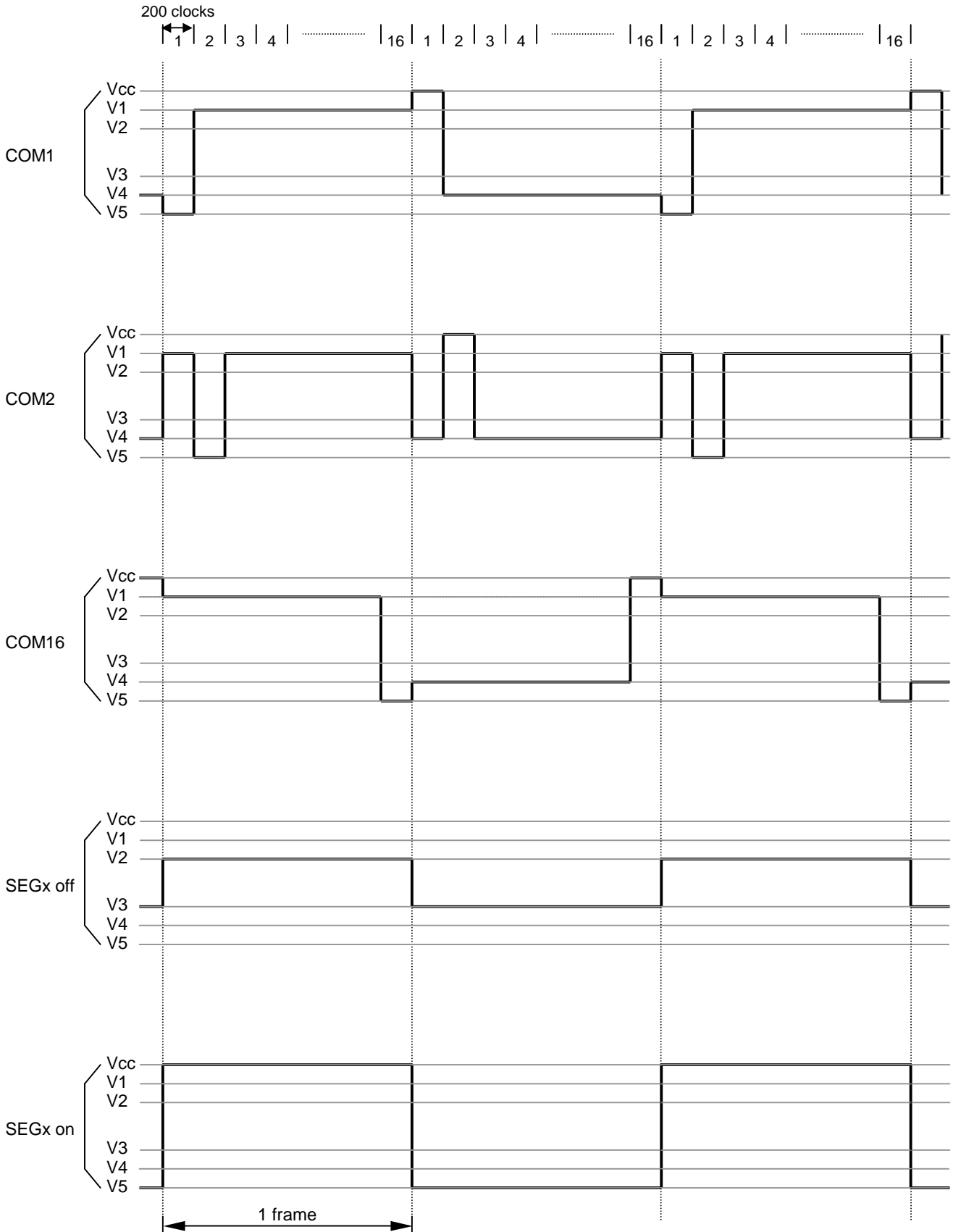
■ DC Characteristics

(TA = 25°C, V_{CC} = 4.5 V - 5.5 V)

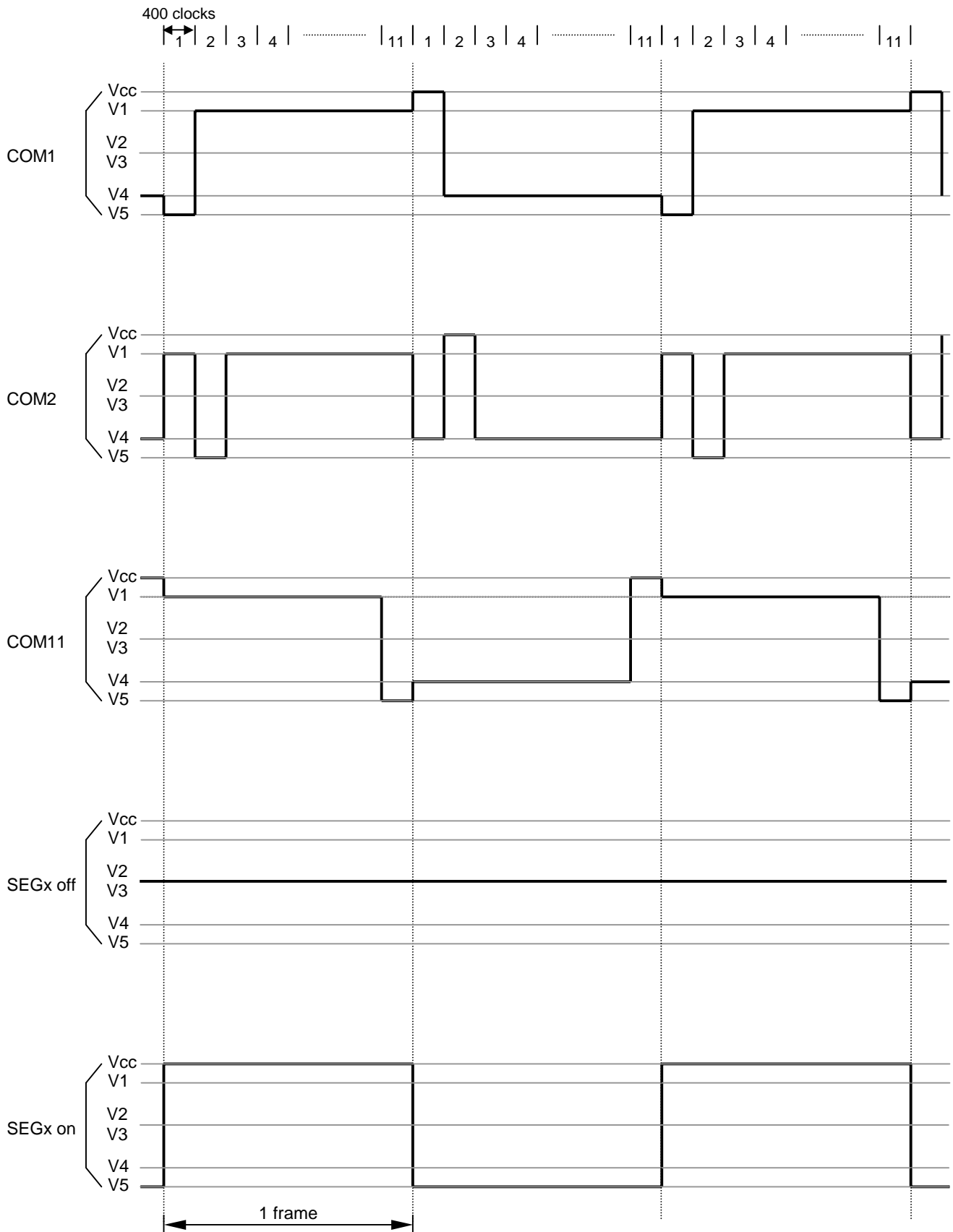
| Symbol | Characteristics | Test Condition | Min. | Typ. | Max. | Unit |
|-------------------|---|--|--------------------|------|--------------------|------|
| V _{CC} | Operating Voltage | - | 4.5 | - | 5.5 | V |
| V _{LCD} | LCD Voltage | V _{CC} -V5 | 3.0 | - | 10.0 | V |
| I _{CC} | Power Supply Current | f _{OSC} = 270KHz V _{CC} =5.0V | - | 0.2 | 0.5 | mA |
| V _{IH1} | Input High Voltage (Except OSC1) | - | 0.7V _{CC} | - | V _{CC} | V |
| V _{IL1} | Input Low Voltage (Except OSC1) | - | -0.3 | - | 0.6 | V |
| V _{IH2} | Input High Voltage (OSC1) | - | V _{CC} -1 | - | V _{CC} | V |
| V _{IL2} | Input Low Voltage (OSC1) | - | - | - | 1.0 | V |
| V _{OH1} | Output High Voltage (DB0 - DB7) | I _{OH} = -0.1mA | 3.9 | - | V _{CC} | V |
| V _{OL1} | Output Low Voltage (DB0 - DB7) | I _{OL} = 0.1mA | - | - | 0.4 | V |
| V _{OH2} | Output High Voltage (Except DB0 - DB7) | I _{OH} = -0.04mA | 0.9V _{CC} | - | V _{CC} | V |
| V _{OL2} | Output Low Voltage (Except DB0 - DB7) | I _{OL} = 0.04mA | - | - | 0.1V _{CC} | V |
| R _{COM} | Common Resistance | V _{LCD} = 4V, I _d = 0.05mA | - | 2 | 20 | KΩ |
| R _{SEG} | Segment Resistance | V _{LCD} = 4V, I _d = 0.05mA | - | 2 | 30 | KΩ |
| I _{LEAK} | Input Leakage Current | V _{IN} = 0V to V _{CC} | -1 | - | 1 | μA |
| I _{PUP} | Pull Up MOS Current | V _{CC} = 5V | -50 | -110 | -180 | μA |

■ LCD Frame Frequency

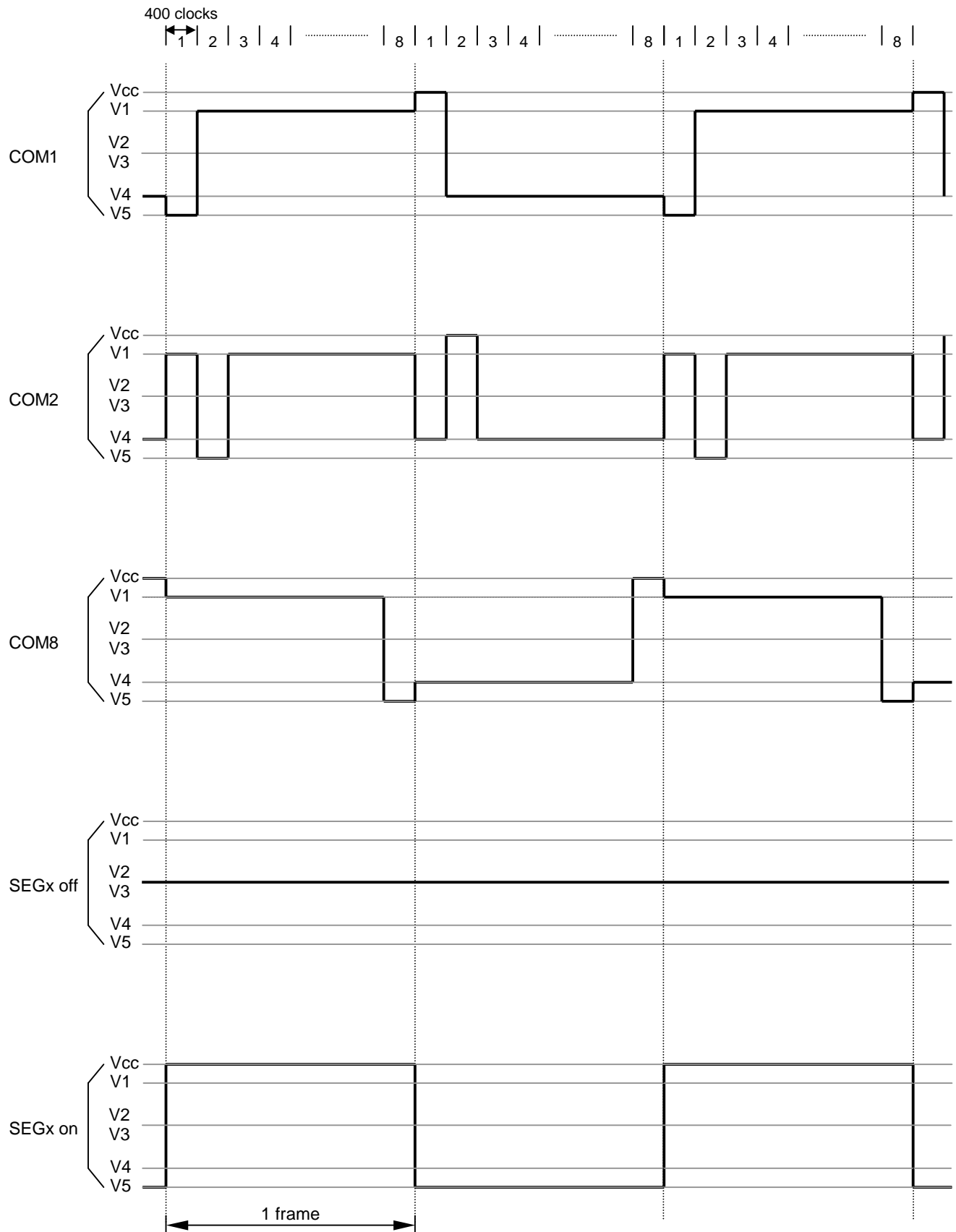
- Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/16 duty; 1/5 bias, 1 frame = 3.7us x 200 x 16 = 11840us=11.8ms(84.7Hz)



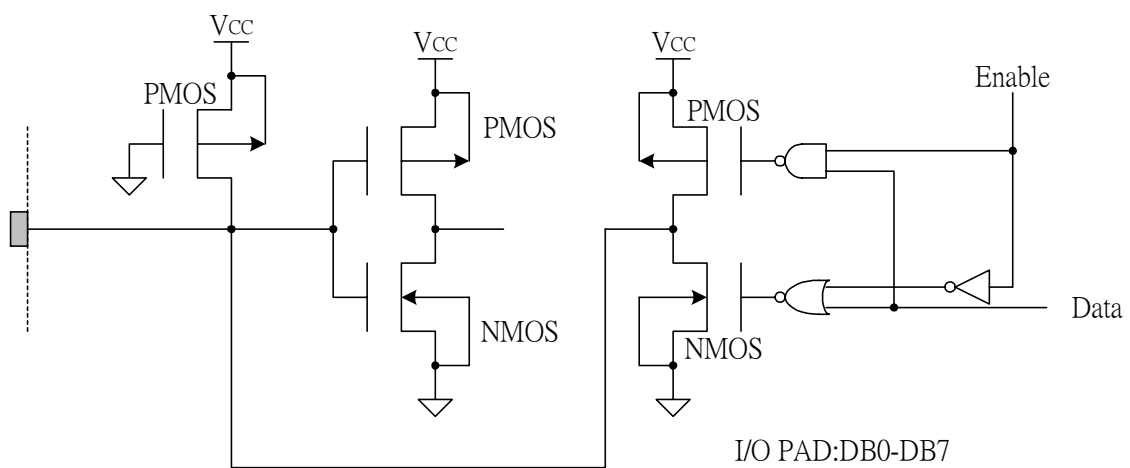
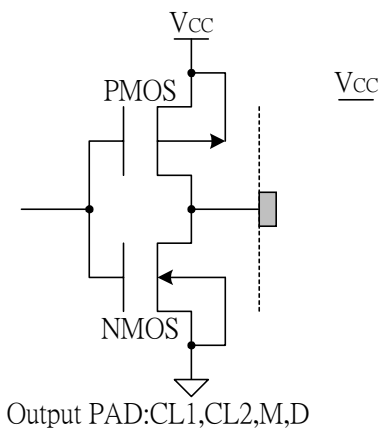
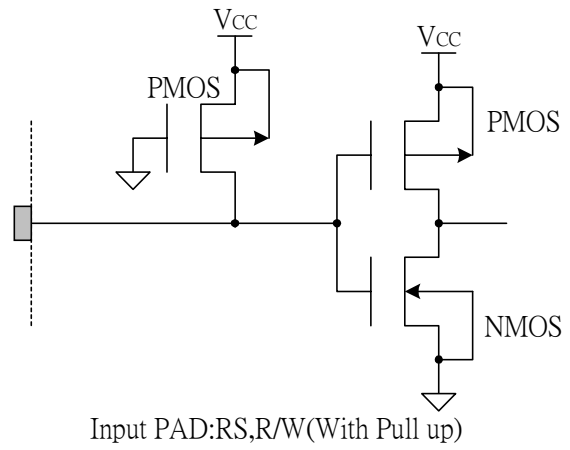
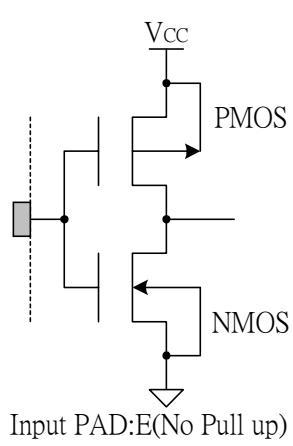
- Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/11 duty; 1/4 bias,1 frame = 3.7us x 400 x 11 = 16280us=16.3ms (61.3Hz)



- Assume the oscillation frequency is 270KHZ, 1 clock cycle time = 3.7us, 1/8 duty; 1/4 bias, 1 frame = 3.7us x 400 x 8 = 11840us=11.8ms (84.7Hz)

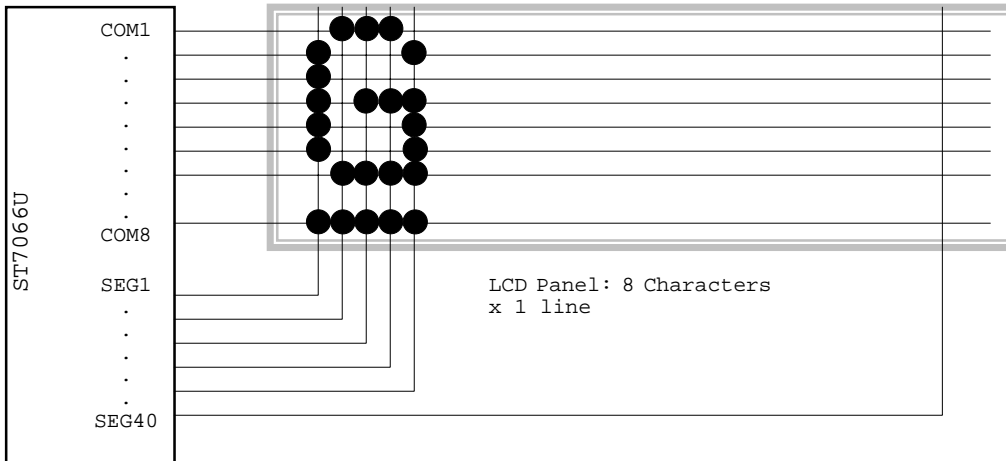


I/O Pad Configuration

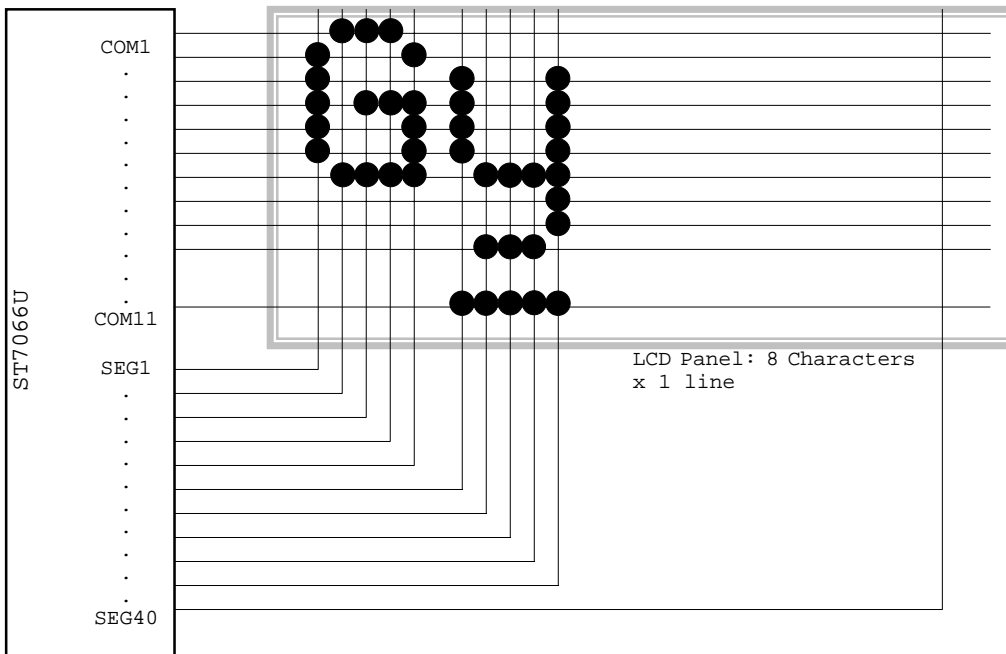


■ LCD and ST7066U Connection

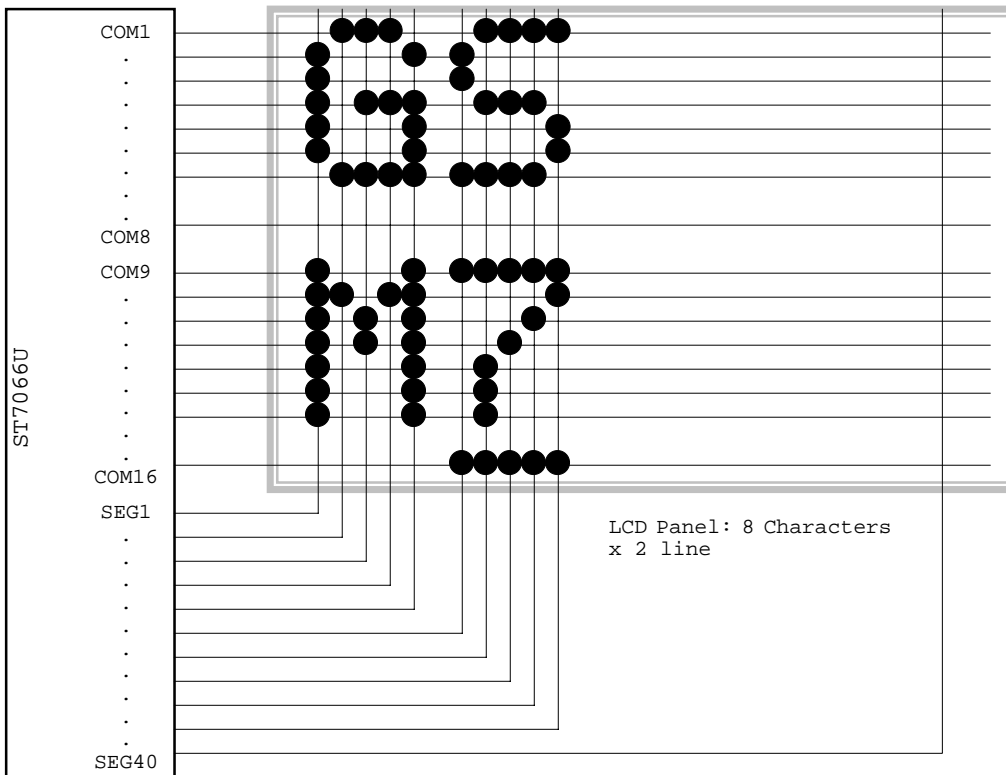
1. 5x8 dots, 8 characters x 1 line (1/4 bias, 1/8 duty)



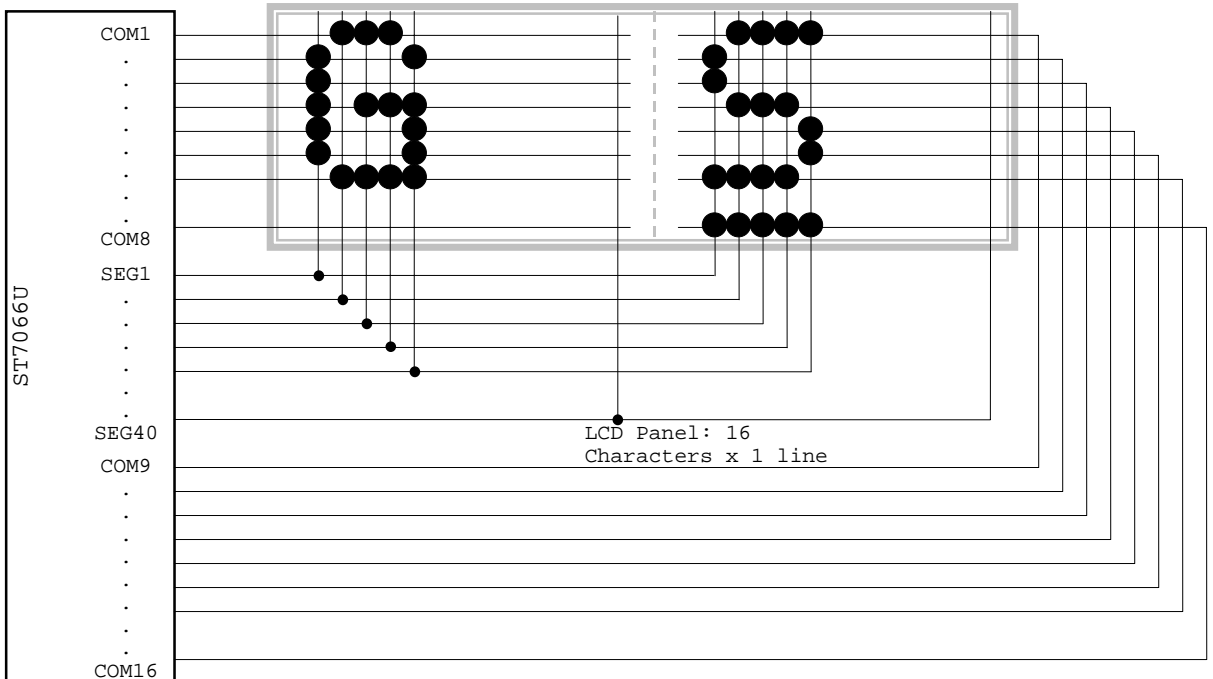
2. 5x11 dots, 8 characters x 1 line (1/4 bias, 1/11 duty)



3. 5x8 dots, 8 characters x 2 line (1/5 bias, 1/16 duty)



4. 5x8 dots, 16 characters x 1 line (1/5 bias, 1/16 duty)



Application Circuit

