SPEAr1310 embedded microprocessor

Dual ARM® Cortex®-A9 cores enable high-performance, high-connectivity and industrial applications

ST's SPEAr1310 is a part of the growing SPEAr family of embedded MPUs for networking.

It offers an unprecedented combination of processing performance and extreme power reduction control for next-generation communication applications.

The SPEAr1310 is based on ARM's new multicore technology (Cortex-A9 SMP/AMP), and is manufactured using ST's 55 nm HCMOS low-power silicon process.

Key features

- CPU subsystem
  - Dual ARM Cortex-A9 cores, 600 MHz
  - Supports both symmetric (SMP) and asymmetric (AMP) multiprocessing
  - 32 + 32-Kbyte L1 instruction/data cache per core with parity check
  - Shared 512-Kbyte L2 cache (ECC protected)
  - Accelerator coherence port
- Bus: 64-bit multilayer network-on-chip
- Memories
  - 32 Kbyte boot ROM
  - 32 Kbyte internal SRAM
  - Multiport controller (MPMC) for external DDR2-800/DDR3-1066
  - Controller (FSMC) for external Flash and SRAM
  - Controller (SMI) for external serial NOR Flash
- Controls external peripherals
  - TFT LCD display up to 1920 x 1080 (60 Hz)
  - Touchscreen I/F
  - 9 x 9 keyboard
  - Memory card interface
- Connectivity
  - Giga/Fast Ethernet ports
  - 3x PCIe 2.0 / SATA
  - 3x USB 2.0 (Host/OTG)
  - 2x CAN 2.0 a/b interfaces
  - 2x HDLC RS485
  - I²S, UART, I²C and SPI
- Expansion interface (EXPI)
- Security: C3 cryptographic accelerator
- Power saving
  - Power islands for leakage reduction
  - IP clock gating for dynamic power reduction
  - Dynamic frequency scaling
- Package: PBGA628 (23 x 23 mm, 0.8 mm pitch)

Overview

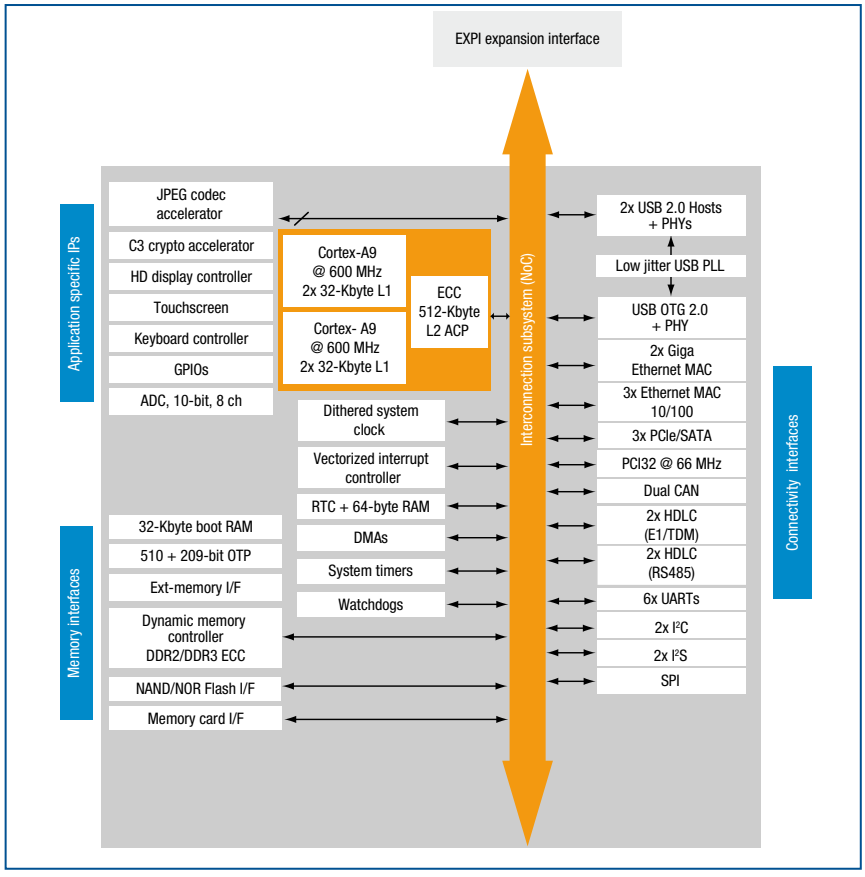
The SPEAr1310 combines two ARM Cortex-A9 cores with a DDR3 (third-generation, double-data-rate) memory interface. Together with ST's low-power 55 nm HCMOS process technology, the SPEAr1310 delivers high computing power and customizability for a variety of embedded applications, with a high degree of cost competitiveness. The dual processors support both fully symmetric and asymmetric operations, at speeds of 600 MHz (industrial worst-case conditions) for an equivalent of 3000 DMIPS.

In addition to unrivalled low power and multiprocessing capabilities, this new eMPU offers the innovative network-on-chip (NoC) technology. NoC is a flexible communications architecture that enables multiple and different traffic profiles while maximizing data throughput in the most performance and power-efficient way.

Equipped with an integrated DDR2/DDR3 memory controller and a full set of connectivity peripherals, including USB, SATA, PCIe (with integrated PHY) and Giga Ethernet MAC, the SPEAr1310 targets high-performance, embedded-control applications across the communication, computer peripherals and industrial automation markets.

Cache memory coherency with hardware accelerators and I/O blocks increases throughput and simplifies software development. The accelerator coherency port (ACP), together with the device's NoC routing capabilities, addresses the latest application requirements for hardware acceleration and I/O performance. ECC (error correction coding) protection against soft and hard errors on both DRAM and L2 cache memories significantly improves the mean-time-between-failures for enhanced reliability.

SPEAr1310 block diagram



Design support

Information on development tools and evaluation boards, as well as downloads of the latest STLinux OS, firmware, and technical documentation, can be found on:

www.st.com/spear