PIC32MX110/120/210/220 Family Silicon Errata and Data Sheet Clarification

The PIC32MX110/120/210/220 family devices that you have received conform functionally to the current Device Data Sheet (DS61168**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX110/120/210/220 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A0**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with the REAL ICE™ in-circuit emulator:

1. Using the appropriate interface, connect the device to the REAL ICE in-circuit emulator.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX110/120/210/220 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		A0
PIC32MX110F016B	0x04A07053	0x0
PIC32MX110F016C	0x04A09053	
PIC32MX110F016D	0x04A0B053	
PIC32MX120F032B	0x04A06053	
PIC32MX120F032C	0x04A08053	
PIC32MX120F032D	0x04A0A053	
PIC32MX210F016B	0x04A01053	
PIC32MX210F016C	0x04A03053	
PIC32MX210F016D	0x04A05053	
PIC32MX220F032B	0x04A00053	
PIC32MX220F032C	0x04A02053	
PIC32MX220F032D	0x04A04053	

Note 1: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A0
Voltage Regulator	BOR	1.	Device may not exit BOR state if BOR event occurs.	X
Oscillator	Clock Switch	2.	If a Fail-Safe Clock Monitor (FSCM) event occurs when Primary Oscillator (POSC) mode is used, firmware clock switch requests to switch from FRC mode will fail.	X
I^2C™	Slave Mode	3.	The I^2C module does not respond to address 0x78 when the STRICT and A10M bits are cleared in the I2CxCON register.	X
USB	UIDLE Interrupt	4.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	X
ADC	—	5.	The DNL parameter of the ADC module is not within the published data sheet specifications when the ADC module is operating at maximum conversion rate.	X
ADC	CTMU Calibration	6.	Open selection for Channel 0 positive input is not functional.	X
ADC	Conversion Trigger from INT0 Interrupt	7.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	X
Parallel Master Port (PMP)	Address Pins	8.	When the Parallel Master Port (PMP) module is enabled, address pins cannot be used as GPIO output pins.	X
I/O Ports	RA0 and RA1 Output	9.	Output High Voltage (VOH) on pins RA0 and RA1 is not within the published data sheet specification.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A0**).

1. Module: Voltage Regulator

Device may not exit BOR state if BOR event occurs.

Work arounds

Work around 1:

VDD must remain within the published specification (see parameter DC10 of the device data sheet).

Work around 2:

Reset device by providing POR condition.

Affected Silicon Revisions

A0							
X							

2. Module: Oscillator

If the Primary Oscillator (POSC) mode is implemented and a Fail-Safe Clock Monitor (FSCM) event occurs (failure of the external primary clock), the internal clock source will switch to the FRC oscillator. Subsequent firmware clock switch requests from the FRC oscillator to other clock sources will fail and the device will continue to execute on the FRC oscillator. Upon repair of the external clock source and a power-on state, the device will resume operation with the primary oscillator clock source.

Work around

None.

Affected Silicon Revisions

A0							
X							

3. Module: I²C™

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I^2C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but does not.

Work around

None.

Affected Silicon Revisions

A0							
X							

4. Module: USB

In the case where the bus has been idle for > 3 ms, and the UIDLE interrupt flag is set, if software clears the interrupt flag, and the bus remains idle, the UIDLE interrupt flag will not be set again.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption. (Resume, Reset, SOF, or Error).

Note:	Resume and Reset are the only interrupts that should be gotten following UIDLE assertion. If, at any point in time, the UIDLE bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). Note that this will require software to clear the UIDLE interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

A0							
X							

5. Module: ADC

If the ADC module is configured to operate at a maximum conversion rate of 1.1 Msps, missing codes are possible every 2^5 codes and the DNL parameter will not be within the published specification.

Work around

Configure the ADC module to operate for a maximum conversion rate of 500 ksps.

Affected Silicon Revisions

A0							
X							

6. Module: ADC

If the ADC module is used in conjunction with the CTMU module in Absolute Capacitive/Time Measurement mode, Channel 0 positive input must remain open (CH0SA<3:0> = 1111 or CH0SB<3:0> = 1111) during calibration step. However, open selection for Channel 0 positive input is not functional and connects this input to AVSS.

Work around

Use ADC and CTMU for relative capacitive/time measurement, where calibration step is not required.

Affected Silicon Revisions

A0							
X							

7. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternatively, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

A0							
X							

8. Module: Parallel Master Port (PMP)

If the PMP module is enabled, any pin with a PMP addressing capability (PMAx) cannot be used as a general purpose output pin, even when the corresponding PTEN<10:0> bit in the PMAEN register is cleared. All other functionality on these pins, including GPIO input functionality is not affected.

Work around

To use a GPIO pin as an output when this pin is shared with PMP addressing functionality and PMP is enabled, do the following:

1. Enable PMP addressing by setting the corresponding PTEN<10:0> bit in the PMAEN register.
2. Instead of using corresponding LATx registers to output GPIO data, use the PMADDR register.

Affected Silicon Revisions

A0							
X							

9. Module: I/O Ports

Output High Voltage (VOH) on pins RA0 and RA1 is not within the published data sheet specification.

Work around

Disable slew rate control of the I^2C1 module by setting the DISSLW bit (I2C1CON<9>).

Affected Silicon Revisions

A0							
X							

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS61168**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None to report at this time.

APPENDIX A: REVISION HISTORY

Rev A Document (10/2011)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (Voltage Regulator), 2 (Oscillator), 3 (I^2C™), 4 (USB), 5 (ADC), 6 (ADC), 7 (ADC), 8 (Parallel Master Port (PMP)), and 9 (I/O Ports).

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