

256-TAPS DUAL CHANNEL DIGITAL POTENTIOMETER WITH SPI INTERFACE AND NON-VOLATILE MEMORY

Check for Samples: [TPL0202](#)

FEATURES

- Dual Channel, 256-Position Resolution
- Non-volatile Memory Stores Wiper Settings
- 2mm x 2mm, 14-pin MicroQFN or 3mm x 3mm, 16-pin QFN Packages
- 10 kΩ End-to-End Resistance (TPL0202-10)
- Fast Power-up Response Time: <math><100\mu\text{s}</math>
- ± 1 LSB INL, ± 0.5 LSB DNL (Voltage-Divider Mode)
- 12 ppm/ $^{\circ}\text{C}$ Ratiometric Temperature Coefficient
- SPI-Compatible Serial Interface
- 2.7 V to 5.5 V Single-Supply Operation
- Operating Temperature Range From -40°C to $+85^{\circ}\text{C}$
- ESD Performance Tested Per JESD 22
 - 2000-V Human Body Model (A114-B, Class II)

APPLICATIONS

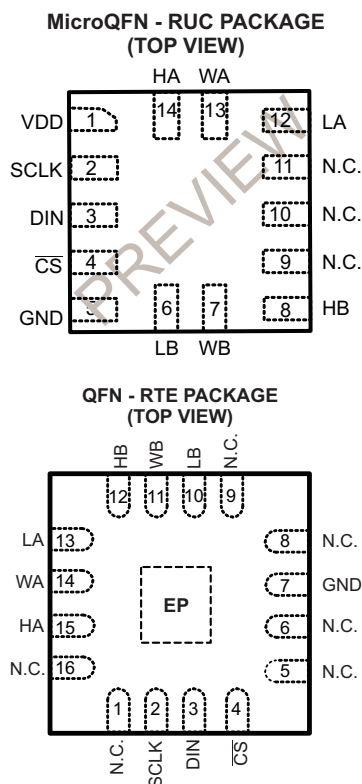
- Adjustable Gain Amplifiers and Offset Trimming
- Adjustable Power Supplies
- Precision Calibration of Set Point Thresholds
- Sensor Trimming and Calibration
- Mechanical Potentiometer Replacement

DESCRIPTION

The TPL0202 is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0202-10 has an end-to-end resistance of 10kΩ.

The TPL0202 has non-volatile memory (EEPROM) which can be used to store the wiper position. The internal registers of the TPL0202 can be accessed using a SPI-compatible digital interface.

The TPL0202 is available in a 14-pin MicroQFN (2mm x 2mm) and 16-pin QFN (3mm x 3mm) package with a specified temperature range of -40°C to $+85^{\circ}\text{C}$.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

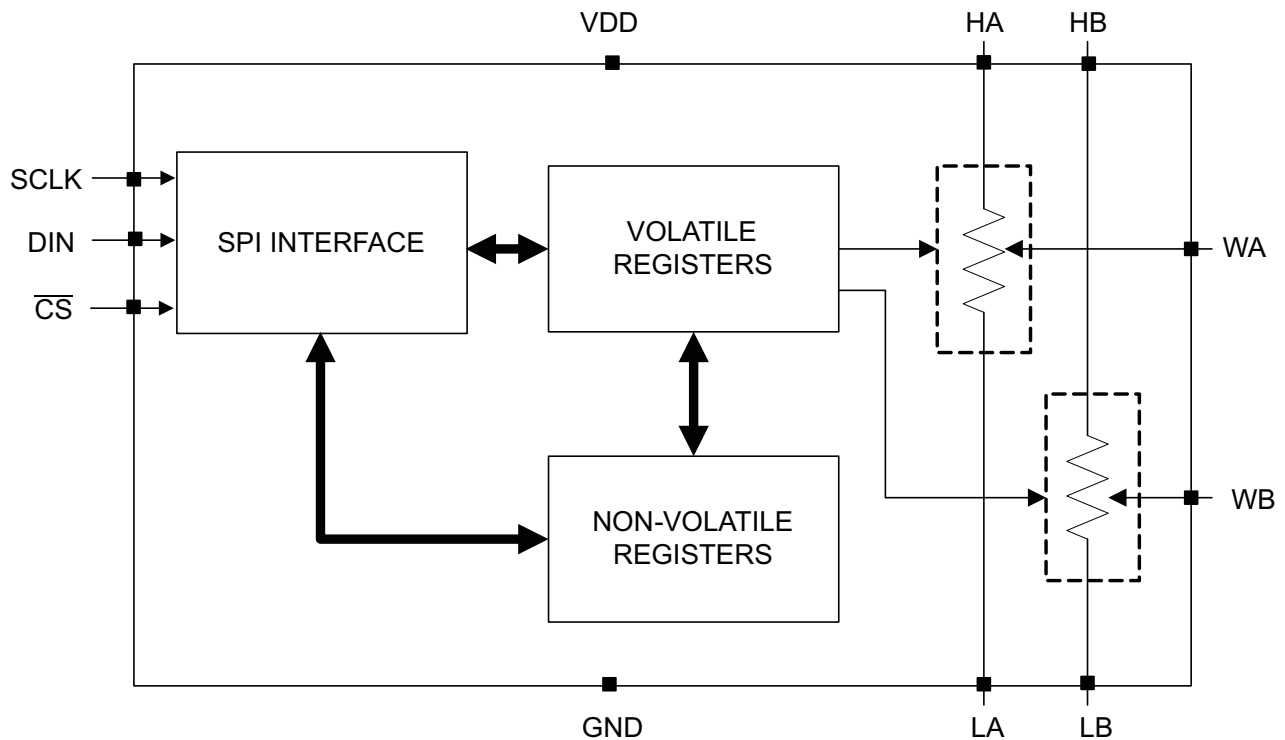
| T _A | PACKAGE ⁽¹⁾ (2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------------|---------------|-----------------------|------------------|
| -40°C to 85°C | QFN – RTE | Tape and reel | TPL0202-10MRTER | ZUR |
| | QFN – RUC | | TPL0202-10RUCR | TBD |

- (1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. Summary of Features

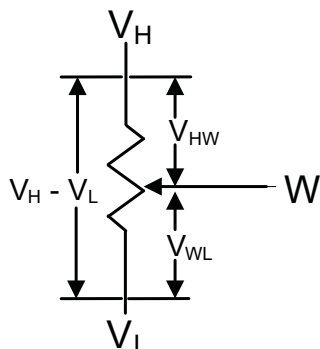
| Feature | TPL0202-10 |
|---------------------------------|-----------------------------------|
| # of Potentiometers | 2 |
| Digital Interface | SPI |
| Steps | 256 |
| Wiper Memory | Non-Volatile |
| Taper | Linear |
| End-to-end Resistance | 10kΩ |
| End-to-end Resistance Tolerance | 20% |
| Wiper Resistance | 25 Ω (typ) |
| Smallest Package Size | MicroQFN (RUC): 4 mm ² |

FUNCTIONAL BLOCK DIAGRAM



DIGITAL POTENTIOMETER CONFIGURATIONS

VOLTAGE DIVIDER MODE

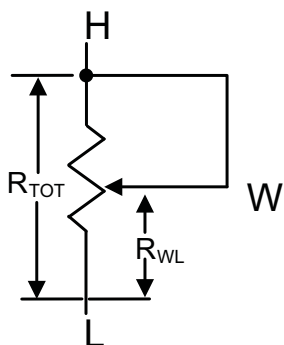


$$V_{HW} = (V_H - V_L) \times (1 - (D/256))$$

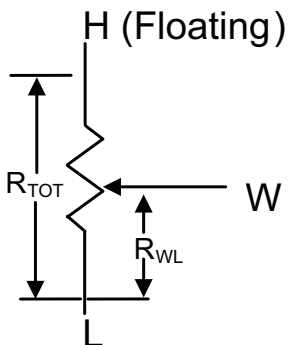
$$V_{WL} = (V_H - V_L) \times D/256$$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE A



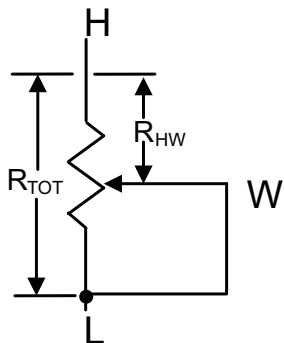
OR



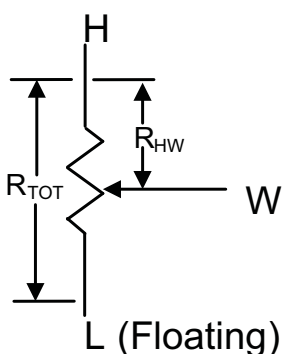
$$R_{WL} = R_{TOT} \times D/256$$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE B



OR



$$R_{HW} = R_{TOT} \times (1 - (D/256))$$

Where D = Decimal Value of Wiper Code

Figure 1. DPOT Configurations

Table 2. PIN DESCRIPTION TABLE

| 16 RTE | 14 RUC | PIN NAME | TYPE | DESCRIPTION |
|--------|--------|------------------------|--------|---|
| 1 | 1 | VDD | Power | Supply Voltage |
| 2 | 2 | SCLK | Input | SPI Clock |
| 3 | 3 | DIN | Input | SPI Input |
| 4 | 4 | $\overline{\text{CS}}$ | Input | SPI Chip Select (Active Low) |
| 5 | 9 | N.C. | – | Not internally connected |
| 6 | 10 | N.C. | – | Not internally connected |
| 7 | 5 | GND | Ground | Ground |
| 8 | – | N.C. | – | Not internally connected |
| 9 | 11 | N.C. | – | Not internally connected |
| 10 | 6 | LB | I/O | Low terminal of Potentiometer B |
| 11 | 7 | WB | I/O | Wiper terminal of Potentiometer B |
| 12 | 8 | HB | I/O | High terminal of Potentiometer B |
| 13 | 12 | LA | I/O | Low terminal of Potentiometer A |
| 14 | 13 | WA | I/O | Wiper terminal of Potentiometer A |
| 15 | 14 | HA | I/O | High terminal of Potentiometer A |
| 16 | – | N.C. | – | Not internally connected |
| EP | - | EP | - | Exposed Thermal Pad. Can be connected to GND or left unconnected. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾⁽³⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------------|--|-------------|----------------|------|
| V_{DD} to GND | Supply voltage range | -0.3 | 7 | V |
| All other pins to GND | | -0.3 | $V_{DD} + 0.3$ | |
| I_L | Pulse Current | | ± 20 | mA |
| I_W I_H | Continuous Current | | ± 2 | mA |
| θ_{JA} | Package Thermal Impedance ⁽⁴⁾ | RTE package | 56.4 | °C/W |
| | | RUC package | 216.7 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS

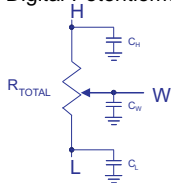
V_{DD} = 2.7V to 5.5V, T_A = -40°C to 85°C (unless otherwise noted). Typical values are at V_{DD} = 5V, T_A = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------|------|-----------------|--------|
| R _{TOT} | End-to-end Resistance (Between H and L Terminals) | | 8 | 10 | 12 | kΩ |
| V _H , V _L | Terminal voltage range | | 0 | | V _{DD} | V |
| R _H , R _L | Terminal resistance | | | 60 | 200 | Ω |
| R _W | Wiper resistance | | | 25 | 100 | Ω |
| C _H , C _L ⁽¹⁾⁽²⁾ | Terminal capacitance | | | 22 | | pF |
| C _W ⁽¹⁾⁽²⁾ | Wiper capacitance | | | 18 | | pF |
| I _{LKG} | Terminal Leakage Current | V _H = V _{SS} to V _{DD} , V _L = Floating OR V _L = V _{SS} to V _{DD} , V _H = Floating | | 0.1 | 1 | μA |
| TC _R | Resistance temperature coefficient | Input Code = 0x80h | | 132 | | ppm/°C |
| R _{TOT, MATCH} | Channel-to-channel resistance match | | | 0.1 | | % |
| Voltage Divider Mode | | | | | | |
| INL ⁽³⁾⁽⁴⁾ | Integral non-linearity | | -1 | | 1 | LSB |
| DNL ⁽³⁾⁽⁵⁾ | Differential non-linearity | | -0.5 | | 0.5 | LSB |
| Z _{ERROR} ⁽⁶⁾⁽⁷⁾ | Zero-scale error | | 0 | 2 | 5 | LSB |
| F _{ERROR} ⁽⁶⁾⁽⁸⁾ | Full-scale error | | -5 | -2 | 0 | LSB |
| V _{MATCH} ⁽⁶⁾⁽⁹⁾ | Channel-to-Channel matching | Wiper at the same tap position, same voltage all H and the same voltage at all L terminals | -2 | | 2 | LSB |
| TC _V | Ratiometric temperature coefficient | Wiper set at mid-scale | | 12 | | ppm/°C |
| BW | Bandwidth | Wiper set at mid-scale C _{LOAD} = 10 pF | | 2000 | | kHz |
| T _{SW} | Wiper setting time | | | 0.4 | | μS |
| THD | Total harmonic distortion | V _H = 1 V _{RMS} at 1 kHz, V _L = V _{DD} /2, Measurement at W | | 0.03 | | % |
| X _{TALK} | Crosstalk | f _H = 1 kHz, V _L = GND, Measurement at W | | -94 | | dB |

(1) Terminal and Wiper Capacitance extracted from self admittance of three port network measurement

$$Y_{ii} = \frac{I_i}{V_i} \Big|_{V_k=0 \text{ for } k \neq i}$$

(2) Digital Potentiometer Macromodel



- (3) $LSB = (V_{MEAS[code\ 255]} - V_{MEAS[code\ 0]}) / 255$
- (4) $INL = ((V_{MEAS[code\ x]} - V_{MEAS[code\ 0]}) / LSB) - [code\ x]$
- (5) $DNL = ((V_{MEAS[code\ x]} - V_{MEAS[code\ x-1]}) / LSB) - 1$
- (6) $IDEAL_LSB = (V_H - V_L) / 256$
- (7) $Z_{ERROR} = V_{MEAS[code\ 0]} / IDEAL_LSB$
- (8) $F_{ERROR} = ((V_{MEAS[code\ 255]} - (V_H - V_L)) / IDEAL_LSB) + 1$
- (9) $V_{MATCH} = (V_{MEAS_A[code\ x]} - V_{MEAS_B[code\ x]}) / IDEAL_LSB$

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = 2.7V$ to $5.5V$, $T_A = -40^\circ C$ to $85^\circ C$ (unless otherwise noted). Typical values are at $V_{DD} = 5V$, $T_A = 25^\circ C$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------------------|--|------|-----|-----|------|
| RHEOSTAT MODE (Measurements between W and L with H not connected, or between W and H with L not connected) | | | | | | |
| RINL ⁽¹⁰⁾⁽¹¹⁾ | Integral non-linearity | | -1.5 | | 1.5 | LSB |
| RDNL ⁽¹⁰⁾⁽¹²⁾ | Differential non-linearity | | -0.5 | | 0.5 | LSB |
| R _{OFFSET} ⁽¹³⁾⁽¹⁴⁾ | Offset | | 0 | 2.5 | 7 | LSB |
| R _{MATCH} ⁽¹³⁾⁽¹⁵⁾ | Channel-to-Channel matching | | -2 | | 2 | LSB |
| RBW | Bandwidth | Code = 0x00h, L Floating, Input applied to W, Measure at H, C _{LOAD} = 10 pF | | 400 | | kHz |

(10) $RLSB = (R_{MEAS[code\ 255]} - R_{MEAS[code\ 0]}) / 255$

(11) $RINL = ((R_{MEAS[code\ x]} - R_{MEAS[code\ 0]}) / RLSB) - [code\ x]$

(12) $RDNL = ((R_{MEAS[code\ x]} - R_{MEAS[code\ x-1]}) / RLSB) - 1$

(13) $IDEAL_RLSB = R_{TOT} / 256$

(14) $R_{OFFSET} = R_{MEAS[code\ 0]} / IDEAL_RLSB$

(15) $R_{MATCH} = (R_{MEAS_A[code\ x]} - R_{MEAS_B[code\ x]}) / IDEAL_RLSB$

OPERATING CHARACTERISTICS

$V_{DD} = 2.7V$ to $5.5V$, $V_H = V_{DD}$, $V_L = GND$, $T_A = -40^\circ C$ to $85^\circ C$ (unless otherwise noted). Typical values are at $V_{DD} = 5V$, $T_A = 25^\circ C$ (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|-----------------------|---------|-----|--------|
| I _{DD(STBY)} | V _{DD} supply current during standby | Digital Inputs = V _{DD} or GND | | 1 | 5 | μA |
| I _{DD} | V _{DD} supply current during write cycle only | Digital Inputs = V _{DD} or GND | | | 400 | μA |
| I _{IN-DIG} | Digital pins leakage current (SCLK, DIN, CS inputs) | | -1 | | 1 | μA |
| V _{POR} | Power-on recall voltage | Minimum V _{DD} at which memory recall occurs | | 2 | | V |
| EEPROM Specification | | | | | | |
| | EEPROM endurance | | | 100,000 | | Cycles |
| | EEPROM retention | T _A = 85 °C | | 100 | | Years |
| t _{BUSY} | Write NV register busy time | | | 20 | | ms |
| t _{ACC} | Read NV register access time | | | 40 | | ns |
| t _{WO} | Write wiper register to output delay | | | 40 | | ns |
| t _D | Power-up Response Time (V _{DD} above V _{POR} to wiper register value recall completed) | | | 35 | 100 | μs |
| Serial Interface Specifications (SCLK, DIN, CS Inputs) | | | | | | |
| V _{IH} | Input high voltage | V _{DD} = 3.6 V to 5.5 V | 2.4 | | 5.5 | V |
| | | V _{DD} = 2.7 V to 3.6 V | 0.7 × V _{DD} | | 5.5 | |
| V _{IL} | Input low voltage | SCLK, DIN, CS inputs | 0 | | 0.8 | V |
| C _{IN} | Pin capacitance | SCLK, DIN, CS inputs | | 7 | | pF |

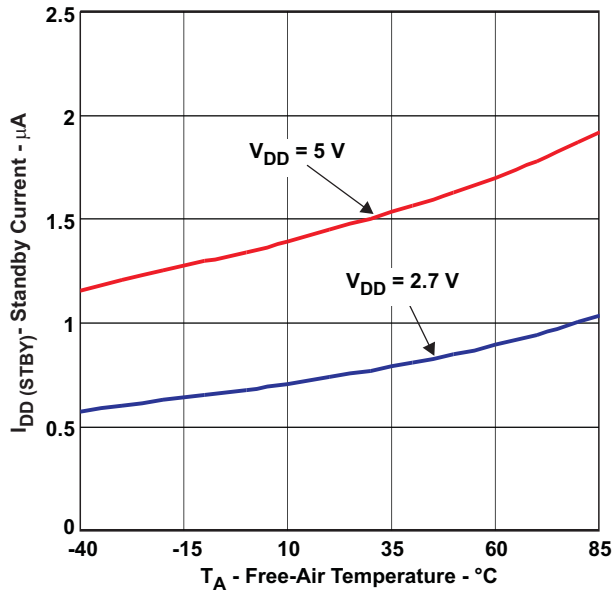
SPI INTERFACE TIMING REQUIREMENTS

$V_{DD} = 2.7V$ to $5.5V$, $V_H = V_{DD}$, $V_L = GND$, $T_A = -40^{\circ}C$ to $85^{\circ}C$ (unless otherwise noted)

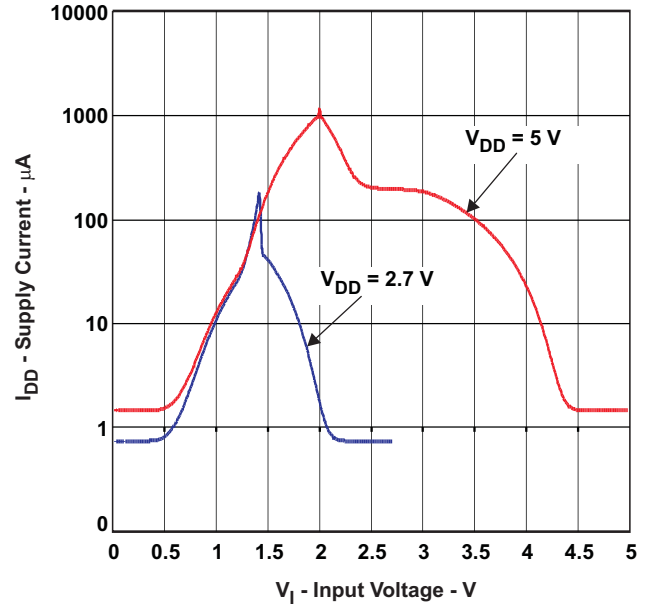
| | | MIN | TYP | UNLTD |
|------------|--|-----|-----|-------|
| f_{SCLK} | SCLK frequency | | 5 | MHz |
| t_{SCP} | SCLK period | 200 | | ns |
| t_{SCH} | SCLK high time | 80 | | ns |
| t_{SCL} | SCLK low time | 80 | | ns |
| t_{CSS} | \overline{CS} fall to SCLK rise setup time | 80 | | ns |
| t_{CSH} | SCLK rise to \overline{CS} hold time | 0 | | ns |
| t_{DS} | DIN to SCLK setup time | 50 | | ns |
| t_{DH} | DIN hold after SCLK rise to \overline{CS} fall | 0 | | ns |
| t_{CS0} | SCLK rise to \overline{CS} fall | 20 | | ns |
| t_{CS1} | \overline{CS} rise to SCLK rise hold | 80 | | ns |
| t_{CSW} | \overline{CS} pulse width high | 200 | | ns |

TYPICAL PERFORMANCE CURVES

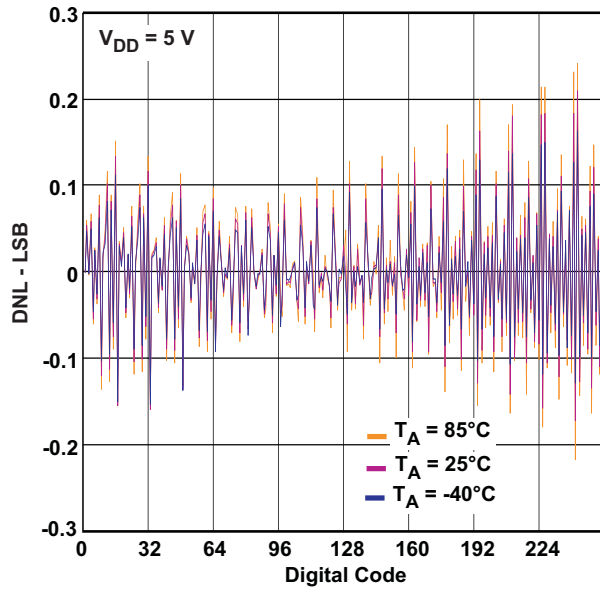
STANDBY CURRENT
vs
TEMPERATURE



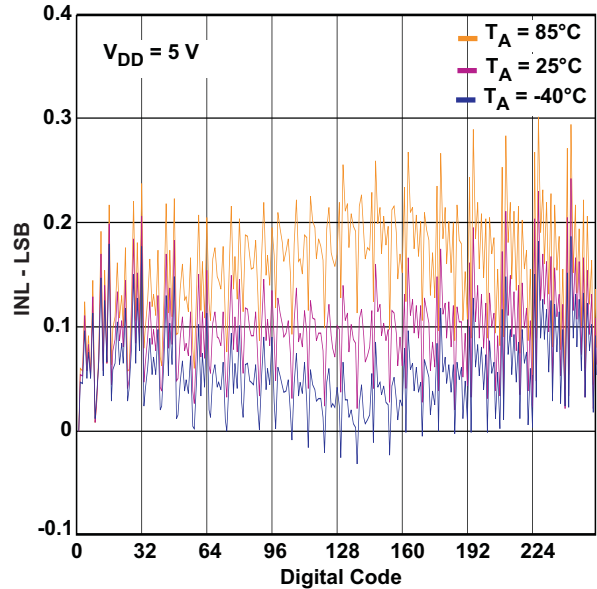
SUPPLY CURRENT
vs
DIGITAL INPUT VOLTAGE



VOLTAGE DIVIDER MODE DNL
vs
TEMPERATURE (V_DD = 5V)

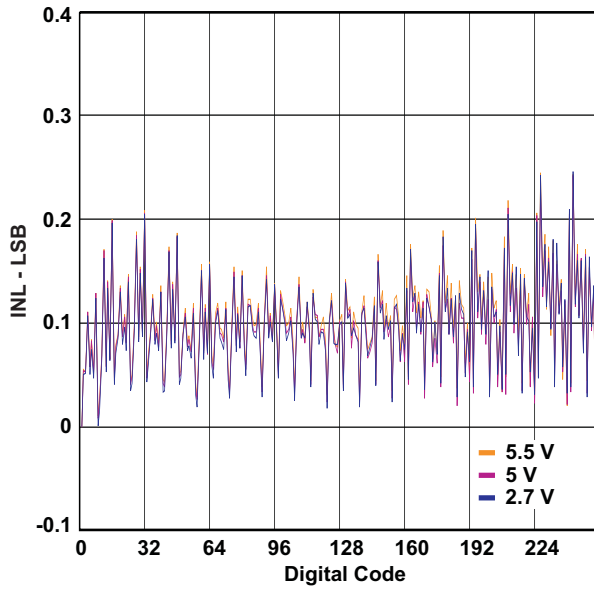


VOLTAGE DIVIDER MODE INL
vs
TEMPERATURE (V_DD = 5V)

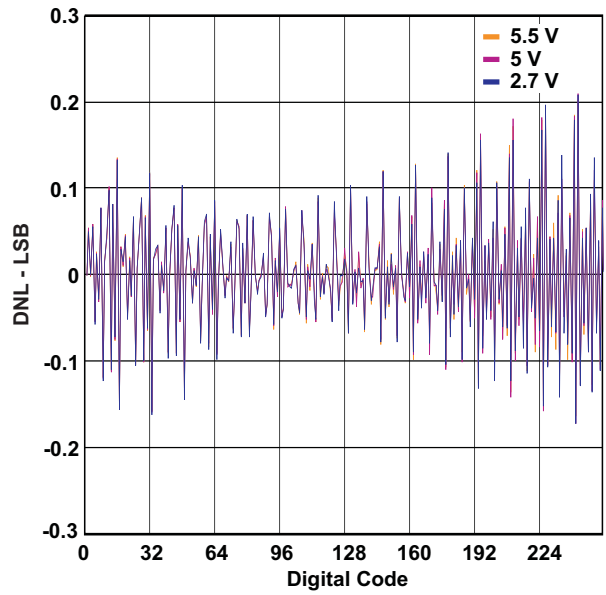


TYPICAL PERFORMANCE CURVES (continued)

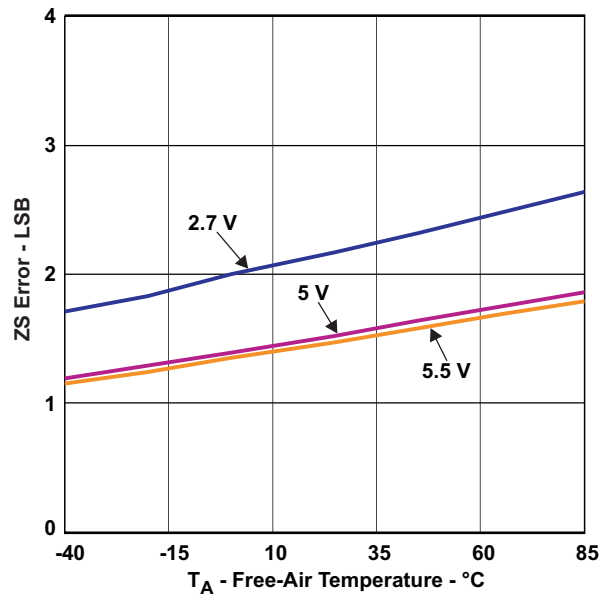
VOLTAGE DIVIDER MODE INL
vs
SUPPLY VOLTAGE (25°C)



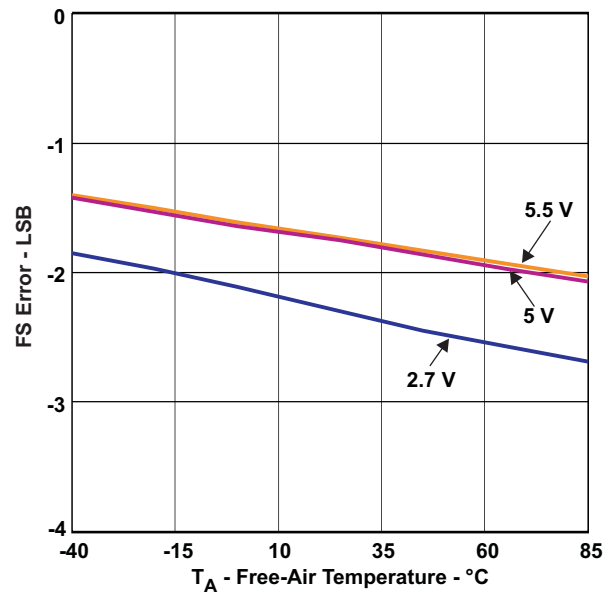
VOLTAGE DIVIDER MODE DNL
vs
SUPPLY VOLTAGE (25°C)



VOLTAGE DIVIDER MODE ZS ERROR
vs
TEMPERATURE

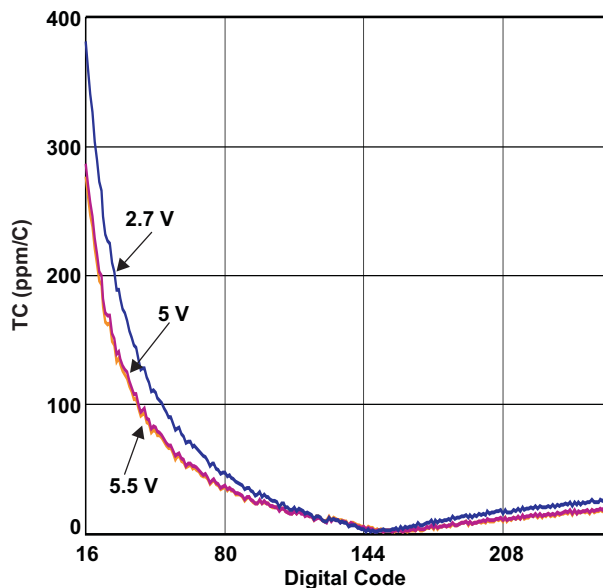


VOLTAGE DIVIDER MODE FS ERROR
vs
TEMPERATURE

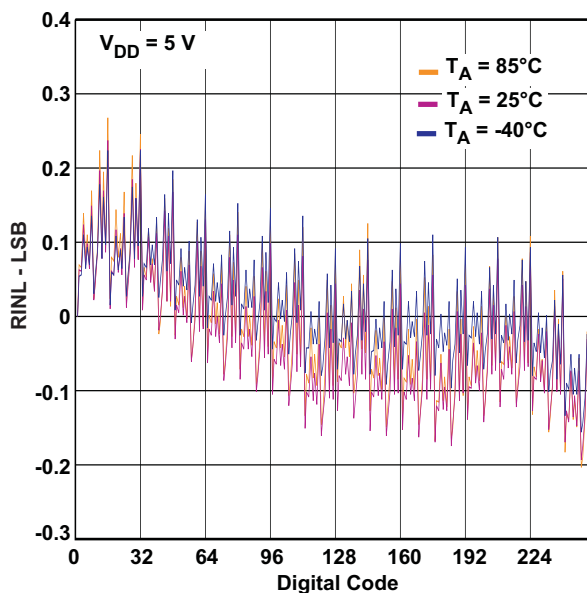


TYPICAL PERFORMANCE CURVES (continued)

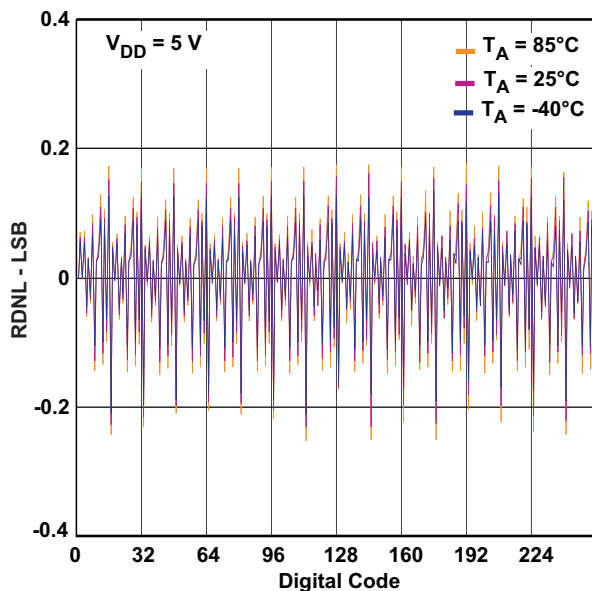
VOLTAGE DIVIDER MODE
vs
DIGITAL CODE



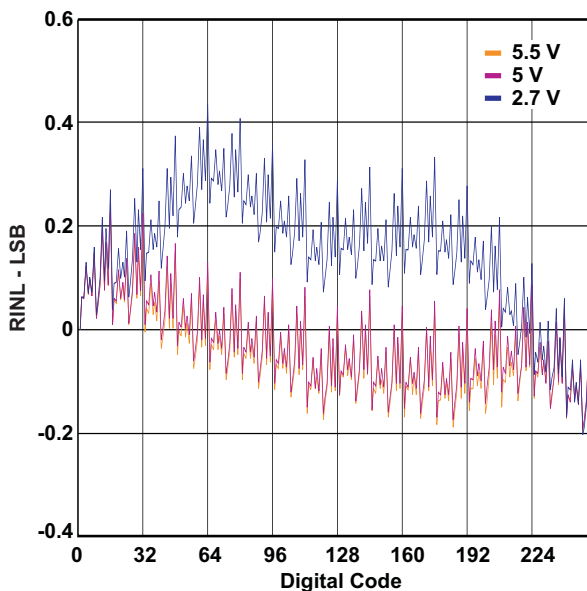
RHEOSTAT MODE RINL
vs
TEMPERATURE ($V_{DD} = 5V$)



RHEOSTAT MODE RDNL
vs
TEMPERATURE ($V_{DD} = 5V$)

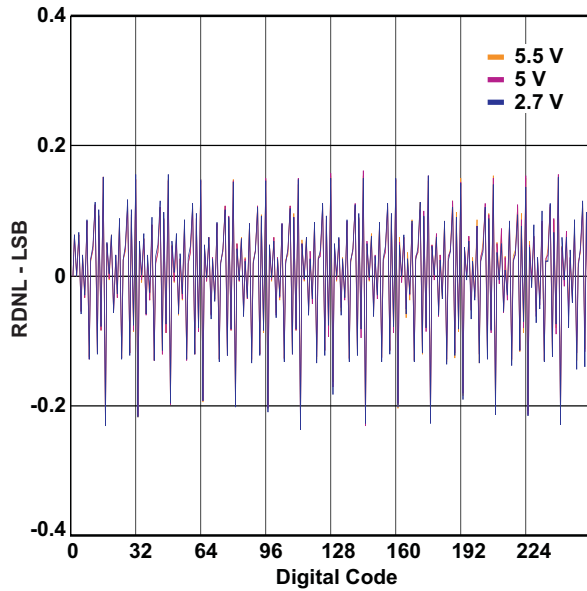


RHEOSTAT MODE RINL
vs
SUPPLY VOLTAGE (25°C)

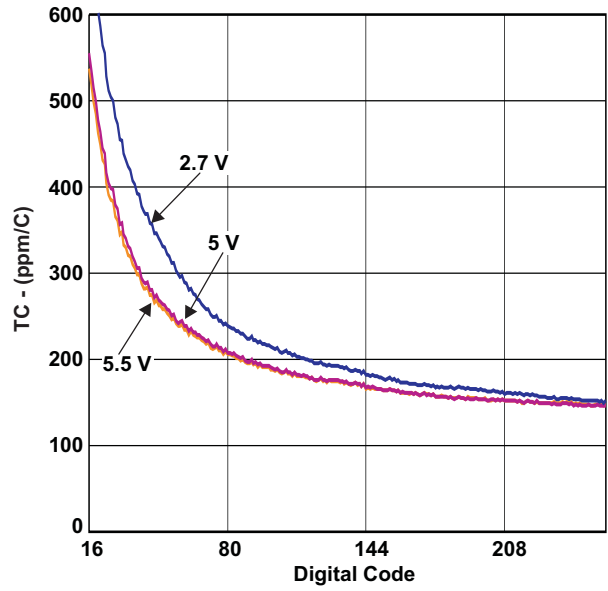


TYPICAL PERFORMANCE CURVES (continued)

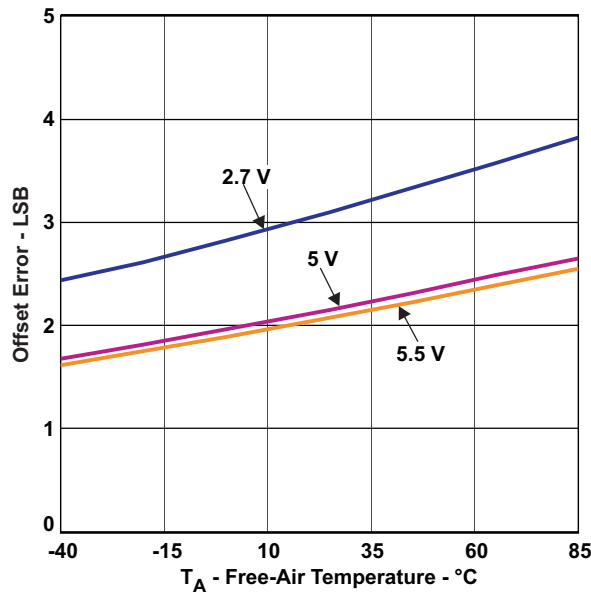
RHEOSTAT MODE RINL
vs
SUPPLY VOLTAGE (25°C)



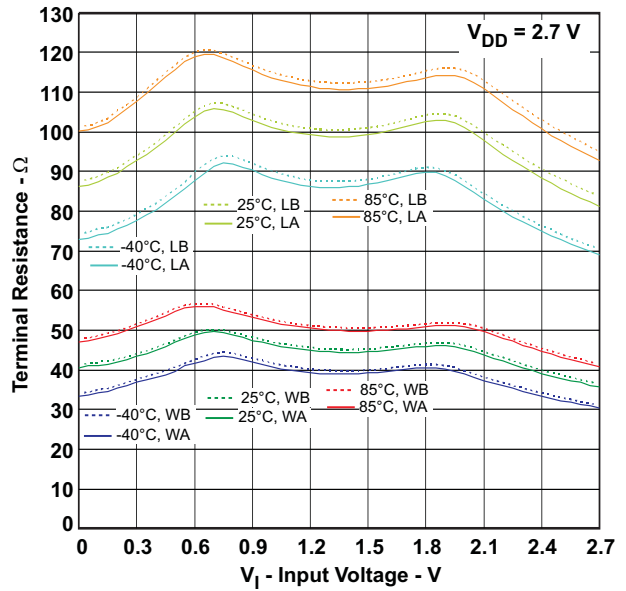
RHEOSTAT MODE TC
vs
DIGITAL CODE



RHEOSTAT MODE OFFSET ERROR
vs
TEMPERATURE

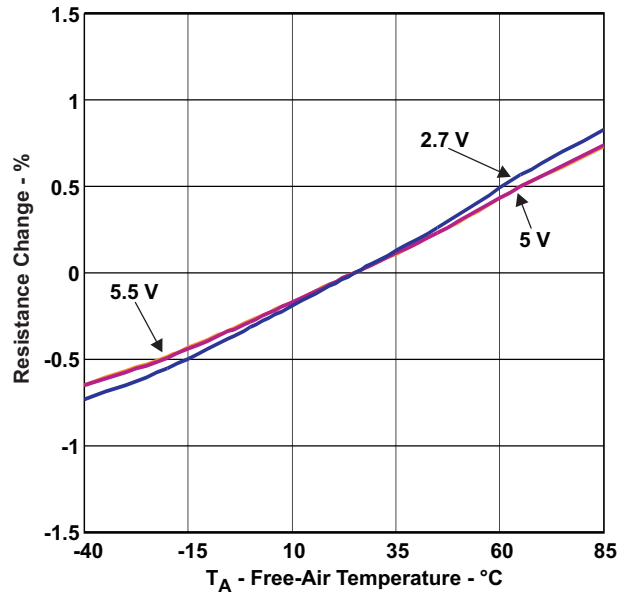
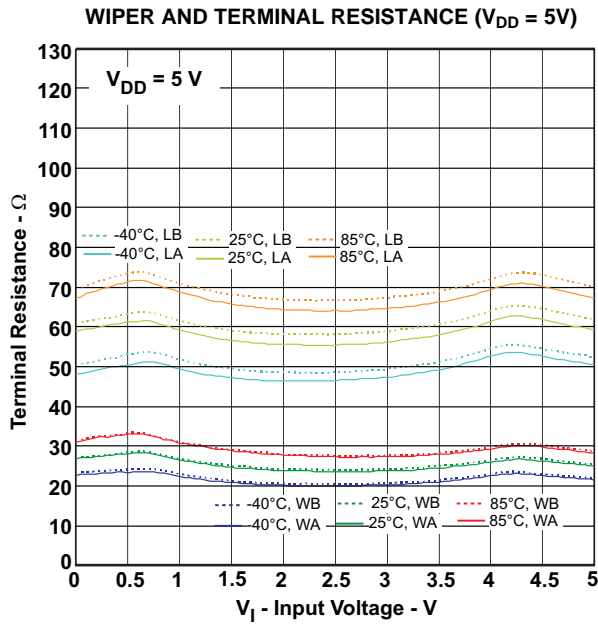


WIPER AND TERMINAL RESISTANCE (V_{DD} = 2.7V)

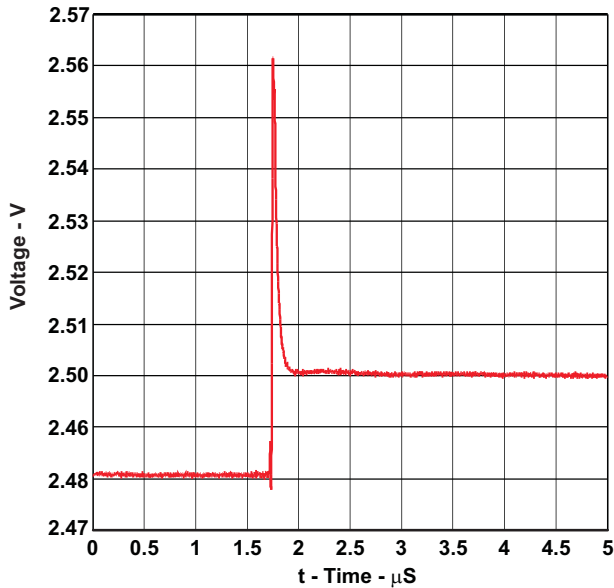


TYPICAL PERFORMANCE CURVES (continued)

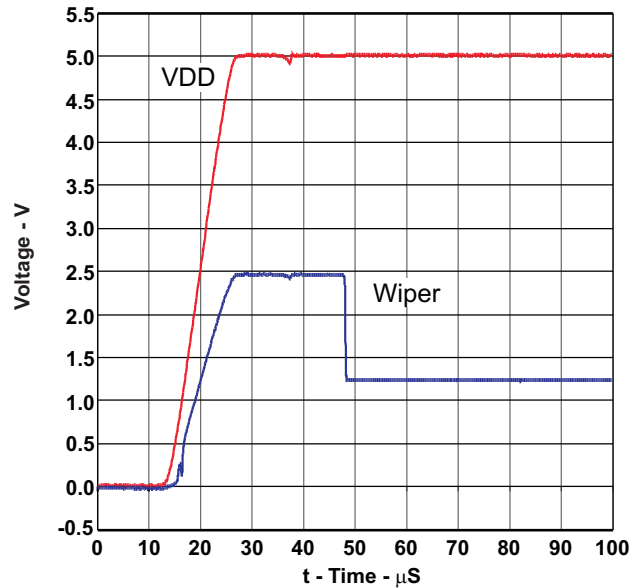
END-END RESISTANCE CHANGE
vs
TEMPERATURE



MIDSCALE WIPER GLITCH (CODE 7Fh to 80h)
 $V_{DD} = 5V, V_H = V_{DD}, V_L = GND, C_{LOAD} = 10pF$



T_{POR} (POWER-UP RESPONSE TIME)
NON-VOLATILE MEMORY = 40h



SPI DIGITAL INTERFACE

The TPL0202 uses a 3-wire SPI-compatible serial data interface. This write-only interface has three inputs: chip-select (\overline{CS}), data clock (SCLK), and data input (DIN). Drive \overline{CS} low to enable the serial interface and clock data synchronously into the shift register on each SCLK rising edge. The WRITE commands (C1, C0 = 00 or 01) require 16 clock cycles to clock in the command, address, and data. The COPY commands (C1, C0 = 10 or 11) can use either eight clock cycles to transfer only command and address bits or 16 clock cycles, with the device disregarding 8 data bits. After loading data into the shift register, drive \overline{CS} high to latch the data into the appropriate potentiometer control register and disable the serial interface. Keep \overline{CS} low during the entire serial data stream to avoid corruption of the data.

Register Map

| CLOCK EDGE | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|----|----|---|---|----|----|----|----|----|----|----|----|----|----|
| | – | – | C1 | C0 | – | – | A1 | A0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write Wiper Register A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write Wiper Register B | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write Wiper Register A and B | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write NV Register A | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write NV Register B | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Write NV Register A and B | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Copy Wiper Register A to NV Register A | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | – | – | – | – | – | – | – | – |
| Copy Wiper Register B to NV Register B | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | – | – | – | – | – | – | – | – |
| Copy Both Wiper Registers to NV Registers | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | – | – | – | – | – | – | – | – |
| Copy NV Register A to Wiper Register A | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | – | – | – | – | – | – | – | – |
| Copy NV Register B to Wiper Register A | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | – | – | – | – | – | – | – | – |
| Copy Both NV Registers to Wiper Registers | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | – | – | – | – | – | – | – | – |

Digital Interface Format

The data format consists of three elements: command bits, address bits, and data bits. The command bits (C1 and C0) indicate the action to be taken such as changing or storing the wiper position. The address bits (A1 and A0) specify which potentiometer the command affects and the 8 data bits (D7 to D0) specify the wiper position.

Write-Wiper Register (Command 00)

Data written to the write-wiper registers (C1, C0 = 00) controls the wiper positions. The 8 data bits (D7 to D0) indicate the position of the wiper. If DIN = 0x00h, the wiper moves to the position closest to the L terminal. If DIN=0xFFh, the wiper moves to the position closest to the H terminal. This command writes data to the volatile RAM, leaving the NV registers unchanged. When the device powers up, the data stored in the NV registers transfers to the volatile wiper register, moving the wiper to the stored position

Write-NV Register (Command 01)

This command (C1, C0 = 01) stores the position of the wipers to the NV registers for use at power-up. Alternatively, the “copy wiper register to NV register” command can be used to store the position of the wipers to the NV registers. Writing to the NV registers does not affect the position of the wipers.

Copy Wiper Register to NV Register (Command 10)

This command (C1, C0 = 10) stores the current position of the wiper to the NV register, for use at power-up. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0. Alternatively, the “write NV register” command can be used to store the current position of the wiper to the NV register.

Copy NV Register to Wiper Register (Command 11)

This command (C1, C0 = 11) restores the wiper position to the previously stored position in the NV register. This command may affect one potentiometer at a time, or both simultaneously, depending on the state of A1 and A0.

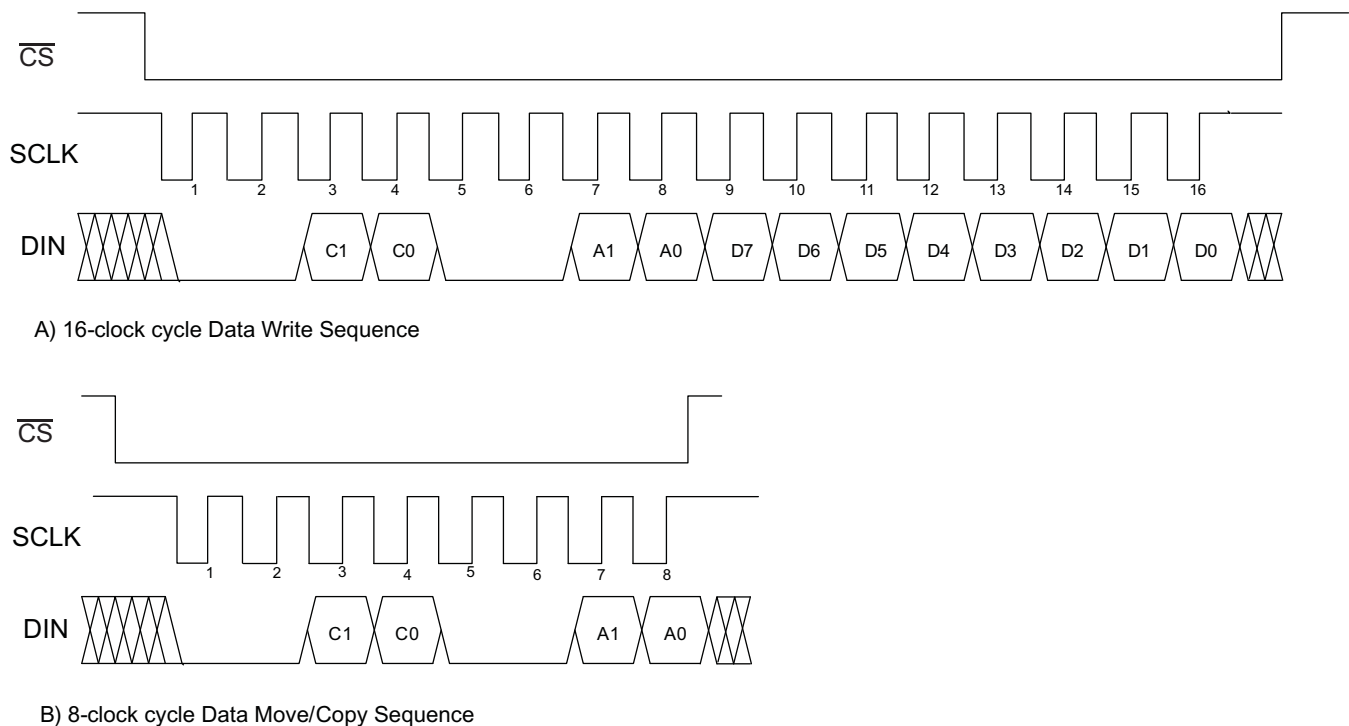


Figure 2. Digital Interface Write Sequence

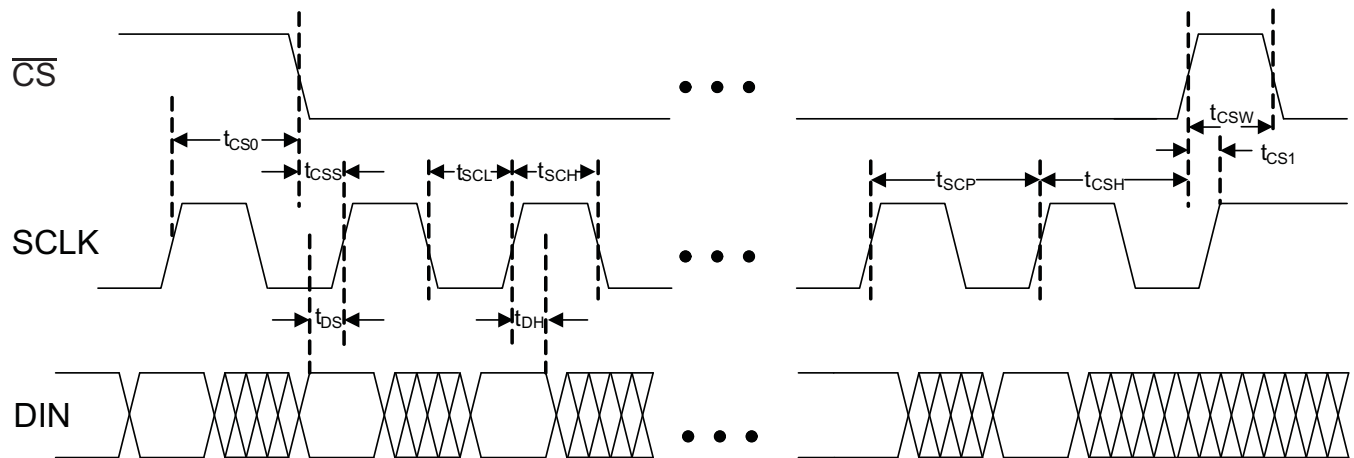


Figure 3. Digital Interface Timing Diagram

APPLICATION EXAMPLE

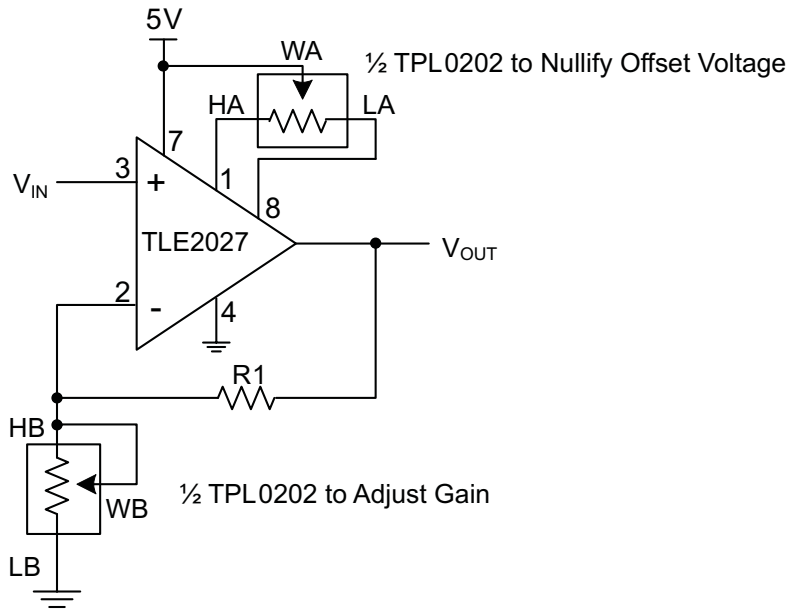


Figure 4. Offset Voltage and Gain Adjustment

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|----------------------------------|
| TPL0202-10MRTER | ACTIVE | WQFN | RTE | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | Purchase Samples |
| TPL0202-10RUCR | PREVIEW | QFN | RUC | 14 | 3000 | TBD | Call TI | Call TI | Samples Not Available |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPL0202-10MRTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.0 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



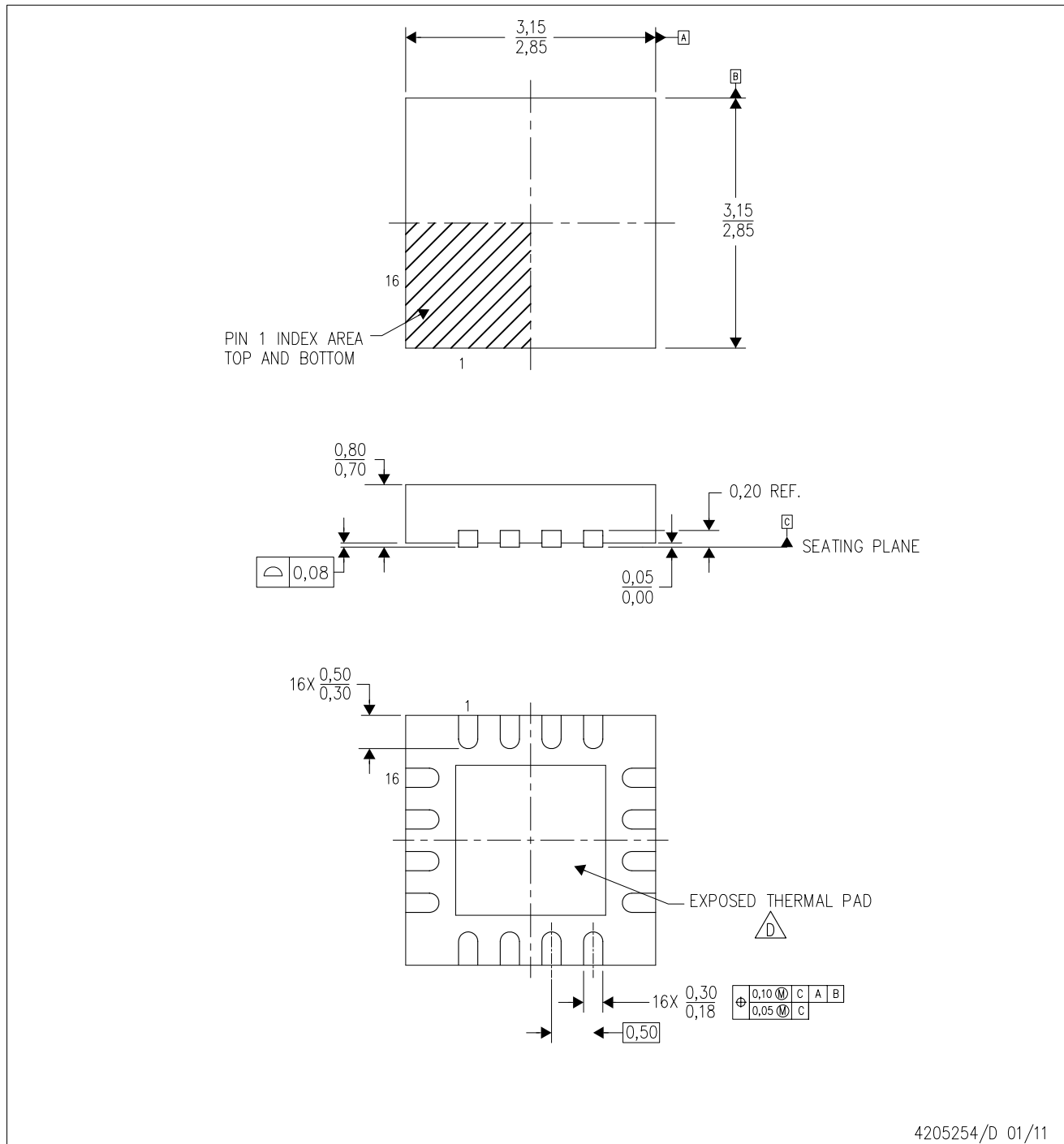
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPL0202-10MRTER | WQFN | RTE | 16 | 3000 | 370.0 | 355.0 | 55.0 |


MECHANICAL DATA

RTE (S-PWQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4205254/D 01/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RTE (S-PWQFN-N16)

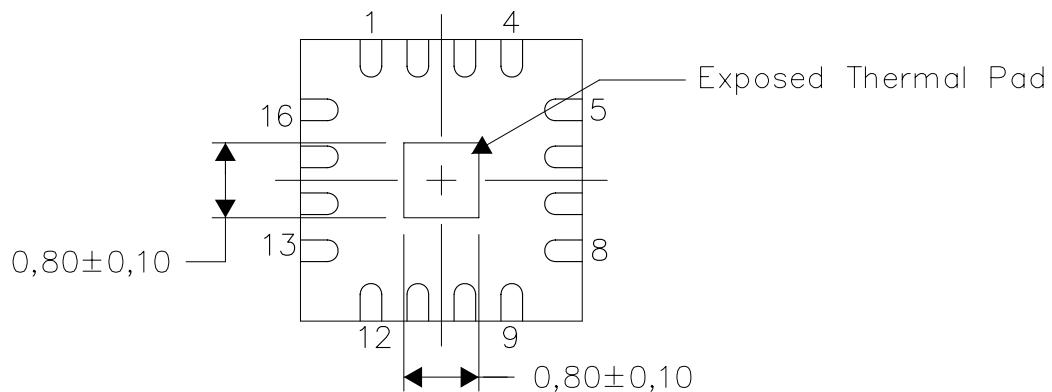
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

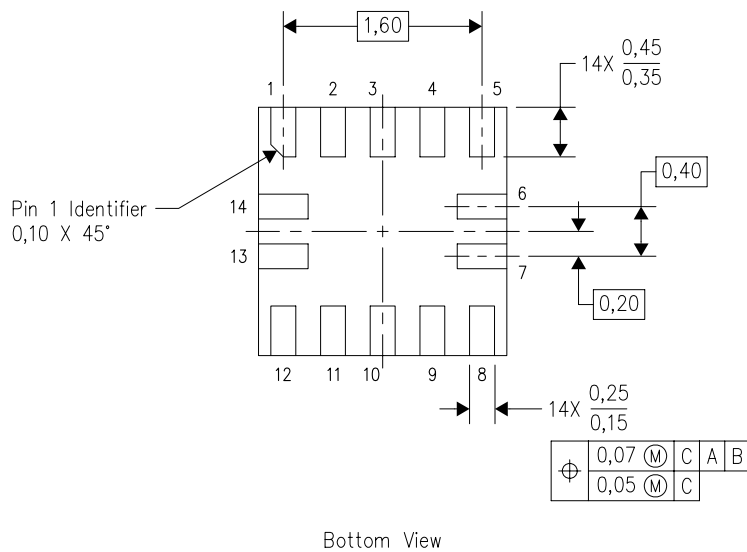
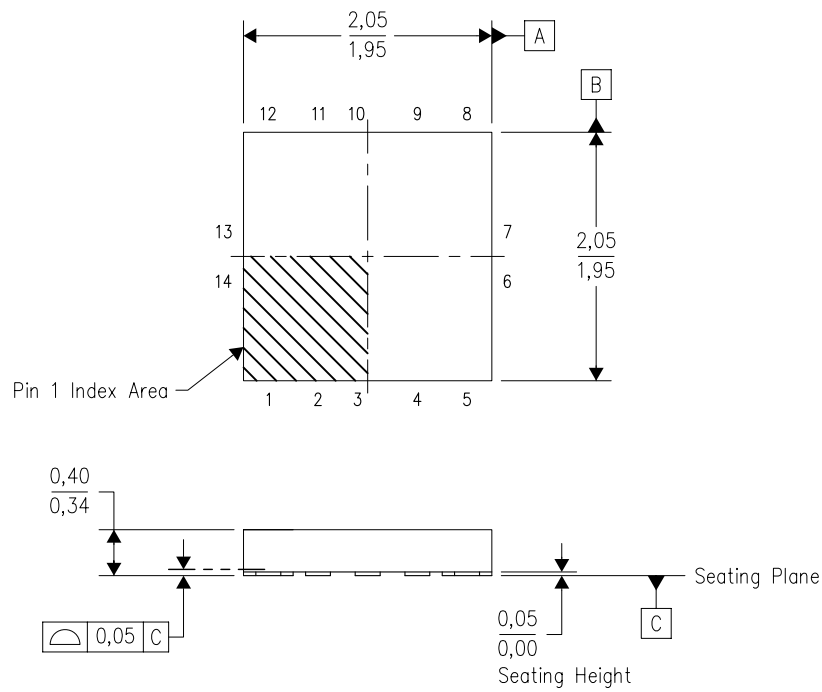
Exposed Thermal Pad Dimensions

4206446-6/1 01/11

NOTE: A. All linear dimensions are in millimeters

RUC (S-PX2QFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4208447/C 08/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2GFE.

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