

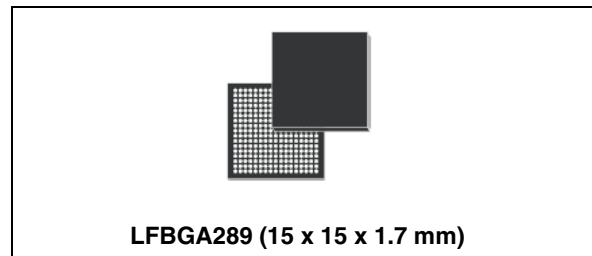


# SPEAr300

Embedded MPU with ARM926 core, flexible memory support, powerful connectivity features and human machine interface

## Features

- ARM926EJ-S core up to 333 MHz
- High-performance 8-channel DMA
- Dynamic power-saving features
- Configurable peripheral functions on 102 shared I/Os (please refer to [Table 11: PL\\_GPIO multiplexing scheme](#))
- Memory
  - 32 KB ROM and 56 KB internal SRAM
  - LPDDR-333/DDR2-666 external memory interface (up to 1 GB addressable memory)
  - SDIO/MMC card interface
  - Serial Flash memory interface (SMI)
  - Flexible static memory controller (FSMC) up to 16-bit data bus width, supporting external SRAM, NAND/NOR Flash and FPGAs
  - Serial SPI Flash interface
- Connectivity
  - 2 x USB 2.0 Host
  - USB 2.0 Device
  - Fast Ethernet (MII port)
  - 1x SSP Synchronous serial peripheral (SPI, Microwire or TI protocol)
  - 1x I<sup>2</sup>C
  - 1x I<sup>2</sup>S,
  - 1x fast IrDA interface
  - 1x UART interface
  - TDM bus (512 timeslots)
  - Up to 8 additional I<sup>2</sup>C/SPI chip selects
- Security
  - C3 cryptographic accelerator
- Peripherals supported
  - Camera interface (ITU-601/656 and CSI2 support)
  - TFT/STN LCD controller (resolution up to 1024 x 768 and up to 24 bpp)



- Touchscreen support (using the ADC)
- 9 x 9 keyboard controller
- Glueless management of up to 8 SLICs/CODECs
- Miscellaneous functions
  - Integrated real time clock, watchdog, and system controller
  - 8-channel 10-bit ADC, 1 Msp/s
  - 1-bit DAC
  - JPEG codec accelerator
  - Six 16-bit general purpose timers with capture mode and programmable prescaler
  - Up to 62 GPIOs

## Applications

- SPEAr300 embedded MPU is configurable in 13 sets of peripheral functions targeting a range of applications:
  - General purpose NAND Flash or NOR Flash based devices
  - Digital photo frames
  - WiFi or IP phones (low end or high end)
  - ATA PABX systems (with or without I<sup>2</sup>S)
  - 8-bit or 14-bit camera (with or without LCD)

**Table 1. Device summary**

| Order code | Temp range, °C | Package                          | Packing |
|------------|----------------|----------------------------------|---------|
| SPEAR300-2 | - 40 to 85 °C  | LFBGA289 (15x15 mm) pitch 0.8 mm | Tray    |

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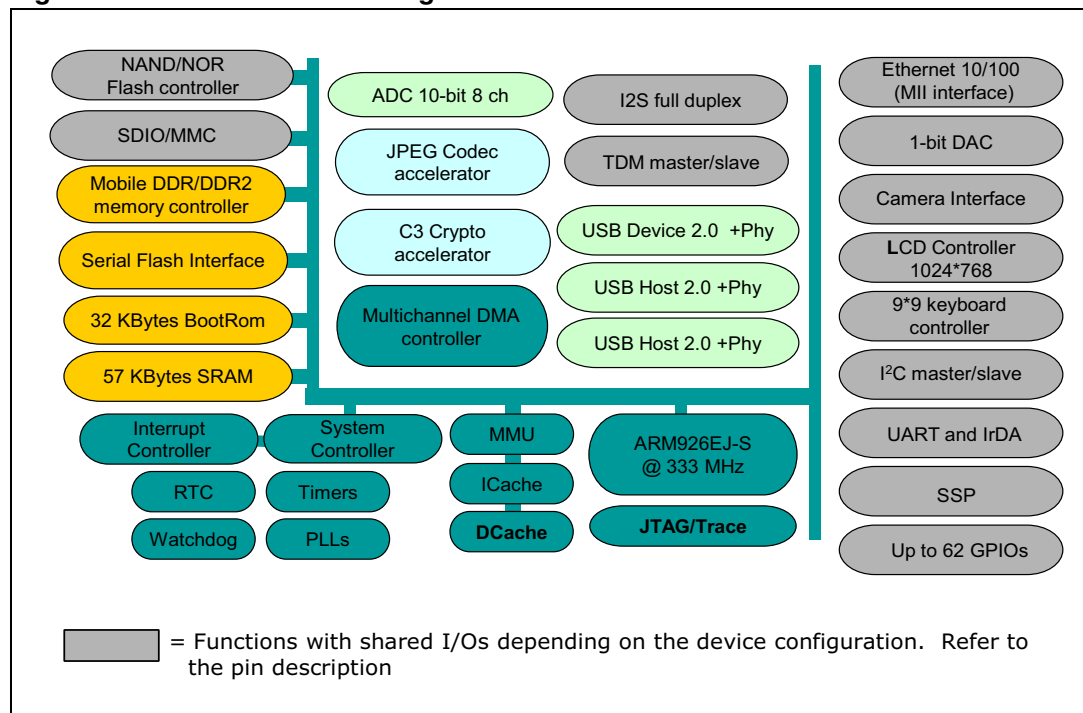
# 1 Description

The SPEAr300 is a member of the SPEAr family of embedded MPUs for networked devices. It is based on the powerful ARM926EJ-S processor (up to 333 MHz), widely used in applications where high computation performance is required.

In addition, SPEAr300 has an MMU that allows virtual memory management -- making the system compliant with advanced operating systems like Linux. It also offers 16 KB of data cache, 16 KB of instruction cache, JTAG and ETM (embedded trace macro-cell) for debug operations.

A full set of peripherals allows the system to be used in many applications, some typical applications being HMI, Security and VoIP phones.

**Figure 1. Functional block diagram**





## 1.1 Main features:

- ARM926EJ-S 32-bit RISC CPU, up to 333 MHz
  - 16 Kbytes of instruction cache, 16 Kbytes of data cache
  - 3 instruction sets: 32-bit for high performance, 16-bit (Thumb) for efficient code density, bytecode Java mode (Jazelle™) for direct execution of Java code.
  - AMBA bus interface
- 32-KByte on-chip BootROM
- 8-KByte on-chip SRAM
- 16-bit mobile DDR/DDR2 memory controller (up to 333 MHz)
- Serial memory interface
- SDIO/MMC interface supporting SPI, SD1, SD4 and SD8 mode with card detect, write protect, LED
- 8/16-bits NOR Flash/NAND Flash controller
- Boot capability from NAND Flash, serial/parallel NOR Flash, Ethernet and UART
- Boot and field upgrade capability from USB
- Multichannel DMA controller
- Color LCD Controller for STN/TFT display panels
  - up to 1024 x 768 resolution
  - 24 bpp true color
- Up to 62 GPIOs (muxed with peripheral I/Os), up to 22 with interrupt capability
- JPEG CODEC accelerator, 1 clock/pixel
- Camera interface ITU-601 with external or embedded synchronization (ITU-656 or CSI2). Picture limit is given by the line length that must be stored in a 2048 x 32 buffer
- C3 Crypto accelerator (DES/3DES/AES/SHA1)
- TDM master/slave
  - Up to 512 timeslots
  - Any input timeslot can be switched to any output timeslot, and/or can be buffered for computation
  - Up to 16 channels of 1 to 4 timeslots buffered during 32 ms
  - Up to 16 buffers can be played in output timeslots
- I<sup>2</sup>S interface, full duplex with data buffer for left and right channels allowing up to 64 ms of voice buffer (for 32 bit samples).
- 10-bit ADC, 1 Msps, 8 inputs/1-bit DAC
- 9 x 9 keyboard controller
- Ethernet MAC 10/100 Mbps (MII PHY interface)
- Two USB2.0 host (high-full-low speed) with integrated PHY transceiver
- One USB2.0 device (high-full-low speed) with integrated PHY transceiver
- SSP master/slave (Motorola SPI, Texas instruments, National semiconductor protocols) up to 50 Mbps
- I<sup>2</sup>C (slow- fast-high speed, up to 1.2 Mb/s) master/slave
- I/O peripherals
  - UART (speed rate up to 3 Mbps)
  - IrDA (FIR/MIR/SIR) 9.6 kbps to 4 Mbps speed-rate

- Advanced power saving features
  - Normal, Slow, Doze and Sleep modes
  - CPU clock with software-programmable frequency
  - Enhanced dynamic power-domain management
  - Clock gating functionality
  - Low frequency operating mode
  - Automatic power saving controlled from application activity demands
- Vectored interrupt controller
- System and peripheral controller
  - 3 pairs of 16-bit general purpose timers with programmable prescaler.
  - RTC with separate power supply allowing battery connection
  - Watchdog timer
  - Miscellaneous registers array for embedded MPU configuration
- Programmable PLL for CPU and system clocks
- JTAG IEEE 1149.1
- Boundary scan
- ETM functionality multiplexed on primary pins
- Supply voltages
  - 1.2 V core, 1.8 V/2.5 V DDR, 2.5 V PLLs, 1.5 V RTC and 3.3 V I/Os
- Operating temperature: - 40 to 85 °C
- LFBGA289 (15 x15 mm, pitch 0.8 mm)

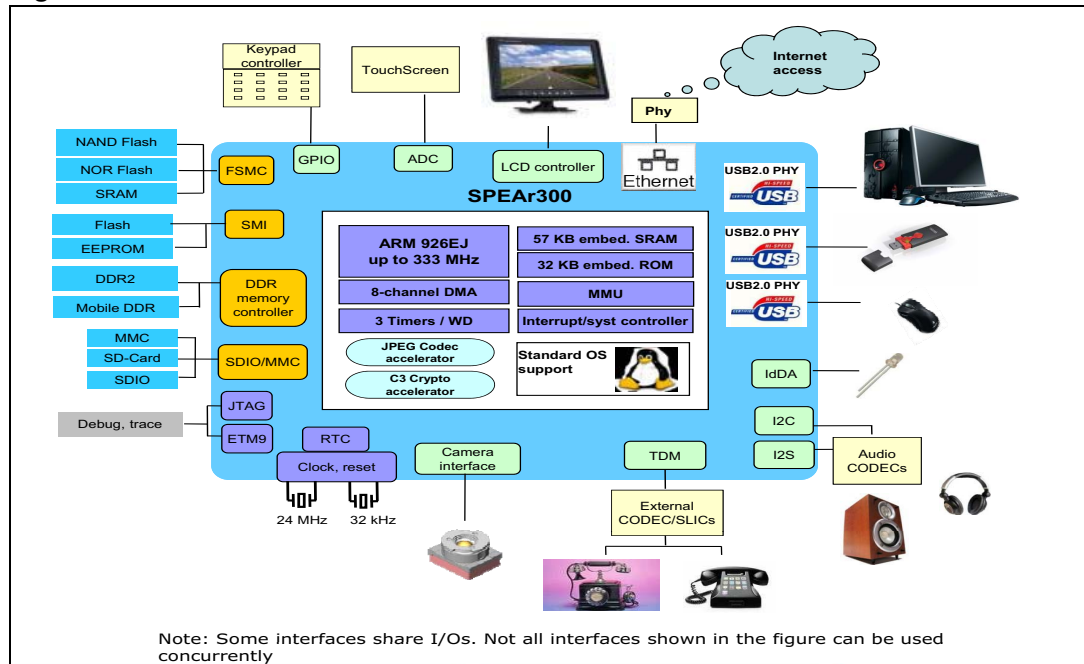
## 2 Architecture overview

The SPEAr300 internal architecture is based on several shared subsystem logic blocks interconnected through a multilayer interconnection matrix.

The switch matrix structure allows different subsystem dataflow to be executed in parallel improving the core platform efficiency.

High performance master agents are directly interconnected with the memory controller reducing the memory access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal efficient weighted round-robin arbitration mechanism.

Figure 2. SPEAr300 overview



### 2.1 ARM926EJ-S CPU

The core of the SPEAr300 is an ARM926EJ-S reduced instruction set computer (RISC) processor.

It supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density and includes features for efficient execution of Java byte codes.

The ARM CPU and is clocked at a frequency up to 333 MHz. It has a 16-Kbyte instruction cache, a 16-Kbyte data cache, and features a memory management unit (MMU) which makes it fully compliant with Linux and WindowsCE operating systems.

It also includes an embedded trace module (ETM Medium+) for real-time CPU activity tracing and debugging. It supports 4-bit and 8-bit normal trace mode and 4-bit demultiplexed trace mode, with normal or half-rate clock.

## 2.2 System controller

The System Controller provides an interface for controlling the operation of the overall system.

### Main features:

- Power saving system mode control
- Crystal oscillator and PLL control
- Configuration of system response to interrupts
- Reset status capture and soft reset generation
- Watchdog and timer module clock enable
- Remap control
- General purpose peripheral control r
- System and peripheral clock control and status

### 2.2.1 Clock and reset system

The clock system is a fully programmable block that generates all the clocks for the SPEAr300.

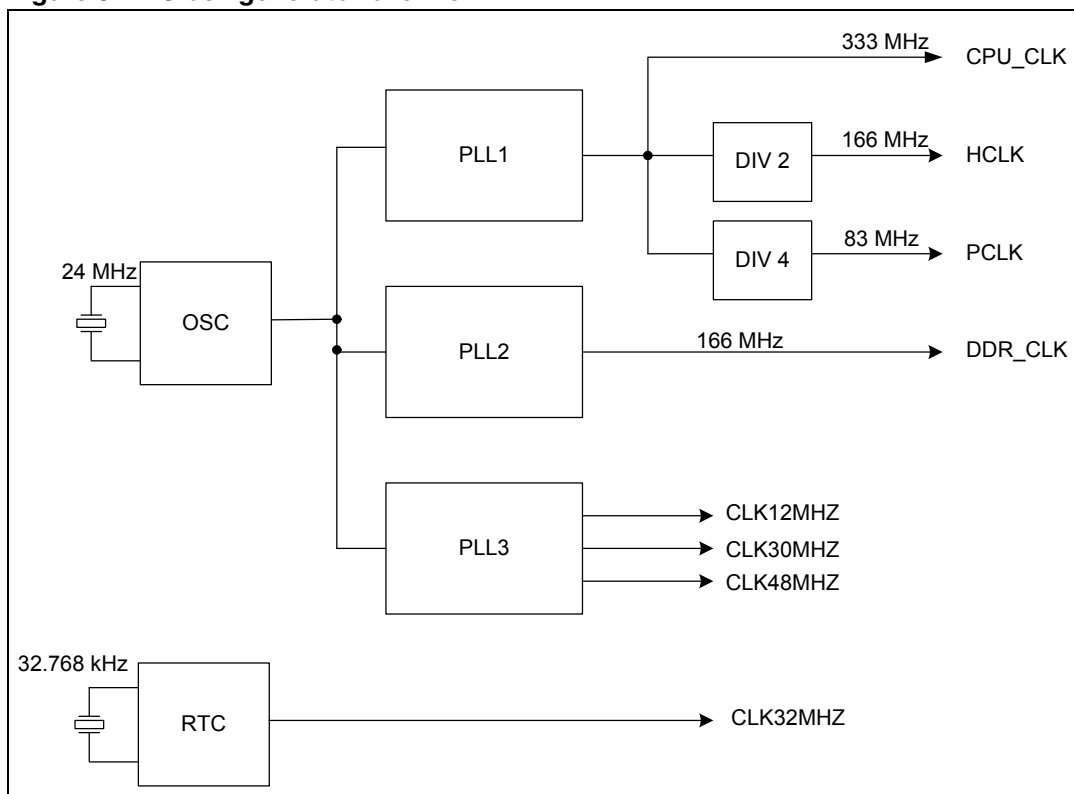
The default operating clock frequencies are:

- CPU\_CLK @ 333 MHz for the CPU.
- HCLK @ 166 MHz for AHB bus and AHB peripherals.
- PCLK @ 83 MHz for, APB bus and APB peripherals.
- DDR\_CLK @ 100-333 MHz for DDR memory interface.

The above frequencies are the maximum allowed values. The clock frequencies can be modified by programming the clock system registers.

The clock system consists of 2 main parts: a multi clock generator block and two internal PLLs.

Figure 3. Clock generator overview



The multi clock generator block, takes a reference signal (which is usually delivered by the PLL), generates all clocks for the IPs of SPEAr300 according to dedicated programmable registers.

Each PLL uses an oscillator input of 24 MHz to generate a clock signal at a frequency corresponding to the highest of the group. This is the reference signal used by the multi clock generator block to obtain all the other required clocks for the group. Its main feature is electromagnetic interference reduction capability.

The user can set up the PLL in order to modulate the VCO with a triangular wave. The resulting signal has a spectrum (and power) spread over a small programmable range of frequencies centered on F0 (the VCO frequency), obtaining minimum electromagnetic emissions. This method replaces all the other traditional methods of EMI reduction, such as filtering, ferrite beads, chokes, adding power layers and ground planes to PCBs, metal shielding and so on. This gives the customer appreciable cost savings.

In sleep mode the SPEAr300 runs with the PLL disabled so the available frequency is 24 MHz or a sub-multiple (1/2, 1/4, 1/8).

### 2.2.2 Power saving system mode control

Using three mode control bits, the system controller switch the SPEAr300 to any one of four different modes: DOZE, SLEEP, SLOW and NORMAL.

- **SLEEP mode:** In this mode the system clocks, HCLK and CPU\_CLK, are disabled and the System Controller clock is driven by a low speed oscillator (nominally 32768 Hz). When either a FIQ or an IRQ interrupt is generated (through the VIC) the system enters

DOZE mode. Additionally, the operating mode setting in the system control register automatically changes from SLEEP to DOZE.

- **DOZE mode:** In this mode the system clocks, HCLK and CPU\_CLK, and the System Controller clock are driven by a low speed oscillator. The System Controller moves into SLEEP mode from DOZE mode only when none of the mode control bits are set and the processor is in Wait-for-interrupt state. If SLOW mode or NORMAL mode is required the system moves into the XTAL control transition state to initialize the crystal oscillator.
- **SLOW mode:** During this mode, both the system clocks and the System Controller clock are driven by the crystal oscillator. If NORMAL mode is selected, the system goes into the "PLL control" transition state. If neither the SLOW nor the NORMAL mode control bits are set, the system goes into the "Switch from XTAL" transition state.
- **NORMAL mode:** In NORMAL mode, both the system clocks and the System Controller clock are driven by the PLL output. If the NORMAL mode control bit is not set, then the system goes into the "Switch from PLL" transition state.

## 2.3 Vectored interrupt controller (VIC)

The VIC allows the OS interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. There are 32 interrupt lines and the VIC uses a separate bit position for each interrupt source. Software controls each request line to generate software interrupts.

## 2.4 General purpose timers

SPEAr300 provides three general purpose timers (GPTs) acting as APB slaves.

Each GPT consists of 2 channels, each one made up of a programmable 16-bit counter and a dedicated 8-bit timer clock prescaler. The programmable 8-bit prescaler performs a clock division by 1 up to 256, and different input frequencies can be chosen through SPEAr300 configuration registers (frequencies ranging from 3.96 Hz to 48 MHz can be synthesized).

Two different modes of operation are available:

- Auto-reload mode, an interrupt source is activated, the counter is automatically cleared and then it restarts incrementing.
- Single-shot mode, an interrupt source is activated, the counter is stopped and the GPT is disabled.

## 2.5 Watchdog timer

The watchdog timer consists of a 32-bit down counter with a programmable timeout interval that has the capability to generate an interrupt and a reset signal on timing out. The watchdog module is intended to be used to apply a reset to a system in the event of a software failure.

## 2.6 RTC oscillator

The RTC provides a 1-second resolution clock. This keeps time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

## 2.7 Multichannel DMA controller

Within its basic subsystem, SPEAr300 provides an DMA controller (DMAC) able to service up to 8 independent DMA channels for sequential data transfers between single source and destination (i.e., memory-to-memory, memory-to-peripheral, peripheral to- memory, and peripheral-to-peripheral).

Each DMA channel can support a unidirectional transfer, with internal four-word FIFO per channel.

## 2.8 Embedded memory units

- 32 Kbytes of BootROM
- Up to 57 Kbytes of SRAM

The size of available SRAM varies according to the peripheral configuration mode See [Table 10.](#):

- 57 Kbytes in modes 1 and 2
- 8 Kbytes in modes 3 to 13.

## 2.9 Mobile DDR/DDR2 memory controller

SPEAr300 integrates a high performances multi-channel memory controller able to support low power Mobile DDR and DDR2 double data rate memory devices. The multi-port architecture ensures memory is shared efficiently among different high-bandwidth client modules.

It has 6 internal ports. One of them is reserved for register access during the controller initialization while the other five are used to access the external memory.

It also include the physical layer (PHY) and some DLLs that allow fine tuning of all the timing parameters to maximize the data valid windows at any frequency in the allowed range.

## 2.10 Serial memory interface

SPEAr300 provides a serial memory interface (SMI) to SPI-compatible off-chip memories. These serial memories can be used for both data storage and code execution.

**Main features:**

- Supports the following SPI-compatible Flash and EEPROM devices:
  - STMicroelectronics M25Pxxx, M45Pxxx
  - STMicroelectronics M95xxx, except M95040, M95020 and M95010
  - ATMEL AT25Fxx
  - YMC Y25Fxx
  - SST SST25LFxx
- Acts always as a SPI master and up to 2 SPI slave memory devices are supported (through as many chip select signals), with up to 16 MB address space each
- SMI clock signal (SMICK) is generated by SMI (and input to all slaves)
- SMICK can be up to 50 MHz in fast read mode (or 20 MHz in normal mode). It can be controlled by 7 programmable bits.



## 2.11 Flexible static memory controller (FSMC)

SPEAr300 provides a Flexible Static Memory Controller (FSMC) which interfaces the AHB bus to external NAND/NOR Flash memories and to asynchronous SRAM memories.

### Main features:

- Provides an interface between AHB system bus and external parallel memory devices
- Interfaces static memory-mapped devices including RAM, ROM and synchronous burst Flash.
- For SRAM and Flash 8/16-bit wide, external memory and data paths are provided
- FSMC performs only one access at a time and only one external device is accessed.
- Supports little-endian and big-endian memory architectures
- AHB burst transfer handling to reduce access time to external devices
- Supplies an independent configuration for each memory bank
- Programmable timings to support a wide range of devices
  - Programmable wait states (up to 31)
  - Programmable bus turnaround cycles (up to 15)
  - Programmable output enable and write enable delays (up to 15)
- Provides independent chip select control for each memory bank
- Shares the address bus and the data bus with all the external peripherals. Only the chip selects are unique for each peripheral
- External asynchronous wait control

## 2.12 UART

### Main features:

- Hardware/software flow control
- Modem control signals
- Separate 16 x 8 (16 locations deep x 8-bit wide) transmit and 16 x 12 receive FIFOs to reduce CPU interrupts
- Speed up to 3 Mbps.

## 2.13 Fast IrDA controller (FIrDA)

The fast IrDA controller is a programmable infrared controller that acts as an interface to an off-chip infrared transceiver. This controller is able to perform the modulation and the demodulation of the infrared signals and the wrapping of the IrDA link access protocol (IrLAP) frames.

**Main features:**

- Supports IrDA serial infrared physical layer specification (IrPHY), version 1.3
- Supports IrDA link access protocol (IrLAP), version 1.1
- Serial infrared (SIR), with rates 9.6 Kbps, 19.2 Kbps, 38.4 Kbps, 57.6 Kbps and 115.2 Kbps
- Medium infrared (MIR), with rates 576 Kbps and 1.152 Mbps
- Fast infrared (FIR), with rate 4 Mbps.
- Transceiver interface compliant with all IrDA transceivers with configurable TX and RX signal polarity.
- Half-duplex infrared frame transmission and reception.
- 16-bit CRC algorithm for SIR and MIR, and 32-bit CRC algorithm for FIR.

## 2.14 Synchronous serial port (SSP)

SPEAr300 provides one synchronous serial port (SSP) block that offers a master or slave interface for synchronous serial communication with slave or master peripherals

**Main features:**

- Maximum speed of 41.5 Mbps
- Master and slave mode capability
- Programmable clock bit rate and prescale
- Separate transmit and receive first-in, first-out memory buffers, 16 bits wide, 8 locations deep
- Programmable choice of interface operation:
  - SPI (Motorola)
  - Microwire (National Semiconductor)
  - TI synchronous serial
- Programmable data frame size from 4 to 16-bit.
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts
- DMA interface

## 2.15 I2C

The I2C controller, acts as an APB slave interface to the two-wire serial I2C bus.

**Main features:**

- Compliance to the I2C-bus specification (Philips)
- I<sup>2</sup>C v2.0 compatible.
- Operates in three different speed modes:
  - Standard (100 kbps)
  - Fast (400 kbps)
  - High-speed (3.4 Mbps)
- Master and slave mode configuration possible
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Slave bulk data transfer capability.
- Connection with general purpose DMA is provided to reduce the CPU load.
- Interrupt or polled-mode operation

## 2.16 SPI\_I2C multiple slave control

The SPI interface has only one slave select signal, SS0.

The I<sup>2</sup>C interface does not allow control of several devices with the same address, which is frequently required for CODECs.

The SPI\_I2C extension allows management of up to 8 SPI devices, or 8 I<sup>2</sup>C devices at the same address (total SPI+I<sup>2</sup>C devices=8).

The SPI extension is made by generating three more slave select signals SS1, SS2 and SS3.

The I<sup>2</sup>C extension is done by replicating the I2C\_SCL signal if the corresponding pin is set active. Otherwise the pin remains low, so that the start condition is not met.

Each of the 8 pins can reproduce either the SPI SS0 signal, or the I2C\_SCL signal. The selection is made through a register.

## 2.17 TDM interface

The TDM block implements time division multiplexing.

### Main features:

- TDM interface with 512 timeslots and up to 16 bufferization channels.
- 32 ms bufferization for 16 channels (of 4 bytes each)
- Supports master and slave mode operation
- Programmable clock and synchronization signal generation in master mode
- Clock & synchronization signal recovery in slave mode
- 8 programmable synchronization signals for CODECs
- Uses 11 pins:
  - SYNC7-0 are dedicated frame syncs for CODECs without timeslot recognition
  - CLK is the TDM clock
  - DIN is the TDM input and receives the data
  - DOUT is the TDM output and transmits the data. It can be high impedance on a unused timeslot
- The TDM interface can be the master or a slave of the CLK or SYNC0 signals.
- Timeslots can be used for switching or bufferization purposes:
  - Switching and bufferization can be used concurrently for different timeslots on the same TDM
  - The only limitation is that an output timeslot can not be switched and bufferized at the same time.
  - Timeslot switching: any of the output time slots can receive any input timeslot of the previous frame. The connection memory is part of the action memory, indicating which timeslot has to be output.
  - Timeslot bufferization: data from DIN is stored in an input buffer and data from an output buffer is played on DOUT. When the number of samples stored/played reaches the buffer size, the processor is interrupted in order to read the input buffer and prepare a new output buffer (or a DMA request is generated).

## 2.18 I<sup>2</sup>S interface

The I<sup>2</sup>S interface is very similar to the TDM block, but the frame sync is limited to Philips I<sup>2</sup>S definition. It is composed of 4 signals:

- I2S\_LRCK; Left and right channels synchronization (Master/slave)
- I2S\_CLK: I<sup>2</sup>S clock (Master/slave)
- I2S\_DIN: I<sup>2</sup>S clock (Master/slave)
- I2S DOUT: I<sup>2</sup>S output (tri-state)

The DOUT line can be high impedance when out of samples. Data is always stored in 32 bit format in the buffer. A shift left operation is possible to left align the data.

### Main features:

- Can be master or slave for the clock and sync signals
- Buffering of up to 1024 samples (512 left and 512 right samples representing 64 ms of voice). Data is stored always on 32 bits.
- Left and right channels are stored in two different buffers.
- Two banks are used to exchange data with the processor.
- In master mode, LRCK can be adjusted for 8, 16 or 32 bits width.
- Data width can be less than LRCK width. Input (received on I2S\_DIN) and output (transmitted on DOUT) can be 8, 16 or 32 bits.

## 2.19 GPIOs

The General Purpose Input/Outputs (GPIOs) provide programmable inputs or outputs.

### Main features:

- Individually programmable input/output pins implemented in 3 blocks:
  - Up to 6 base GPIOs in the basic subsystem (basGPIO)
  - Up to 18 GPIOs in the RAS subsystem (G10 and G8)
  - Up to 18 GPIOs in the keyboard controller
  - Up to 8 GPIOs in the independent GPIO block (GPIO[7:0])
- Programmable interrupt generation capability up to 22 pins.
- Base GPIOs and independent GPIOs support bit masking in both read and write operation through address lines.

Up to 62 general purpose I/Os are available in Mode 4 (LEND\_IP\_ph) (see [Table 10](#)).

- In this mode the application can use:
  - 10 GPIOs in G10 block
  - 8 GPIOs in G8 block (0 to 3 in output mode only)
  - 18 GPIO (keyboard controller I/Os in GPIO mode)
  - 6 base GPIOs (basGPIO) (enabled as alternate functions (see [Table 11](#)))
  - 8 IT pins (input only, with interrupt capability)
  - 4 SYNC outputs (SYNC4-7)
  - 8 SPI\_I2C outputs

## 2.20 Keyboard controller

SPEAr300 provides a GPIO/keyboard controller block which is a two-mode input and output port.

### Main features:

- The selection between the two modes is an APB Bus programmable bit.
- Keyboard interface uses 18 pins
- 18-bit general-purpose parallel port with input or output single pin programmability
- Pins can be used as general purpose I/O or to drive a 9 x 9 keyboard (81 keys)
- Keyboard scan period can be adjusted between 10 ms and 80 ms
- Supports auto-scanning with debouncing.

## 2.21 CLCD controller

SPEAr300 has a color liquid crystal display controller (CLCDC) that provides all the necessary control signals to interface directly to a variety of color and monochrome LCD panels.

### Main features:

- Resolution programmable up to 1024 x 768
- 16-bpp true-color non-palletized, for color STN and TFT
- 24-bpp true-color non-palletized, for color TFT
- Supports single and dual panel mono super twisted nematic (STN) displays with 4 or 8-bit interfaces
- Supports single and dual-panel color and monochrome STN displays
- Supports thin film transistor (TFT) color displays
- 15 gray-level mono, 3375 color STN, and 32 K color TFT support
- 1, 2, or 4 bits per pixel (bpp) palletized displays for mono STN
- 1, 2, 4 or 8-bpp palletized color displays for color STN and TFT
- Programmable timing for different display panels
- 256 entry, 16-bit palette RAM, arranged as a 128 x 32-bit RAM physically frame, line and pixel clock signals
- AC bias signal for STN and data enable signal for TFT panels patented gray scale algorithm
- Supports little and big-endian

## 2.22 Camera interface

The camera interface receives data from a sensor in parallel mode (8 to 14-bits) by storing a full line in a buffer memory, then requesting a DMA transfer or interrupting the processor.

When all the lines of a frame are transferred, a frame sync interrupt is generated.

### Main features:

- Supports both hardware synchronization (HSYNC and VSYNC signals) and embedded synchronization (ITU656 or CSI2).
- Data carried by the bus can be:
  - Raw Bayer10 (10-14 bits/pixel – 2 Bytes), Raw Bayer8 (8 bits/pixel – 1 Byte),
  - YCbCr400 (1 Byte/pixel – 1 Byte), YCbCr422 (4 Bytes/ 2 pixels – 2\*2 Bytes), YCbCr444 (3 Bytes/ pixel – 4 Bytes)
  - RGB444 (2 Bytes/ pixel – 2 Bytes), RGB565 (2 Bytes/ pixel – 2 Bytes), RGB888 (3 Bytes/ pixel – 4 Bytes)
  - JPEG compressed
- Data is stored in a 2048 x 32 buffer memory
- The camera interface can be assigned to two different set of pins. When using data greater than 8-bits, it is not possible to use the MII interface.
- Max pixel clock frequency is 100 MHz

## 2.23 SDIO controller/MMC card interface

The SDIO host controller has an AMBA compatible interface and conforms to the SD host controller standard specification version 2.0. It handles SD/SDIO protocol at transmission level, packing data, adding cyclic redundancy check (CRC), start/end bit, and checking for transaction format correctness.

### Main features:

- Meets the following standard specifications:
  - SD host controller standard specification version 2.0
  - SDIO card specification version 2.0
  - SD memory card specification draft version 2.0
  - SD memory card security specification version 1.01
  - MMC specification version 3.31 and 4.2
- Supports both DMA and non-DMA mode of operation
- Supports MMC plus and MMC mobile
- Card detection (insertion/removal)
- Password protection of cards
- Host clock rate variable between 0 and 48 MHz
- Supports 1-bit, 4-bit and 8-bit SD modes and SPI mode
- Supports Multi Media Card interrupt mode
- Allows card to interrupt host in 1-bit, 4-bit, 8-bit SD modes and SPI mode.
- Up to 100 Mbit/s data rate using 4 parallel data lines (sd4-bit mode)
- Up to 416 Mbit/s data rate using 8-bit parallel data lines (sd8-bit mode)
- Cyclic redundancy check CRC7 for command and CRC16 for data integrity
- Designed to work with I/O cards, read-only cards and read/write cards
- Error correction code (ECC) support for MMC4.2 cards
- Supports read wait control, suspend/resume operation
- Supports FIFO overrun and underrun condition by stopping the SD clock
- Conforms to AMBA specification AHB (2.0)



## 2.24 Ethernet controller

SPEAr300 provides an Ethernet MAC 10/100 Universal (commonly referred to as GMAC-UNIV), enabling to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2002 standard.

*Note: GMAC is a hardware block implementing Ethernet MAC layer 2 processing. GMAC is configured for 10/100 Mbps operation on SPEAr3xx family and up to 1 Gbps on SPEAr600.*

### Main features:

- Compliant with the IEEE 802.3-2002 standard
- Supports the default MII interface to the external PHY
- Supports 10/100 Mbps data transfer rates
- Local FIFO available (4 Kbyte RX, 2 Kbyte TX)
- Supports both half-duplex and full-duplex operation. In half-duplex operation, CSMA/CD protocol is provided for, as well as packet bursting and frame extension at 100 Mbps
- Programmable frame length to support both standard and jumbo Ethernet frames with size up to 16 Kbyte
- A variety of flexible addresses filtering modes are supported
- A set of control and status registers (CSRs) to control MAC core operation
- Native DMA with single-channel transmit and receive engines
- DMA implements dual-buffer (ring) or linked-list (chained) descriptor chaining
- An AHB slave acting as programming interface to access all CSRs, for both DMA and MAC core subsystems
- An AHB master for data transfer to system memory
- 32-bit AHB master bus width, supporting 32, 64, and 128-bit wide data transactions
- It supports both little and big endian memory architectures

## 2.25 USB2 host controller

SPEAr300 has a fully independent USB 2.0 host controller, consisting of the following six major blocks:

- An EHCI block for high-speed transfers (HS mode, 480 Mbps)
- 2 OHCI blocks for full and low speed transfers (FS and LS modes, 12 and 1.5 Mbps)
- Local 2-Kbyte FIFO
- Local DMA
- Integrated USB2 transceiver (PHY)

This host can manage an external power switch, providing a control line to enable or disable the power, and an input line to sense any over-current condition detected by the external switch.

The Host controller is capable of managing two different devices at a time on its two downstream ports.

- An HS device connected to either of the two ports is managed by the EHCI.
- An FS/LS device connected to port0 is managed by OHCI0.
- An FS/LS device connected to port1 is managed by OHCI1.

## 2.26 USB2 device controller

### Main features:

- Supports the 480 Mbps high-speed mode (HS) for USB 2.0, as well as the 12 Mbps full-speed (FS) and the 1.5 Mbps low-speed (LS modes) for USB 1.1
- Supports 16 physical endpoints, which can be assigned to different interfaces and configurations to implement logical endpoints
- Integrated USB transceiver (PHY)
- Local 4 Kbyte FIFO shared by all endpoints
- DMA mode and slave-only mode are supported
- In DMA mode, the UDC supports descriptor-based memory structures in application memory
- In both modes, an AHB slave is provided by UDC-AHB, acting as programming interface to access to memory-mapped control and status registers (CSRs)
- An AHB master for data transfer to system memory is provided, supporting 8, 16, and 32-bit wide data transactions on the AHB bus
- A USB plug detect (UPD) which detects the connection of a cable.

## 2.27 JPEG (CODEC)

SPEAr300 provides a JPEG CODEC with header processing (JPGC), able to decode (or encode) image data contained in the RAM memory, from the JPEG (or MCU) format to the MCU (or JPEG) format.

### Main features:

- Compliance with the baseline JPEG standard (ISO/IEC 10918-1)
- Single-clock per pixel encoding/decoding
- Support for up to four channels of component color
- 8-bit/channel pixel depths
- Programmable quantization tables (up to four)
- Programmable Huffman tables (two AC and two DC)
- Programmable minimum coded unit (MCU)
- Configurable JPEG headers processing
- Support for restart marker insertion
- Use of two DMA channels and of two 8 x 32-bits FIFO's (local to the JPEG) for efficient transferring and buffering of encoded/decoded data from/to the CODEC core.

## 2.28 Cryptographic co-processor (C3)

### Main features:

- Supported cryptographic algorithms:
  - Advanced encryption standard (AES) cipher in ECB, CBC, CTR modes
  - Data encryption standard (DES) cipher in ECB and CBC modes.
  - SHA-1, HMAC-SHA-1, MD5, HMAC-MD5 digests.
- Instruction driven DMA based programmable engine.
- AHB master port for data access from/to system memory.
- AHB slave port for co-processor register accesses and initial engine-setup
- The co-processor is fully autonomous (DMA input reading, cryptographic operation execution, DMA output writing) after being set up by the host processor
- The co-processor executes programs written by the host in memory, it can execute an unlimited list of programs.
- The co-processor supports hardware chaining of cryptographic blocks for optimized execution of data-flow requiring multiple algorithms processing over the same set of data (for example encryption + hashing on the fly)

## 2.29 8-channel ADC

### Main features:

- Successive approximation conversion method
- 10-bit resolution @1 Msps
- Hardware supporting up to 13.5 bits resolution at 8 ksps by oversampling and accumulation
- Eight analog input (AIN) channels, ranging from 0 to 2.5 V
- $INL \pm 1$  LSB,  $DNL \pm 1$  LSB
- Programmable conversion speed, (min. conversion time is 1 s)
- Programmable average results from 1 (no averaging) up to 128
- Programmable auto scan for all the eight channels.
- Normal or enhanced mode;
  - In normal mode the conversion start upon CPU request
  - In enhanced mode the ADC converts continuously the selected channels inserting a selectable amount of time between two conversions.

## 2.30 1-bit DAC

The one-bit DAC is a second-order noise shaper based on the TDM hardware. The action memory determines whether a new sample needs to be sent to the DAC during the next byte. Samples are read from the buffer memory.

**Main features:**

- Input data must be 32-bits wide, either in 2's complement or binary form.
- Oversampling min 32, max 256
- S/N ratio is 82 dB, THD is 72 dB (Measured on a 1 kHz sine wave x64 over sampled by the processor and x32 by the DAC)
- Dynamic: 80% of full scale
- Optionally, the order of the noise shaper can be set to 1

### 3 Pin description

The following tables describe the pinout of the SPEAr300 listed by functional block.

#### List of abbreviations:

PU = Pull Up

PD = Pull Down

#### 3.1 Required external components

1. DDR\_COMP\_1V8: place an external 121 kΩ resistor between ball P4 and ball R4
2. USB\_TX\_RTUNE: connect an external 43.2 kΩ pull-down resistor to ball K5
3. DIGITAL\_REXT: place an external 121 kΩ resistor between ball G4 and ball F4.

#### 3.2 Dedicated pins

**Table 2. Master clock, RTC, Reset and 3.3 V comparator pin descriptions**

| Group        | Signal name     | Ball | Direction | Function                     | Pin type   |
|--------------|-----------------|------|-----------|------------------------------|--|
| Master Clock | MCLK_XI         | P1   | Input     | 24 MHz (typical) crystal in  | Oscillator 2.5 V capable                             |
|              | MCLK_XO         | P2   | Output    | 24 MHz (typical) crystal out |  |
| RTC          | RTC_XI          | E2   | Input     | 32 kHz crystal in            | Oscillator 1.5 V capable                             |
|              | RTC_XO          | E1   | Output    | 32 kHz crystal out           |  |
| Reset        | MRESET#         | M17  | Input     | Main Reset                   | TTL Schmitt trigger input buffer, 3.3 V tolerant, PU |
| 3.3 V Comp.  | DIGITAL_REXT    | G4   | Output    | Configuration                | Analog, 3.3 V capable                                |
|              | DIGITAL_GND_REX | F4   | Power     | Power                        | Power  |

**Table 3. Power supply pin description**

| Group          | Signal name | Ball   | Value |
|----------------|-------------|--|-------|
| DIGITAL GROUND | GND         | G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L6, L7, L8, L9, L10, M8, M9, M10 | 0 V   |
| ANALOG GROUND  | AGND        | F2, G1, J2, L1, L3, L5, N2, N4, P3, R3, N12  | 0 V   |
| I/O            | VDD3        | F5, F6, F7, F10, F11, F12, G5, J12, K12, L12, M12  | 3.3 V |

**Table 3. Power supply pin description (continued)**

| Group               | Signal name  | Ball                                       | Value |
|---------------------|--------------|--|-------|
| CORE                | VDD          | F8, F9, G12, H5, H12, J5, L11, M6, M7, M11 | 1.2 V |
| USB HOST0 PHY       | HOST0_VDDbc  | L2   | 2.5 V |
|                     | HOST0_VDDb3  | K4   | 3.3 V |
|                     | HOST0_VDDbs  | M3   | 1.2 V |
| USB HOST 1 PHY      | HOST1_VDDbc  | K3   | 2.5 V |
|                     | HOST1_VDDb3  | J1   | 3.3 V |
|                     | HOST1_VDDbs  | M3   | 1.2 V |
| USB DEVICE PHY      | DEVICE_VDDbc | N1   | 2.5 V |
|                     | DEVICE_VDDb3 | N3   | 3.3 V |
|                     | HOST0_VDDbs  | M3   | 1.2V  |
| OSCI (master clock) | MCLK_VDD     | R1   | 1.2V  |
|                     | MCLK_VDD2v5  | R2   | 2.5 V |
| PLL1                | DITH1_AVDD   | G2   | 2.5 V |
| PLL2                | DITH2_AVDD   | M4   | 2.5 V |
| DDR I/O             | SSTL_VDDe    | M5, N5, N6, N7, N8, N9, N10, N11           | 1.8 V |
| ADC                 | ADC_AVDD     | N13  | 2.5 V |
| OSCI RTC            | RTC VDD      | F1   | 1.5 V |

**Table 4. Debug pin descriptions**

| Group | Signal name | Ball  | Direction        | Function  | Pin type   |
|-------|-------------|-------|------------------|---|--|
| DEBUG | TEST_0      | K16   | Input            | Test[4:0] configuration ports. For functional mode, they have to be set to 00110. | TTL input buffer, 3.3 V tolerant, PD                 |
|       | TEST_1      | K15   |                  |   |  |
|       | TEST_2      | K14   |                  |   |  |
|       | TEST_3      | K13   |                  |   |  |
|       | TEST_4      | J15   |                  |   |  |
|       | BOOT_SEL    | J14   |                  |   |  |
|       | nTRST       | L16   | Input            | Test reset input  | TTL Schmitt trigger input buffer, 3.3 V tolerant, PU |
|       | TDO         | L15   | Output           | Test data output  | TTL output buffer, 3.3 V capable 4 mA                |
|       | TCK         | L17   | Input            | Test clock  | TTL Schmitt trigger input buffer, 3.3 V tolerant, PU |
|       | TDI         | L14   | Input            | Test data input   |  |
| TMS   | L13         | Input | Test mode select |   |  |

**Table 5. Serial memory interface (SMI) pin description**

| Group | Signal name | Ball | Direction | Function                 | Pin type                                |
|-------|-------------|------|-----------|--------------------------|---|
| SMI   | SMI_DATAIN  | M13  | Input     | Serial Flash input data  | TTL Input Buffer<br>3.3 V tolerant, PU  |
|       | SMI_DATAOUT | M14  | Output    | Serial Flash output data | TTL output buffer<br>3.3 V capable 4 mA |
|       | SMI_CLK     | N17  | I/O       | Serial Flash clock       |   |
|       | SMI_CS_0    | M15  | Output    | Serial Flash chip select |   |
|       | SMI_CS_1    | M16  |           |                          |   |

**Table 6. USB pin descriptions**

| Group    | Signal name         | Ball | Direction | Function               | Pin type                                 |
|----------|---------------------|------|-----------|------------------------|--|
| USB DEV  | DEV_DP              | M1   | I/O       | USB Device D+          | Bidirectional analog buffer 5 V tolerant |
|          | DEV_DM              | M2   |           | USB Device D-          |  |
|          | DEV_VBUS            | G3   | Input     | USB Device VBUS        | TTL input buffer 3.3 V tolerant, PD      |
|          | HOST1_DP            | H1   | I/O       | USB HOST1 D+           | Bidirectional analog buffer 5 V tolerant |
|          | HOST1_DM            | H2   |           | USB HOST1 D-           |  |
| USB HOST | HOST1_VBUS          | H3   | Output    | USBHOST1 VBUS          | TTL output buffer 3.3 V capable, 4 mA    |
|          | HOST1_OVRC          | J4   | Input     | USB Host1 Over-Current | TTL input buffer 3.3 V tolerant, PD      |
|          | HOST0_DP            | K1   | I/O       | USB HOST0 D+           | Bidirectional analog buffer 5 V tolerant |
|          | HOST0_DM            | K2   |           | USB HOST0 D-           |  |
|          | HOST0_VBUS          | J3   | Output    | USB HOST0 VBUS         | TTL output buffer 3.3 V capable, 4 mA    |
|          | HOST0_OVRC          | H4   | Input     | USB Host0 Over-current | TTL Input Buffer 3.3 V tolerant, PD      |
|          | USB_TXRTUNE         | K5   | Output    | Reference resistor     | Analog                                   |
|          | USB_ANALOG_T<br>EST | L4   | Output    | Analog Test Output     | Analog                                   |

**Table 7. ADC pin description**

| Group     | Signal name | Ball                           | Direction | Function                       | Pin type                     |
|-----------|-------------|--------------------------------|-----------|--------------------------------|------------------------------|
| ADC       | AIN_0       | N16                            | Input     | ADC analog input channel       | Analog buffer 2.5 V tolerant |
|           | AIN_1       | N15                            |           |                                |                              |
|           | AIN_2       | P17                            |           |                                |                              |
|           | AIN_3       | P16                            |           |                                |                              |
|           | AIN_4       | P15                            |           |                                |                              |
|           | AIN_5       | R17                            |           |                                |                              |
|           | AIN_6       | R16                            |           |                                |                              |
|           | AIN_7       | R15                            |           |                                |                              |
|           | ADC_VREFN   | N14                            |           | ADC negative voltage reference |                              |
| ADC_VREFP | P14         | ADC positive voltage reference |           |                                |                              |



**Table 8. DDR pin description**

| Group     | Signal name | Ball   | Direction          | Function                       | Pin type       |
|-----------|-------------|--------|--------------------|--------------------------------|----------------|
| DDR       | DDR_ADD_0   | T2     | Output             | Address Line                   | SSTL_2/SSTL_18 |
|           | DDR_ADD_1   | T1     |                    |                                |                |
|           | DDR_ADD_2   | U1     |                    |                                |                |
|           | DDR_ADD_3   | U2     |                    |                                |                |
|           | DDR_ADD_4   | U3     |                    |                                |                |
|           | DDR_ADD_5   | U4     |                    |                                |                |
|           | DDR_ADD_6   | U5     |                    |                                |                |
|           | DDR_ADD_7   | T5     |                    |                                |                |
|           | DDR_ADD_8   | R5     |                    |                                |                |
|           | DDR_ADD_9   | P5     |                    |                                |                |
|           | DDR_ADD_10  | P6     |                    |                                |                |
|           | DDR_ADD_11  | R6     |                    |                                |                |
|           | DDR_ADD_12  | T6     |                    |                                |                |
|           | DDR_ADD_13  | U6     |                    |                                |                |
|           | DDR_ADD_14  | R7     |                    |                                |                |
|           | DDR_BA_0    | P7     | Output             | Bank select                    | SSTL_2/SSTL_18 |
|           | DDR_BA_1    | P8     |                    |                                |                |
|           | DDR_BA_2    | R8     |                    |                                |                |
|           | DDR_RAS     | U8     | Output             | Row Add. Strobe                | SSTL_2/SSTL_18 |
|           | DDR_CAS     | T8     | Output             | Col. Add. Strobe               |                |
| DDR_WE    | T7          | Output | Write enable       |                                |                |
| DDR_CLKEN | U7          | Output | Clock enable       |                                |                |
| DDR_CLK_P | T9          | Output | Differential clock | Differential<br>SSTL_2/SSTL_18 |                |
| DDR_CLK_N | U9          |        |                    |                                |                |

**Table 8. DDR pin description (continued)**

| Group | Signal name        | Ball | Direction | Function                        | Pin type                            |
|-------|--------------------|------|-----------|---------------------------------|-------------------------------------|
| DDR   | DDR_CS_0           | P9   | Output    | Chip Select                     | SSTL_2/SSTL_18                      |
|       | DDR_CS_1           | R9   |           |                                 |                                     |
|       | DDR_ODT_0          | T3   | I/O       | On-Die Termination Enable lines |                                     |
|       | DDR_ODT_1          | T4   |           |                                 |                                     |
|       | DDR_DATA_0         | P11  | I/O       | Data Lines (Lower byte)         |                                     |
|       | DDR_DATA_1         | R11  |           |                                 |                                     |
|       | DDR_DATA_2         | T11  |           |                                 |                                     |
|       | DDR_DATA_3         | U11  |           |                                 |                                     |
|       | DDR_DATA_4         | T12  |           |                                 |                                     |
|       | DDR_DATA_5         | R12  |           |                                 |                                     |
|       | DDR_DATA_6         | P12  |           |                                 |                                     |
|       | DDR_DATA_7         | P13  |           |                                 |                                     |
|       | DDR_DQS_0          | U10  | Output    | Lower Data Strobe               | Differential SSTL_2/SSTL_18         |
|       | DDR_nDQS_0         | T10  |           |                                 |                                     |
|       | DDR_DM_0           | U12  | Output    | Lower Data Mask                 | SSTL_2/SSTL_18                      |
|       | DDR_GATE_0         | R10  | I/O       | Lower Gate Open                 |                                     |
|       | DDR_DATA_8         | T17  | I/O       | Data Lines (Upper byte)         |                                     |
|       | DDR_DATA_9         | T16  |           |                                 |                                     |
|       | DDR_DATA_10        | U17  |           |                                 |                                     |
|       | DDR_DATA_11        | U16  |           |                                 |                                     |
|       | DDR_DATA_12        | U14  |           |                                 |                                     |
|       | DDR_DATA_13        | U13  |           |                                 |                                     |
|       | DDR_DATA_14        | T13  |           |                                 |                                     |
|       | DDR_DATA_15        | R13  |           |                                 |                                     |
|       | DDR_DQS_1          | U15  | I/O       | Upper Data Strobe               | Differential SSTL_2/SSTL_18         |
|       | DDR_nDQS_1         | T15  |           |                                 |                                     |
|       | DDR_DM_1           | T14  | I/O       | Upper Data Mask                 | SSTL_2/SSTL_18                      |
|       | DDR_GATE_1         | R14  |           | Upper Gate Open                 |                                     |
|       | DDR_VREF           | P10  | Input     | Reference Voltage               | Analog                              |
|       | DDR_MEM_COM P_GND  | R4   | Power     | Return for Ext. Resistors       | Power                               |
|       | DDR_MEM_COM P_REXT | P4   | Power     | Ext. Resistor                   | Analog                              |
|       | DDR2_EN            | J13  | Input     | Configuration                   | TTL Input Buffer 3.3 V Tolerant, PU |

### 3.3 Shared I/O pins (PL\_GPIOs)

SPEAr300 devices feature, in the Reconfigurable Array Subsystem (RAS), specific sets of IPs as well as groups of software controllable GPIOs (that can be used alternatively). In the SPEAr300 the following IPs are implemented in the RAS:

- FSMC NAND/NOR Flash interface
- GPIO/Keyboard controller
- 8-bit camera interface
- CLCD controller interface
- Digital-to-analog converter (DAC)
- I2S
- 4 SPI/I2C control signals
- TDM block
- SDIO interface
- GPIOs

The 98 PL\_GPIO and 4 PL\_CLK pins have the following characteristics:

- Output buffer: TTL 3.3 V capable up to 10 mA
- Input buffer: TTL, 3.3 V tolerant, selectable internal pull up/pull down (PU/PD)

The PL\_GPIOs can be configured in 13 different modes. This allows SPEAr300 to be tailored for use in various applications, see [Section 3.3.2](#).

#### 3.3.1 PL\_GPIO pin description

**Table 9. PL\_GPIO pin description**

| Group    | Signal name                | Ball                            | Direction | Function  | Pin type  |
|----------|----------------------------|---------------------------------|-----------|---|---|
| PL_GPIOs | PL_GPIO_97...<br>PL_GPIO_0 | (see <a href="#">Table 11</a> ) | I/O       | General purpose I/O or multiplexed pins (see <a href="#">Table 11</a> ) | (see the introduction of the <a href="#">Section 3.3</a> above) |
|          | PL_CLK1...<br>PL_CLK4      |                                 |           | Programmable logic external clocks                                      |   |

#### 3.3.2 Configuration modes

This section describes the main operating modes created by using a selection of the embedded IPs.

13 configurations are available selected by RAS register 2. The peripherals available in each configuration are shown in [Table 10: Available peripherals in each configuration mode](#). Details of each PL\_GPIO pin are given for each mode in [Table 11: PL\\_GPIO multiplexing scheme](#).

The following modes can be selected by programming some control registers present in the reconfigurable array subsystem.

- NAND mode
- NOR Mode
- PHOTO\_FRAME Mode (PHOTO FRAME)
- LEND\_IP\_PHONE Mode (LOW END IP PHONE)
- HEND\_IP\_PHONE Mode (HIGH END IP PHONE)
- LEND\_WIFI\_PHONE Mode (LOW END WI-FI PHONE)
- HEND\_WIFI\_PHONE Mode (HIGH END WI-FI PHONE)
- ATA\_PABX\_wI2S Mode (ATA PABX without I2S)
- ATA\_PABX\_I2S Mode (ATA PABX with I2S)
- CAMI\_LCDw Mode (8-bit CAMERA without LCD)
- CAMu\_LCD Mode (14-bit camera with LCD)
- CAMu\_wLCD Mode (14-bit camera without LCD)
- CAMI\_LCD Mode (8-bit camera with LCD)

Configuration 1 is the default mode for SPEAr300. It supports the FSMC interface for NAND Flash connectivity and boot pins used for selecting the boot mode.

#### **Mode 1: NAND interface**

NAND mode mainly provides:

- NAND Flash interface (16 bits, 5 control signals)

#### **Mode 2: NOR interface**

NOR mode mainly provides:

- External Memory Interface (16 data bits, 24 address bits and 4 chip selects)

#### **Mode 3: Photo frame**

Photo frame mode mainly provides:

- NAND Flash interface (16 bits, 5 control signals)
- CLCD controller interface
- TDM for voice/music capabilities
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

#### **Mode 4: Low end IP phone**

Low end IP phone mode mainly provides:

- 9x9 keyboard
- 8 SPI/I2C control signals
- I2S block
- GPIOs with interrupt capability
- Digital-to-analog converter (DAC)

**Mode 5: High end IP phone**

Main features:

- 9x9 keyboard
- CLCD controller interface
- 4 SPI/I2C control signals
- Digital-to-analog converter (DAC)
- TDM block capable of communicating with 2 external devices
- I2S block
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

**Mode 6: Low end Wifi phone**

Main features:

- 9x9 keyboard
- 8 SPI/I2C control signals
- Digital-to-analog converter (DAC)
- TDM block capable of communicating with 8 external devices
- I2S block
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

**Mode 7: High end Wifi phone**

Main features:

- 9x9 keyboard
- CLCD controller interface
- 4 SPI/I2C control signals
- Digital-to-analog converter (DAC)
- TDM block capable of communicating with 2 external devices
- I2S block
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

**Mode 8: ATA PABX without I2S**

Main features:

- 8 SPI/I2C control signals
- TDM block capable of communicating with 8 external devices
- SDIO interface supporting SPI, SD1 and SD4 mode
- External Memory Interface (8 data bits, 8 address bits and 4 control signals)
- GPIOs with interrupt capability

**Mode 9: ATA PABX with I2S**

Main features:

- NAND Flash interface (8 bits, 5 control signals)
- External Memory Interface (8 data bits, 8 address bits and 4 control signals)
- 8 SPI/I2C control signals
- Digital-to-analog converter (DAC)
- I2S block
- TDM block capable of communicating with 4 external devices
- SDIO interface supporting SPI, SD1 and SD4 mode
- GPIOs with interrupt capability

#### **Mode 10: 8-bit camera without LCD**

Main features:

- 8-bit camera interface
- 9x9 keyboard
- 4 SPI/I2C control signals
- Digital-to-analog converter (DAC)
- I2S block
- TDM block capable of communicating with 2 external devices
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

#### **Mode 11: 14-bit camera with LCD**

Main features:

- 14-bit camera interface
- 7x5 keyboard
- CLCD controller interface
- Digital-to-analog converter (DAC)
- I2S block
- TDM block capable of communicating with 2 external devices
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

#### **Mode 12: 14-bit camera without LCD**

Main features:

- 14-bit camera interface
- 7x5 keyboard
- Digital-to-analog converter (DAC)
- I2S block
- TDM block capable of communicating with 2 external devices
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

### Mode 13: 8-bit camera with LCD

Main features:

- 8-bit camera interface
- 9x9 keyboard
- CLCD controller interface
- Digital-to-analog converter (DAC)
- I2S block
- 4 SPI/I2C control signals
- TDM block capable of communicating with 2 external devices
- SDIO interface supporting SPI, SD1, SD4 and SD8 mode
- GPIOs with interrupt capability

#### 3.3.3 Alternate functions

Other peripheral functions are listed in the Alternate Functions column of [Table 11: PL\\_GPIO multiplexing scheme](#) and can be enabled/disabled using by via RAS register 1. Refer to the user manual for the register descriptions.

#### 3.3.4 Boot pins

The status of the boot pins is read at startup by the BootROM. Refer to the description of the Boot register in the SPEAr300 user manual.

#### 3.3.5 GPIOs

Some PL\_GPIO pins can be used as software controlled general purpose I/Os (GPIOs) .

- 6 base GPIOs can be enabled as alternate functions on PL\_GPIO.
- 18 GPIO are provided by the RAS IPs G8 and G10 on PL\_GPIO.
- 18 GPIOs are available if the GPIO/ keyboard controller is configured in GPIO mode.

#### 3.3.6 Multiplexing scheme

The two multiplexers shown in [Figure 4](#) are controlled by different registers. The first multiplexer selects the I/O functions of the RAS IPs in one of 13 modes shown in “Configuration mode” columns in [Table 11](#)). This selection is programmable via 4 bits in RAS register 2.

The second multiplexer is controlled by RAS register 1 and allows you to enable the I/O functions shown in alternate functions column of [Table 11](#).

To get more information about these registers, please refer to the SPEAr300 user manual.

**Figure 4. Multiplexing scheme**

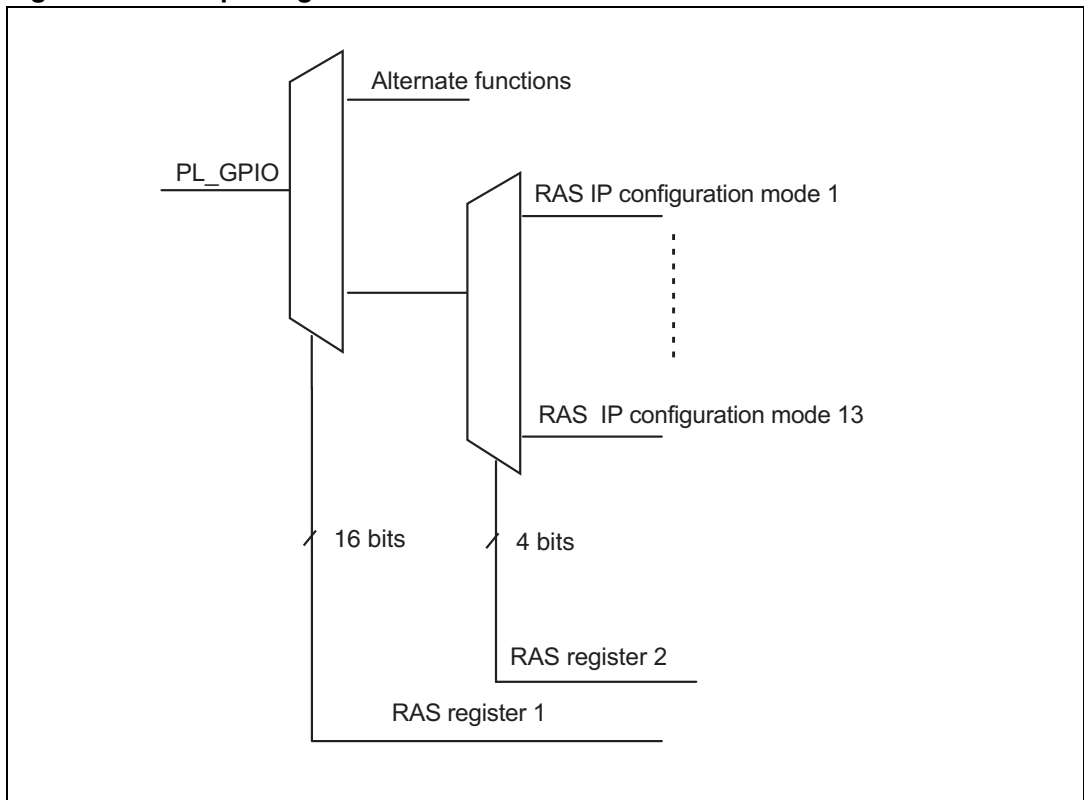




Table 10. Available peripherals in each configuration mode

| Modes | FSMC                  | Boot pins | SPI/I2C<br>Multi slave control | I2S | CLCD | DAC | Camera interface | TDM No of voice<br>devices | SDIO/MMC<br>data lines | Keyboard<br>keys | GPIOs            |               |            |             |                           |
|-------|-----------------------|-----------|--------------------------------|-----|------|-----|------------------|----------------------------|------------------------|------------------|------------------|---------------|------------|-------------|---------------------------|
|       |                       |           |                                |     |      |     |                  |                            |                        |                  | Max. no. of I/Os | Bidirectional | Input only | Output only | Special outputs<br>(sync) |
| 1     | 16-bit<br>NAND        | 4         |                                |     |      |     |                  |                            |                        |                  | 18               | 6             | 12         |             | 6                         |
| 2     | 16-bit<br>NOR         | 4         |                                |     |      |     |                  |                            |                        |                  | 18               | 6             | 12         |             | 6                         |
| 3     | 16-bit<br>NAND        |           |                                |     | 1    |     |                  | 1                          | 8                      |                  | 28               | 28            |            |             | 22                        |
| 4     |                       |           | 8                              | 1   |      | 1   |                  | 8                          | 8                      | 9*9              | 62               | 38            | 8          | 12          | 4                         |
| 5     |                       |           | 4                              | 1   | 1    | 1   |                  | 2                          | 8                      | 9*9              | 42               | 38            |            | 4           | 14                        |
| 6     |                       |           | 8                              | 1   |      | 1   |                  | 8                          | 8                      | 9*9              | 58               | 38            | 8          | 8           | 4                         |
| 7     |                       |           | 4                              | 1   | 1    | 1   |                  | 2                          | 8                      | 9*9              | 42               | 38            |            | 4           | 14                        |
| 8     | 8-bit<br>NOR          |           | 8                              |     |      |     |                  | 8                          | 4                      |                  | 44               | 24            | 8          | 8           | 4                         |
| 9     | 8-bit<br>NAND<br>/NOR |           | 8                              | 1   |      | 1   |                  | 4                          | 4                      |                  | 42               | 24            | 8          | 8           | 2                         |
| 10    |                       |           | 4                              | 1   |      | 1   | 8-bit            | 2                          | 8                      | 9*9              | 36               | 32            |            | 4           | 10                        |
| 11    |                       |           |                                | 1   | 1    | 1   | 14-bit           | 2                          | 8                      | 7*5              | 26               | 26            |            |             | 10                        |
| 12    |                       |           |                                | 1   |      | 1   | 14-bit           | 2                          | 8                      | 7*5              | 26               | 26            |            |             | 10                        |
| 13    |                       |           | 4                              | 1   | 1    | 1   | 8-bit            | 2                          | 8                      | 9*9              | 32               | 28            |            | 4           | 6                         |

### TDM interfacing using GPIOs

In some configuration modes where less than 8 TDM devices are indicated in [Table 10](#), additional TDM devices can be supported by using GPIO pins. The TDM needs a dedicated interrupt line, an SPI and an independent frame sync signal to interface each device. When enough SPI chip selects signals are not available (SPI\_I2C signals), the chip select can be performed by a GPIO. In this case the number of possible TDM devices supported is:

Modes 5, 7, 8 and 9: up to 8 devices

Modes 3 and 10: up to 6 devices

Modes 11 and 12: up to 4 devices



Table 11. PL\_GPIO multiplexing scheme

| PL_GPIO # / ball number | Configuration mode (enabled by RAS register 2) |          |      |            |      |      |      |      |      |          |        |          |      | Alternate function (enabled by RAS register 1) |
|-------------------------|--|----------|------|------------|------|------|------|------|------|----------|--------|----------|------|--|
|                         | 1  | 2        | 3    | 4          | 5    | 6    | 7    | 8    | 9    | 10       | 11     | 12       | 13   |  |
| PL_GPIO_97/H16          | /E1  | /E1      | /E1  | 1          | 1    | 1    | 1    | /E1  | /E1  | 1        | 1      | 1        | 1    |  |
| PL_GPIO_96/H15          | D0   | DQ0      | D0   | COL0       | COL0 | COL0 | COL0 | D0   | D0   | COL0     | COL0   | COL0     | COL0 |  |
| PL_GPIO_95/H14          | D1   | DQ1      | D1   | COL1       | COL1 | COL1 | COL1 | D1   | D1   | COL1     | COL1   | COL1     | COL1 |  |
| PL_GPIO_94/H13          | D2   | DQ2      | D2   | COL2       | COL2 | COL2 | COL2 | D2   | D2   | COL2     | COL2   | COL2     | COL2 |  |
| PL_GPIO_93/G17          | D3   | DQ3      | D3   | COL3       | COL3 | COL3 | COL3 | D3   | D3   | COL3     | COL3   | COL3     | COL3 |  |
| PL_GPIO_92/G16          | D4   | DQ4      | D4   | COL4       | COL4 | COL4 | COL4 | D4   | D4   | COL4     | COL4   | COL4     | COL4 |  |
| PL_GPIO_91/G15          | D5   | DQ5      | D5   | COL5       | COL5 | COL5 | COL5 | D5   | D5   | COL5     | DIO0_1 | DIO0_1   | COL5 |  |
| PL_GPIO_90/G14          | D6   | DQ6      | D6   | COL6       | COL6 | COL6 | COL6 | D6   | D6   | COL6     | DIO1_1 | DIO1_1   | COL6 |  |
| PL_GPIO_89/F17          | D7   | DQ7      | D7   | COL7       | COL7 | COL7 | COL7 | D7   | D7   | COL7     | DIO2_1 | DIO2_1   | COL7 |  |
| PL_GPIO_88/F16          | D8   | DQ8      | D8   | COL8       | COL8 | COL8 | COL8 | G8_0 | G8_0 | COL8     | DIO3_1 | DIO3_1   | COL8 |  |
| PL_GPIO_87/G13          | D9   | DQ9      | D9   | ROW0       | ROW0 | ROW0 | ROW0 | G8_1 | G8_1 | ROW0     | ROW0   | ROW0     | ROW0 |  |
| PL_GPIO_86/E17          | D10  | DQ10     | D10  | ROW1       | ROW1 | ROW1 | ROW1 | G8_2 | G8_2 | ROW1     | ROW1   | ROW1     | ROW1 |  |
| PL_GPIO_85/F15          | D11  | DQ11     | D11  | ROW2       | ROW2 | ROW2 | ROW2 | G8_3 | G8_3 | ROW2     | ROW2   | ROW2     | ROW2 |  |
| PL_GPIO_84/D17          | D12  | DQ12     | D12  | ROW3       | ROW3 | ROW3 | ROW3 | G8_4 | G8_4 | ROW3     | ROW3   | ROW3     | ROW3 |  |
| PL_GPIO_83/E16          | D13  | DQ13     | D13  | ROW4       | ROW4 | ROW4 | ROW4 | G8_5 | G8_5 | ROW4     | ROW4   | ROW4     | ROW4 |  |
| PL_GPIO_82/E15          | D14  | DQ14     | D14  | ROW5       | ROW5 | ROW5 | ROW5 | G8_6 | G8_6 | ROW5     | ROW5   | ROW5     | ROW5 |  |
| PL_GPIO_81/C17          | D15  | DQ15 A-1 | D15  | ROW6       | ROW6 | ROW6 | ROW6 | G8_7 | G8_7 | ROW6     | ROW6   | ROW6     | ROW6 |  |
| PL_GPIO_80/D16          | 0  | A0       | CLD0 | G8_0 (out) | CLD0 | 0    | CLD0 | A0   | A0   | Reserved | CLD0   | Reserved | CLD0 |  |
| PL_GPIO_79/F14          | 0  | A1       | CLD1 | G8_1 (out) | CLD1 | 0    | CLD1 | A1   | A1   | Reserved | CLD1   | Reserved | CLD1 |  |
| PL_GPIO_78/D15          | 0  | A2       | CLD2 | G8_2 (out) | CLD2 | 0    | CLD2 | A2   | A2   | Reserved | CLD2   | Reserved | CLD2 |  |
| PL_GPIO_77/B17          | 0  | A3       | CLD3 | G8_3 (out) | CLD3 | 0    | CLD3 | A3   | A3   | Reserved | CLD3   | Reserved | CLD3 |  |
| PL_GPIO_76/F13          | 0  | A4       | CLD4 | G8_4(out)  | CLD4 | 0    | CLD4 | A4   | A4   | Reserved | CLD4   | Reserved | CLD4 |  |
| PL_GPIO_75/E14          | 0  | A5       | CLD5 | G8_5 (out) | CLD5 | 0    | CLD5 | A5   | A5   | Reserved | CLD5   | Reserved | CLD5 |  |
| PL_GPIO_74/C16          | 0  | A6       | CLD6 | G8_6 (out) | CLD6 | 0    | CLD6 | A6   | A6   | Reserved | CLD6   | Reserved | CLD6 |  |

**Table 11. PL\_GPIO multiplexing scheme (continued)**

| PL_GPIO_# / ball number | Configuration mode (enabled by RAS register 2) |     |       |            |       |           |       |                |                |          |         |          |       | Alternate function (enabled by RAS register 1) |
|-------------------------|--|-----|-------|------------|-------|-----------|-------|----------------|----------------|----------|---------|----------|-------|--|
|                         | 1  | 2   | 3     | 4          | 5     | 6         | 7     | 8              | 9              | 10       | 11      | 12       | 13    |  |
| PL_GPIO_73/A17          | 0  | A7  | CLD7  | G8_7 (out) | CLD7  | 0         | CLD7  | A7             | A7             | Reserved | CLD7    | Reserved | CLD7  |  |
| PL_GPIO_72/B16          | 0  | A8  | CLD8  | IT0        | CLD8  | IT0       | CLD8  | IT0            | IT0            | Reserved | CLD8    | Reserved | CLD8  |  |
| PL_GPIO_71/D14          | 0  | A9  | CLD9  | IT1        | CLD9  | IT1       | CLD9  | IT1            | IT1            | Reserved | CLD9    | Reserved | CLD9  |  |
| PL_GPIO_70/C15          | 0  | A10 | CLD10 | IT2        | CLD10 | IT2       | CLD10 | IT2            | IT2            | Reserved | CLD10   | Reserved | CLD10 |  |
| PL_GPIO_69/A16          | 0  | A11 | CLD11 | IT3        | CLD11 | IT3       | CLD11 | IT3            | IT3            | Reserved | CLD11   | Reserved | CLD11 |  |
| PL_GPIO_68/B15          | 0  | A12 | CLD12 | IT4        | CLD12 | IT4       | CLD12 | IT4            | IT4            | Reserved | CLD12   | Reserved | CLD12 |  |
| PL_GPIO_67/C14          | 0  | A13 | CLD13 | IT5        | CLD13 | IT5       | CLD13 | IT5            | IT5            | Reserved | CLD13   | Reserved | CLD13 |  |
| PL_GPIO_66/E13          | 0  | A14 | CLD14 | IT6        | CLD14 | IT6       | CLD14 | IT6            | IT6            | Reserved | CLD14   | Reserved | CLD14 |  |
| PL_GPIO_65/B14          | 0  | A15 | CLD15 | IT7        | CLD15 | IT7       | CLD15 | IT7            | IT7            | Reserved | CLD15   | Reserved | CLD15 |  |
| PL_GPIO_64/D13          | 0  | A16 | CLD16 | SPI_I2C4   | CLD16 | SPI_I2C4  | CLD16 | SPI_I2C4       | SPI_I2C4       | Reserved | CLD16   | Reserved | CLD16 |  |
| PL_GPIO_63/C13          | 0  | A17 | CLD17 | SPI_I2C5   | CLD17 | SPI_I2C5  | CLD17 | SPI_I2C5       | SPI_I2C5       | Reserved | CLD17   | Reserved | CLD17 |  |
| PL_GPIO_62/A15          | 0  | A18 | CLD18 | SPI_I2C6   | CLD18 | SPI_I2C6  | CLD18 | SPI_I2C6       | SPI_I2C6       | Reserved | CLD18   | Reserved | CLD18 |  |
| PL_GPIO_61/E12          | 0  | A19 | CLD19 | SPI_I2C7   | CLD19 | SPI_I2C7  | CLD19 | SPI_I2C7 /DOUT | SPI_I2C7 /DOUT | Reserved | CLD19   | Reserved | CLD19 |  |
| PL_GPIO_60/A14          | 0  | A20 | CLD20 | TDM_SYNC4  | CLD20 | TDM_SYNC4 | CLD20 | TDM_SYNC4      | TDM_SYNC4      | Reserved | CLD20   | Reserved | CLD20 |  |
| PL_GPIO_59/B13          | 0  | A21 | CLD21 | TDM_SYNC5  | CLD21 | TDM_SYNC5 | CLD21 | TDM_SYNC5      | TDM_SYNC5      | Reserved | CLD21   | Reserved | CLD21 |  |
| PL_GPIO_58/D12          | CL   | A22 | CL    | TDM_SYNC6  | CLD22 | TDM_SYNC6 | CLD22 | TDM_SYNC6      | CL             | Reserved | CLD22   | Reserved | CLD22 |  |
| PL_GPIO_57/E11          | AL   | A23 | AL    | TDM_SYNC7  | CLD23 | TDM_SYNC7 | CLD23 | TDM_SYNC7      | AL             | Reserved | CLD23   | Reserved | CLD23 |  |
| PL_GPIO_56/C12          | /W   | /W  | /W    | ROW7       | ROW7  | ROW7      | ROW7  | /W             | /W             | ROW7     | VSYNC_1 | VSYNC_1  | ROW7  |  |
| PL_GPIO_55/A13          | /R   | /G  | /R    | ROW8       | ROW8  | ROW8      | ROW8  | /R             | /R             | ROW8     | HSYNC_1 | HSYNC_1  | ROW8  |  |
| PL_GPIO_54/E10          | 0  | 0   | CLAC  | G10_9      | CLAC  | G10_9     | CLAC  | G10_9          | G10_9          | G10_9    | CLAC    | G10_9    | CLAC  |  |
| PL_GPIO_53/D11          | 0  | 0   | CLCP  | G10_8      | CLCP  | G10_8     | CLCP  | G10_8          | G10_8          | G10_8    | CLCP    | G10_8    | CLCP  |  |
| PL_GPIO_52/B12          | 0  | 0   | CLFP  | G10_7      | CLFP  | G10_7     | CLFP  | G10_7          | G10_7          | G10_7    | CLFP    | G10_7    | CLFP  |  |



Table 11. PL\_GPIO multiplexing scheme (continued)

| PL_GPIO_# / ball number | Configuration mode (enabled by RAS register 2) |          |           |                  |                  |                  |                  |           |           |           |           |           |           | Alternate function (enabled by RAS register 1) |
|-------------------------|--|----------|-----------|------------------|------------------|------------------|------------------|-----------|-----------|-----------|-----------|-----------|-----------|--|
|                         | 1  | 2        | 3         | 4                | 5                | 6                | 7                | 8         | 9         | 10        | 11        | 12        | 13        |  |
| PL_GPIO_51/D10          | 0  | 0        | CLLP      | G10_6            | CLLP             | G10_6            | CLLP             | G10_6     | G10_6     | G10_6     | CLLP      | G10_6     | CLLP      |  |
| PL_GPIO_50/A12          | 0  | 0        | CLLE      | G10_5            | CLLE             | G10_5            | CLLE             | G10_5     | G10_5     | G10_5     | CLLE      | G10_5     | CLLE      | TMR_CPTR4                                      |
| PL_GPIO_49/C11          | 0  | 0        | CLPP      | G10_4            | CLPP             | G10_4            | CLPP             | G10_4     | G10_4     | G10_4     | CLPP      | G10_4     | CLPP      | TMR_CPTR3                                      |
| PL_GPIO_48/B11          | B0   | B0       | CLD22     | SPI_I2C0         | SPI_I2C0         | SPI_I2C0         | SPI_I2C0         | SPI_I2C0  | SPI_I2C0  | SPI_I2C0  | DIO4_1    | DIO4_1    | SPI_I2C0  | TMR_CPTR2                                      |
| PL_GPIO_47/C10          | B1   | B1       | CLD23     | SPI_I2C1         | SPI_I2C1         | SPI_I2C1         | SPI_I2C1         | SPI_I2C1  | SPI_I2C1  | SPI_I2C1  | DIO5_1    | DIO5_1    | SPI_I2C1  | TMR_CPTR1                                      |
| PL_GPIO_46/A11          | B2   | B2       | GPIO7     | SPI_I2C2         | SPI_I2C2         | SPI_I2C2         | SPI_I2C2         | SPI_I2C2  | SPI_I2C2  | SPI_I2C2  | DIO6_1    | DIO6_1    | SPI_I2C2  | TMR_CLK4                                       |
| PL_GPIO_45/B10          | B3   | B3       | GPIO6     | SPI_I2C3         | SPI_I2C3         | SPI_I2C3         | SPI_I2C3         | SPI_I2C3  | SPI_I2C3  | SPI_I2C3  | DIO7_1    | DIO7_1    | SPI_I2C3  | TMR_CLK3                                       |
| PL_GPIO_44/A10          | H0   | H0       | GPIO5     | G10_3/<br>DAC_O0 | G10_3/<br>DAC_O0 | G10_3/<br>DAC_O0 | G10_3/<br>DAC_O0 | G10_3     | DAC_O0    | DAC_O0    | DAC_O0    | DAC_O0    | DAC_O0    | TMR_CLK2                                       |
| PL_GPIO_43/E9           | H1   | H1       | GPIO4     | G10_2/<br>DAC_O1 | G10_2/<br>DAC_O1 | G10_2/<br>DAC_O1 | G10_2/<br>DAC_O1 | G10_2     | DAC_O1    | DAC_O1    | DAC_O1    | DAC_O1    | DAC_O1    | TMR_CLK1                                       |
| PL_GPIO_42/D9           | H2   | H2       | GPIO3     | I2S_DIN          | I2S_DIN          | I2S_DIN          | I2S_DIN          | G10_1     | I2S_DIN   | I2S_DIN   | I2S_DIN   | I2S_DIN   | I2S_DIN   | UART_DTR                                       |
| PL_GPIO_41/C9           | H3   | H3       | GPIO2     | I2S_LRCK         | I2S_LRCK         | I2S_LRCK         | I2S_LRCK         | G10_0     | I2S_LRCK  | I2S_LRCK  | I2S_LRCK  | I2S_LRCK  | I2S_LRCK  | UART_RI  |
| PL_GPIO_40/B9           | H4   | H4       | GPIO1     | I2S_CLK          | I2S_CLK          | I2S_CLK          | I2S_CLK          | TDM_SYNC3 | I2S_CLK   | I2S_CLK   | I2S_CLK   | I2S_CLK   | I2S_CLK   | UART_DSR                                       |
| PL_GPIO_39/A9           | H5   | H5       | GPIO0     | I2S_DOUT         | I2S_DOUT         | I2S_DOUT         | I2S_DOUT         | TDM_SYNC2 | DOUT      | I2S_DOUT  | I2S_DOUT  | I2S_DOUT  | I2S_DOUT  | UART_DCD                                       |
| PL_GPIO_38/A8           | H6   | H6       | TDM_SYNC1 | TDM_SYNC1        | TDM_SYNC1        | TDM_SYNC1        | TDM_SYNC1        | TDM_SYNC1 | TDM_SYNC1 | TDM_SYNC1 | TDM_SYNC1 | TDM_SYNC1 | TDM_SYNC1 | UART_CTS                                       |
| PL_GPIO_37/B8           | H7   | H7       | TDM_DOUT  | TDM_DOUT         | TDM_DOUT         | TDM_DOUT         | TDM_DOUT         | TDM_DOUT  | TDM_DOUT  | TDM_DOUT  | TDM_DOUT  | TDM_DOUT  | TDM_DOUT  | UART_RTS                                       |
| PL_GPIO_36/C8           | 0  | 0        | TDM_SYNC0 | TDM_SYNC0        | TDM_SYNC0        | TDM_SYNC0        | TDM_SYNC0        | TDM_SYNC0 | TDM_SYNC0 | TDM_SYNC0 | TDM_SYNC0 | TDM_SYNC0 | TDM_SYNC0 | SSP_CS4  |
| PL_GPIO_35/D8           | Reserved                                       | Reserved | TDM_CLK   | TDM_CLK          | TDM_CLK          | TDM_CLK          | TDM_CLK          | TDM_CLK   | TDM_CLK   | TDM_CLK   | TDM_CLK   | TDM_CLK   | TDM_CLK   | SSP_CS3  |
| PL_GPIO_34/E8           | 0  | 0        | TDM_DIN   | TDM_DIN          | TDM_DIN          | TDM_DIN          | TDM_DIN          | TDM_DIN   | TDM_DIN   | TDM_DIN   | TDM_DIN   | TDM_DIN   | TDM_DIN   | SSP_CS2  |
| PL_GPIO_33/E7           | 0  | 0        | SD_CMD    | SD_CMD           | SD_CMD           | SD_CMD           | SD_CMD           | SD_CMD    | SD_CMD    | SD_CMD    | SD_CMD    | SD_CMD    | SD_CMD    | BasGPIO5                                       |
| PL_GPIO_32/D7           | 0  | 0        | SD_CLK    | SD_CLK           | SD_CLK           | SD_CLK           | SD_CLK           | SD_CLK    | SD_CLK    | SD_CLK    | SD_CLK    | SD_CLK    | SD_CLK    | BasGPIO4                                       |
| PL_GPIO_31/C7           | 0  | 0        | SD_DAT0   | SD_DAT0          | SD_DAT0          | SD_DAT0          | SD_DAT0          | SD_DAT0   | SD_DAT0   | SD_DAT0   | SD_DAT0   | SD_DAT0   | SD_DAT0   | BasGPIO3                                       |

**Table 11. PL\_GPIO multiplexing scheme (continued)**

| PL_GPIO_# / ball number | Configuration mode (enabled by RAS register 2) |   |           |          |           |           |           |           |           |           |           |           |           | Alternate function (enabled by RAS register 1) |
|-------------------------|--|---|-----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|--|
|                         | 1  | 2 | 3         | 4        | 5         | 6         | 7         | 8         | 9         | 10        | 11        | 12        | 13        |  |
| PL_GPIO_30/B7           | 0  | 0 | SD_DAT1   | SD_DAT1  | SD_DAT1   | SD_DAT1   | SD_DAT1   | SD_DAT1   | SD_DAT1   | SD_DAT1   | SD_DAT1   | SD_DAT1   | SD_DAT1   | BasGPIO2                                       |
| PL_GPIO_29/A7           | 0  | 0 | SD_DAT2   | SD_DAT2  | SD_DAT2   | SD_DAT2   | SD_DAT2   | SD_DAT2   | SD_DAT2   | SD_DAT2   | SD_DAT2   | SD_DAT2   | SD_DAT2   | BasGPIO1                                       |
| PL_GPIO_28/A6           | 0  | 0 | SD_SDAT_3 | SD_SDAT3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | SD_SDAT_3 | BasGPIO0                                       |
| PL_GPIO_27/B6           | 0  | 0 | SD_SDAT_4 | SD_SDAT4 | SD_SDAT_4 | SD_SDAT_4 | SD_SDAT_4 | G8_0      | G8_0      | SD_SDAT_4 | SD_SDAT_4 | SD_SDAT_4 | SD_SDAT_4 | MII_TX_CLK                                     |
| PL_GPIO_26/A5           | 0  | 0 | SD_SDAT_5 | SD_SDAT5 | SD_SDAT_5 | SD_SDAT_5 | SD_SDAT_5 | G8_1      | G8_1      | SD_SDAT_5 | SD_SDAT_5 | SD_SDAT_5 | SD_SDAT_5 | MII_TXD0                                       |
| PL_GPIO_25/C6           | 0  | 0 | SD_SDAT_6 | SD_SDAT6 | SD_SDAT_6 | SD_SDAT_6 | SD_SDAT_6 | G8_2      | G8_2      | SD_SDAT_6 | SD_SDAT_6 | SD_SDAT_6 | SD_SDAT_6 | MII_TXD1                                       |
| PL_GPIO_24/B5           | 0  | 0 | SD_SDAT_7 | SD_SDAT7 | SD_SDAT_7 | SD_SDAT_7 | SD_SDAT_7 | G8_3      | G8_3      | SD_SDAT_7 | SD_SDAT_7 | SD_SDAT_7 | SD_SDAT_7 | MII_TXD2                                       |
| PL_GPIO_23/A4           | 0  | 0 | G8_4      | G8_4     | G8_4      | G8_4      | G8_4      | G8_4      | G8_4      | G8_4      | G8_4      | G8_4      | G8_4      | MII_TXD3                                       |
| PL_GPIO_22/D6           | 0  | 0 | G8_5      | G8_5     | G8_5      | G8_5      | G8_5      | G8_5      | G8_5      | G8_5      | G8_5      | G8_5      | G8_5      | MII_TX_EN                                      |
| PL_GPIO_21/C5           | 0  | 0 | G8_6      | G8_6     | G8_6      | G8_6      | G8_6      | G8_6      | G8_6      | DIO7      | DIO8_1    | DIO8_1    | DIO7      | MII_TX_ER                                      |
| PL_GPIO_20/B4           | 0  | 0 | G8_7      | G8_7     | G8_7      | G8_7      | G8_7      | G8_7      | G8_7      | DIO6      | DIO9_1    | DIO9_1    | DIO6      | MII_RX_CLK                                     |
| PL_GPIO_19/A3           | 0  | 0 | G10_0     | G10_0    | G10_0     | G10_0     | G10_0     | G10_0     | G10_0     | DIO5      | DIO10_1   | DIO10_1   | DIO5      | MII_RX_DV                                      |
| PL_GPIO_18/D5           | 0  | 0 | G10_1     | G10_1    | G10_1     | G10_1     | G10_1     | G10_1     | G10_1     | DIO4      | DIO11_1   | DIO11_1   | DIO4      | MII_RX_ERR                                     |
| PL_GPIO_17/C4           | 0  | 0 | G10_2     | G10_2    | G10_2     | G10_2     | G10_2     | G10_2     | G10_2     | DIO3      | DIO12_1   | DIO12_1   | DIO3      | MII_RXD0                                       |
| PL_GPIO_16/E6           | 0  | 0 | G10_3     | G10_3    | G10_3     | G10_3     | G10_3     | G10_3     | G10_3     | DIO2      | DIO13_1   | DIO13_1   | DIO2      | MII_RXD1                                       |
| PL_GPIO_15/B3           | 0  | 0 | G10_4     | G10_4    | G10_4     | G10_4     | G10_4     | G10_4     | G10_4     | DIO1      | G10_4     | G10_4     | DIO1      | MII_RXD2                                       |
| PL_GPIO_14/A2           | 0  | 0 | G10_5     | G10_5    | G10_5     | G10_5     | G10_5     | G10_5     | G10_5     | DIO0      | G10_5     | G10_5     | DIO0      | MII_RXD3                                       |
| PL_GPIO_13/A1           | 0  | 0 | G10_6     | G10_6    | G10_6     | G10_6     | G10_6     | G10_6     | G10_6     | VSYNC     | G10_6     | G10_6     | VSYNC     | MII_COL  |
| PL_GPIO_12/D4           | 0  | 0 | G10_7     | G10_7    | G10_7     | G10_7     | G10_7     | G10_7     | G10_7     | HSYNC     | G10_7     | G10_7     | HSYNC     | MII_CRS  |
| PL_GPIO_11/E5           | 0  | 0 | G10_8     | G10_8    | G10_8     | G10_8     | G10_8     | G10_8     | G10_8     | G10_8     | G10_8     | G10_8     | G10_8     | MII_MDC  |
| PL_GPIO_10/C3           | 0  | 0 | G10_9     | G10_9    | G10_9     | G10_9     | G10_9     | G10_9     | G10_9     | G10_9     | G10_9     | G10_9     | G10_9     | MII_MDIO                                       |
| PL_GPIO_9/B2            | 0  | 0 | SD_CD     | SD_CD    | SD_CD     | SD_CD     | SD_CD     | SD_CD     | SD_CD     | SD_CD     | SD_CD     | SD_CD     | SD_CD     | SSP_MOSI                                       |



Table 11. PL\_GPIO multiplexing scheme (continued)

| PL_GPIO_# / ball number | Configuration mode (enabled by RAS register 2) |          |            |           |            |           |            |           |           |           |            |         |            | Alternate function (enabled by RAS register 1) |
|-------------------------|--|----------|------------|-----------|------------|-----------|------------|-----------|-----------|-----------|------------|---------|------------|--|
|                         | 1  | 2        | 3          | 4         | 5          | 6         | 7          | 8         | 9         | 10        | 11         | 12      | 13         |  |
| PL_GPIO_8/C2            | 0  | 0        | SD_WP      | SD_WP     | SD_WP      | SD_WP     | SD_WP      | SD_WP     | SD_WP     | SD_WP     | SD_WP      | SD_WP   | SD_WP      | SSP_SCLK                                       |
| PL_GPIO_7/D3            | 0  | 0        | 0          | 0         | 0          | 0         | 0          | 0         | 0         | 0         | 0          | 0       | 0          | SSP_SS   |
| PL_GPIO_6/B1            | 0  | 0        | SD_LED     | SD_LED    | SD_LED     | SD_LED    | SD_LED     | SD_LED    | SD_LED    | SD_LED    | SD_LED     | SD_LED  | SD_LED     | SSP_MISO                                       |
| PL_GPIO_5/D2            | 0  | 0        | 0          | 0         | 0          | 0         | 0          | 0         | 0         | 0         | 0          | 0       | 0          | I2C_SDA  |
| PL_GPIO_4/C1            | 0  | 0        | 0          | 0         | 0          | 0         | 0          | 0         | 0         | 0         | 0          | 0       | 0          | I2C_SCL  |
| PL_GPIO_3/D1            | /E4  | /E4      | /E4        | 1         | 1          | 1         | 1          | 1         | 1         | 1         | 1          | 1       | 1          | UART_RX  |
| PL_GPIO_2/E4            | /E3  | /E3      | /E3        | 1         | 1          | 1         | 1          | 1         | 1         | 1         | 1          | 1       | 1          | UART_TX  |
| PL_GPIO_1/E3            | /E2  | /E2      | /E2        | 1         | 1          | 1         | 1          | 1         | 1         | 1         | 1          | 1       | 1          | IrDA_RX  |
| PL_GPIO_0/F3            | R/B  | R/B      | R/B        | 1         | 1          | 1         | 1          | R/B       | R/B       | 1         | 1          | 1       | 1          | IrDA_TX  |
| PL_CLK1/K17             | TCLK*  | TCLK*    | CCLK/TCLK* | TCLK*     | CCLK/TCLK* | TCLK*     | CCLK/TCLK* | TCLK*     | TCLK*     | TCLK*     | CCLK/TCLK* | TCLK*   | CCLK/TCLK* | PL_CLK1  |
| PL_CLK2/J17             | Reserved                                       | Reserved | int_CLK    | int_CLK   | int_CLK    | int_CLK   | int_CLK    | int_CLK   | int_CLK   | int_CLK   | int_CLK    | int_CLK | int_CLK    | PL_CLK2  |
| PL_CLK3/J16             | Reserved                                       | Reserved | \int_CLK   | \int_CLK  | \int_CLK   | \int_CLK  | \int_CLK   | \int_CLK  | \int_CLK  | \int_CLK  | CLK        | CLK     | CLK        | CLK  |
| PL_CLK4/H17             | Reserved                                       | Reserved | 2.048 MHz  | 2.048 MHz | 2.048 MHz  | 2.048 MHz | 2.048 MHz  | 2.048 MHz | 2.048 MHz | 2.048 MHz | PCLK       | PCLK    | PCLK       | PCLK   |

**Notes/legend for [Table 11](#):**

GPIO (General purpose I/O):

basGPIO: Base GPIOs in the basic subsystem (enabled as alternate functions)

G10 and G8: GPIOs in the RAS subsystem

GPIOx: GPIOs in the independent GPIO block in the RAS subsystem

TDM\_ : TDM interface signals

SD\_ : SDIO interface

IT pins: interrupts

Table cells filled with '0' or '1' are unused and unless otherwise configured as Alternate function or GPIO, the corresponding pin is held at low or high level respectively by the internal logic.

Table cells filled with 'Reserved' denote pins that must be left unconnected.

**Table 12. Table shading**

| Shading      | Pin group                                       |
|--------------|---|
| FSMC         | FSMC pins: NAND or NOR Flash                    |
| Keyboard     | Keyboard pins ROWs are outputs, COLs are inputs |
| CLCD         | Color LCD controller pins                       |
| CAMERA       | Camera pins                                     |
| UART         | UART pins                                       |
| Ethernet MAC | MII/SMII Ethernet Mac pins                      |
| SDIO/MMC     | SD card controller pins                         |
| GPT          | Timer pins                                      |
| IrDa         | IrDa pins                                       |
| SSP          | SSP pins  |
| I2C          | I2C pins  |

### 3.4 PL\_GPIO pin sharing for debug modes

In some cases the PL\_GPIO pins may be used in different ways for debugging purposes. There are three different cases (see also [Table 13](#)):

1. Case 1 - All the PL\_GPIO get values from Boundary scan registers during Ex-test instruction of JTAG . Typically this configuration is used to verify correctness of the soldering process during the production flow .
2. Case 2 - All the PL\_GPIO maintain their original meaning but the JTAG Interface is connected to the processor. This configuration is useful during the development phase but offers only "static" debug.
3. Case 3 - Some PL\_GPIO, as shown in [Table 13: Ball sharing during debug](#), are used to connect the ETM9 lines to an external box. This configuration is typically used only during the development phase. It offers a very powerful debug capability. When the processor reaches a breakpoint it is possible, by analyzing the trace buffer, to understand the reason why the processor has reached the break.

**Table 13. Ball sharing during debug**

| Signal      | Case 1 - Board Debug | Case 2 - Static Debug | Case 3 - Full Debug |
|-------------|----------------------|-----------------------|---------------------|
| Test[0]     | 0                    | 1                     | 0                   |
| Test[1]     | 0                    | 0                     | 1                   |
| Test[2]     | 0                    | 0/1                   | 0/1                 |
| Test[3]     | 0                    | 0/1                   | 0/1                 |
| Test[4]     | 1                    | 0                     | 0                   |
| nTRST       | nTRST_bscan          | nTRST_ARM             | nTRST_ARM           |
| TCK         | TCK_bscan            | TCK_ARM               | TCK_ARM             |
| TMS         | TSM_bscan            | TMS_ARM               | TSM_ARM             |
| TDI         | TDI_bscan            | TDI_ARM               | TDI_ARM             |
| TDO         | TDO_bscan            | TDO_ARM               | TDO_ARM             |
| PL_GPIO[97] | BSR Value            | Functional I/O        | ARM_TRACE_CLK       |
| PL_GPIO[96] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][0] |
| PL_GPIO[95] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][1] |
| PL_GPIO[94] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][2] |
| PL_GPIO[93] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][3] |
| PL_GPIO[92] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][0] |
| PL_GPIO[91] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][1] |
| PL_GPIO[90] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][2] |
| PL_GPIO[89] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][3] |
| PL_GPIO[88] | BSR Value            | Functional I/O        | ARM_TRACE_SYNC[A]   |
| PL_GPIO[87] | BSR Value            | Functional I/O        | ARM_TRACE_SYNC[B]   |
| PL_GPIO[86] | BSR Value            | Functional I/O        | ARM_PIPESTATA[0]    |
| PL_GPIO[85] | BSR Value            | Functional I/O        | ARM_PIPESTATA[1]    |
| PL_GPIO[84] | BSR Value            | Functional I/O        | ARM_PIPESTATA[2]    |
| PL_GPIO[83] | BSR Value            | Functional I/O        | ARM_PIPESTATB[0]    |
| PL_GPIO[82] | BSR Value            | Functional I/O        | ARM_PIPESTATB[1]    |
| PL_GPIO[81] | BSR Value            | Functional I/O        | ARM_PIPESTATB[2]    |
| PL_GPIO[80] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][4] |
| PL_GPIO[79] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][5] |
| PL_GPIO[78] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][6] |
| PL_GPIO[77] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[A][7] |
| PL_GPIO[76] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][4] |
| PL_GPIO[75] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][5] |
| PL_GPIO[74] | BSR Value            | Functional I/O        | ARM_TRACE_PKT[B][6] |



**Table 13. Ball sharing during debug (continued)**

| Signal        | Case 1 - Board Debug | Case 2 - Static Debug | Case 3 - Full Debug |
|---------------|----------------------|-----------------------|---------------------|
| PL_GPIO[73]   | BSR Value            | Functional I/O        | ARM_TRACE_PKT[7]    |
| PL_GPIO[72:0] |                      |                       |                     |

## 4 Memory mapping

**Table 14. Memory mapping**

| Start address | End address | Peripheral               | Description           |
|---------------|-------------|--------------------------|-----------------------|
| 0x0000.0000   | 0x3FFF.FFFF | External DRAM            | Low power DDR or DDR2 |
| 0x4000.0000   | 0x4FFF.FFFF | C3                       |                       |
| 0x5000.0000   | 0x5000.FFFF | Telecom register         |                       |
| 0x5001.0000   | 0x5001.0FFF | TDM                      | Action memory         |
| 0x5003.0000   | 0x5003.7FFF | TDM                      | Buffer memory         |
| 0x5004.0000   | 0x5004.0FFF | TDM                      | Sync memory           |
| 0x5005.0000   | 0x5005.0FFF | I2S                      | I2S memory bank 1     |
| 0x5005.1000   | 0x5005.1FFF | I2S                      | I2S memory bank 2     |
| 0x6000.0000   | 0x6FFF.FFFF | CLCD                     |                       |
| 0x7000.0000   | 0x7FFF.FFFF | SDIO                     |                       |
| 0x8000.0000   | 0x83FF.FFFF | Static memory controller | NAND bank0            |
| 0x8400.0000   | 0x87FF.FFFF | Static memory controller | NAND bank1            |
| 0x8800.0000   | 0x8BFF.FFFF | Static memory controller | NAND bank2            |
| 0x8C00.0000   | 0x8FFF.FFFF | Static memory controller | NAND bank3            |
| 0x9000.0000   | 0x90FF.FFFF | Static memory controller | NOR bank0             |
| 0x9100.0000   | 0x91FF.FFFF | Static memory controller | NOR bank1             |
| 0x9200.0000   | 0x91FF.FFFF | Static memory controller | NOR bank2             |
| 0x9300.0000   | 0x93FF.FFFF | Static memory controller | NOR bank3             |
| 0x9400.0000   | 0x98FF.FFFF | Static memory controller | Register              |
| 0x9900.0000   | 0x9FFF.FFFF | Registers                |                       |
| 0xA000.0000   | 0xA8FF.FFFF | Keyboard                 |                       |
| 0xA900.0000   | 0xAFFF.FFFF | GPIO                     |                       |
| 0xB000.0000   | 0xBFFF.FFFF | -                        | Reserved              |
| 0xC000.0000   | 0xCFFF.FFFF | -                        | Reserved              |
| 0xD000.0000   | 0xD007.FFFF | UART                     |                       |
| 0xD008.0000   | 0xD00F.FFFF | ADC                      |                       |
| 0xD010.0000   | 0xD017.FFFF | SPI                      |                       |
| 0xD018.0000   | 0xD01F.FFFF | I2C                      |                       |
| 0xD020.0000   | 0xD07F.FFFF | -                        | Reserved              |
| 0xD080.0000   | 0xD0FF.FFFF | JPEG CODEC               |                       |
| 0xD100.0000   | 0xD17F.FFFF | IrDA                     |                       |
| 0xD180.0000   | 0xD1FF.FFFF | -                        | Reserved              |

Table 14. Memory mapping (continued)

| Start address | End address | Peripheral              | Description                          |
|---------------|-------------|-------------------------|--------------------------------------|
| 0xD280.0000   | 0xD2FF.FFFF | SRAM                    | Static RAM shared memory (57 Kbytes) |
| 0xD300.0000   | 0xE07F.FFFF | -                       | Reserved                             |
| 0xE080.0000   | 0xE0FF.FFFF | Ethernet controller     | MAC                                  |
| 0xE100.0000   | 0xE10F.FFFF | USB 2.0 device          | FIFO                                 |
| 0xE110.0000   | 0xE11F.FFFF | USB 2.0 device          | Configuration registers              |
| 0xE120.0000   | 0xE12F.FFFF | USB 2.0 device          | Plug detect                          |
| 0xE130.0000   | 0xE17F.FFFF | -                       | Reserved                             |
| 0xE180.0000   | 0xE18F.FFFF | USB2.0 EHCI 0-1         |                                      |
| 0xE190.0000   | 0xE19F.FFFF | USB2.0 OHCI 0           |                                      |
| 0xE1A0.0000   | 0xE20F.FFFF | -                       | Reserved                             |
| 0xE210.0000   | 0xE21F.FFFF | USB2.0 OHCI 1           |                                      |
| 0xE220.0000   | 0xE27F.FFFF | -                       | Reserved                             |
| 0xE280.0000   | 0xE28F.FFFF | ML USB ARB              | Configuration register               |
| 0xE290.0000   | 0xE7FF.FFFF | -                       | Reserved                             |
| 0xE800.0000   | 0xEFFF.FFFF | -                       | Reserved                             |
| 0xF000.0000   | 0xF00F.FFFF | Timer                   |                                      |
| 0xF010.0000   | 0xF10F.FFFF | -                       | Reserved                             |
| 0xF110.0000   | 0xF11F.FFFF | VIC                     |                                      |
| 0xF120.0000   | 0xF7FF.FFFF | -                       | Reserved                             |
| 0xF800.0000   | 0xFBFF.FFFF | Serial Flash memory     |                                      |
| 0xFC00.0000   | 0xFC1F.FFFF | Serial Flash controller |                                      |
| 0xFC20.0000   | 0xFC3F.FFFF | -                       | Reserved                             |
| 0xFC40.0000   | 0xFC5F.FFFF | DMA controller          |                                      |
| 0xFC60.0000   | 0xFC7F.FFFF | DRAM controller         |                                      |
| 0xFC80.0000   | 0xFC87.FFFF | Timer 1                 |                                      |
| 0xFC88.0000   | 0xFC8F.FFFF | Watchdog timer          |                                      |
| 0xFC90.0000   | 0xFC97.FFFF | Real-time clock         |                                      |
| 0xFC98.0000   | 0xFC9F.FFFF | General purpose I/O     |                                      |
| 0xFCA0.0000   | 0xFCA7.FFFF | System controller       |                                      |
| 0xFCA8.0000   | 0xFCAF.FFFF | Miscellaneous registers |                                      |
| 0xFCB0.0000   | 0xFCB7.FFFF | Timer 2                 |                                      |
| 0xFCB8.0000   | 0xFCFF.FFFF | -                       | Reserved                             |
| 0xFD00.0000   | 0xFEFF.FFFF | -                       | Reserved                             |
| 0xFF00.0000   | 0xFFFF.FFFF | Internal ROM            | Boot                                 |

## 5 Electrical characteristics

### 5.1 Absolute maximum ratings

This product contains devices to protect the inputs against damage due to high/low static voltages. However it is advisable to take normal precaution to avoid application of any voltage higher/lower than the specified maximum/minimum rated voltages.

The absolute maximum rating is the maximum stress that can be applied to a device without causing permanent damage. However, extended exposure to minimum/maximum ratings may affect long-term device reliability.

**Table 15. Absolute maximum ratings**

| Symbol              | Parameter                             | Minimum value | Maximum value | Unit |
|---------------------|---------------------------------------|---------------|---------------|------|
| V <sub>DD</sub> 1.2 | Supply voltage for the core           | - 0.3         | 1.44          | V    |
| V <sub>DD</sub> 3.3 | Supply voltage for the I/Os           | - 0.3         | 3.9           | V    |
| V <sub>DD</sub> 2.5 | Supply voltage for the analog blocks  | - 0.3         | 3             | V    |
| V <sub>DD</sub> 1.8 | Supply voltage for the DRAM interface | - 0.3         | 2.16          | V    |
| V <sub>DD</sub> RTC | RTC supply voltage                    | -0.3          | 2.16          | V    |
| T <sub>STG</sub>    | Storage temperature                   | -55           | 150           | °C   |
| T <sub>J</sub>      | Junction temperature                  | -40           | 125           | °C   |

### 5.2 Maximum power consumption

*Note:* These values take into consideration the worst cases of process variation and voltage range and must be used to design the power supply section of the board.

**Table 16. Maximum power consumption**

| Symbol              | Description  | Max                | Unit |
|---------------------|--|--------------------|------|
| V <sub>DD</sub> 1.2 | Supply voltage for the core                          | 420                | mA   |
| V <sub>DD</sub> 1.8 | Supply voltage for the DRAM interface <sup>(1)</sup> | 160                | mA   |
| V <sub>DD</sub> RTC | RTC supply voltage                                   | 8                  | μA   |
| V <sub>DD</sub> 2.5 | Supply voltage for the analog blocks                 | 35                 | mA   |
| V <sub>DD</sub> 3.3 | Supply voltage for the I/Os <sup>(2)</sup>           | 15                 | mA   |
| P <sub>D</sub>      | Maximum power consumption                            | 930 <sup>(3)</sup> | mW   |

1. Peak current with Linux memory test (50% write and 50% read) plus DMA reading memory.

2. With 30 logic channels connected to the device and simultaneously switching at 10 MHz.

3. The maximum current and power values listed above, obtained with typical supply voltages, are not guaranteed to be the highest obtainable. These values are dependent on many factors including the type of applications running, clock rates, use of internal functional capabilities, external interface usage, case temperature, and the power supply voltages. Your specific application can produce significantly different results.

1.2 V current and power are primarily dependent on the applications running and the use of internal chip functions (DMA, USB, Ethernet, and so on).

3.3 V current and power are primarily dependent on the capacitive loading, frequency, and utilization of the external buses.

### 5.3 DC electrical characteristics

The recommended operating conditions are listed in the following table:

**Table 17. Recommended operating conditions**

| Symbol              | Parameter                            | Min  | Typ | Max  | Unit |
|---------------------|--------------------------------------|------|-----|------|------|
| V <sub>DD</sub> 1.2 | Supply voltage for the core          | 1.14 | 1.2 | 1.3  | V    |
| V <sub>DD</sub> 3.3 | Supply voltage for the I/Os          | 3    | 3.3 | 3.6  | V    |
| V <sub>DD</sub> 2.5 | Supply voltage for the analog blocks | 2.25 | 2.5 | 2.75 | V    |
| V <sub>DD</sub> 1.8 | Supply voltage for DRAM interface    | 1.70 | 1.8 | 1.9  | V    |
| V <sub>DD</sub> RTC | RTC supply voltage                   | 1.3  | 1.5 | 1.8  | V    |
| T <sub>C</sub>      | Case temperature                     | -40  |     | 85   | °C   |

### 5.4 Overshoot and undershoot

This product can support the following values of overshoot and undershoot.

**Table 18. Overshoot and undershoot specifications**

| Parameter   | 3V3 I/Os | 2V5 I/Os | 1V8 I/Os |
|---|----------|----------|----------|
| Amplitude   | 500 mV   | 500 mV   | 500 mV   |
| Ratio of overshoot (or undershoot) duration with respect to pulse width | 1/3      | 1/3      | 1/3      |

If the amplitude of the overshoot/undershoot increases (decreases), the ratio of overshoot/undershoot width to the pulse width decreases (increases). The formula relating the two is:

Amplitude of OS/US = 0.75\*(1- ratio of OS (or US) duration with respect to pulse width)

*Note:* The value of overshoot/undershoot should not exceed the value of 0.5 V. However, the duration of the overshoot/undershoot can be increased by decreasing its amplitude.

### 5.5 3.3V I/O characteristics

The 3.3 V I/Os are compliant with JEDEC standard JESD8b

**Table 19. Low voltage TTL DC input specification (3 V < V<sub>DD</sub> < 3.6 V)**

| Symbol            | Parameter                  | Min | Max | Unit |
|-------------------|----------------------------|-----|-----|------|
| V <sub>IL</sub>   | Low level input voltage    |     | 0.8 | V    |
| V <sub>IH</sub>   | High level input voltage   | 2   |     | V    |
| V <sub>hyst</sub> | Schmitt trigger hysteresis | 300 | 800 | mV   |

**Table 20. Low voltage TTL DC output specification (3 V < V<sub>DD</sub> < 3.6 V)**

| Symbol          | Parameter                 | Test condition                         | Min                   | Max | Unit |
|-----------------|---------------------------|--|-----------------------|-----|------|
| V <sub>OL</sub> | Low level output voltage  | I <sub>OL</sub> = X mA <sup>(1)</sup>  |                       | 0.3 | V    |
| V <sub>OH</sub> | High level output voltage | I <sub>OH</sub> = -X mA <sup>(1)</sup> | V <sub>DD</sub> - 0.3 |     | V    |

1. For the max current value (X mA) refer to [Section 2.29: 8-channel ADC](#).

**Table 21. Pull-up and pull-down characteristics**

| Symbol          | Parameter                       | Test condition                        | Min | Max | Unit |
|-----------------|---------------------------------|---------------------------------------|-----|-----|------|
| R <sub>PU</sub> | Equivalent pull-up resistance   | V <sub>I</sub> = 0 V                  | 29  | 67  | kΩ   |
| R <sub>PD</sub> | Equivalent pull-down resistance | V <sub>I</sub> = V <sub>DDE</sub> 3V3 | 29  | 103 | kΩ   |

### 5.6 LPDDR and DDR2 pin characteristics

**Table 22. DC characteristics**

| Symbol            | Parameter                | Test condition | Min                     | Max                      | Unit |
|-------------------|--------------------------|----------------|-------------------------|--------------------------|------|
| V <sub>IL</sub>   | Low level input voltage  | SSTL2          | -0.3                    | V <sub>REF</sub> -0.15   | V    |
|                   |                          | SSTL18         | -0.3                    | V <sub>REF</sub> -0.125  | V    |
| V <sub>IH</sub>   | High level input voltage | SSTL2          | V <sub>REF</sub> +0.15  | V <sub>DDE</sub> 2V5+0.3 | V    |
|                   |                          | SSTL18         | V <sub>REF</sub> +0.125 | V <sub>DDE</sub> 1V8+0.3 | V    |
| V <sub>hyst</sub> | Input voltage hysteresis |                | 200                     |                          | mV   |

**Table 23. Driver characteristics**

| Symbol         | Parameter                       | Min  | Typ | Max  | Unit |
|----------------|---------------------------------|------|-----|------|------|
| R <sub>O</sub> | Output impedance (strong value) | 40.5 | 45  | 49.5 | Ω    |
|                | Output impedance (weak value)   | 44.1 | 49  | 53.9 | Ω    |

**Table 24. On die termination**

| Symbol | Parameter  | Min | Typ | Max | Unit     |
|--------|--|-----|-----|-----|----------|
| RT1*   | Termination value of resistance for on die termination |     | 75  |     | $\Omega$ |
| RT2*   | Termination value of resistance for on die termination |     | 150 |     | $\Omega$ |

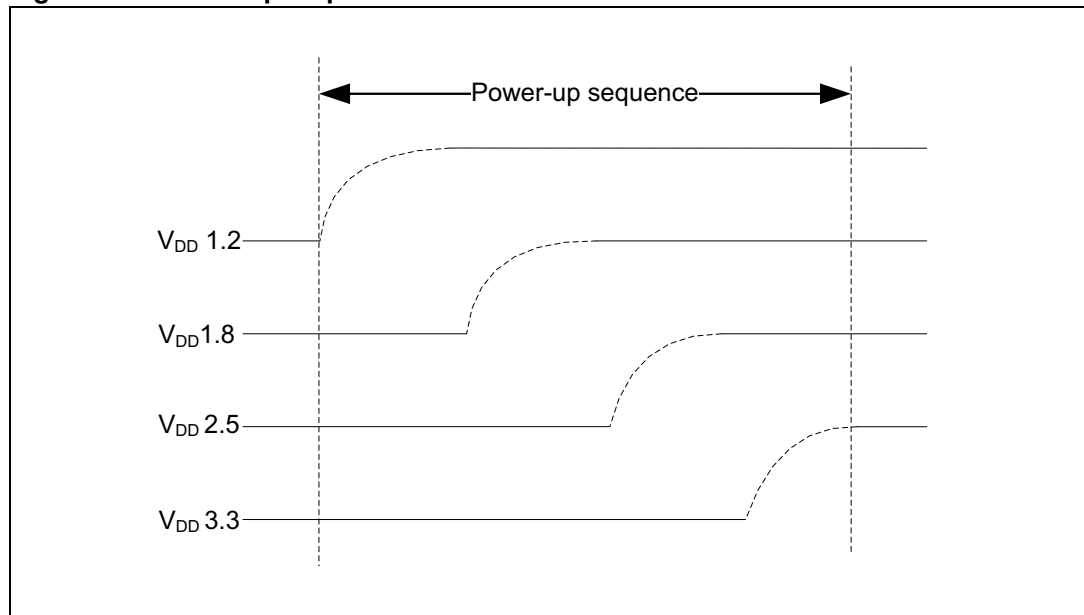
**Table 25. Reference voltage**

| Symbol      | Parameter                   | Min                 | Typ                  | Max                 | Unit |
|-------------|-----------------------------|---------------------|----------------------|---------------------|------|
| $V_{REFIN}$ | Voltage applied to core/pad | 0.49 *<br>$V_{DDE}$ | 0.500 *<br>$V_{DDE}$ | 0.51 *<br>$V_{DDE}$ | V    |

### 5.7 Power up sequence

It is recommended to power up the power supplies in the order shown in [Figure 5](#).  $V_{DD} 1.2$  is brought up first, followed by  $V_{DD} 1.8$ , then  $V_{DD} 2.5$  and finally  $V_{DD} 3.3$ .

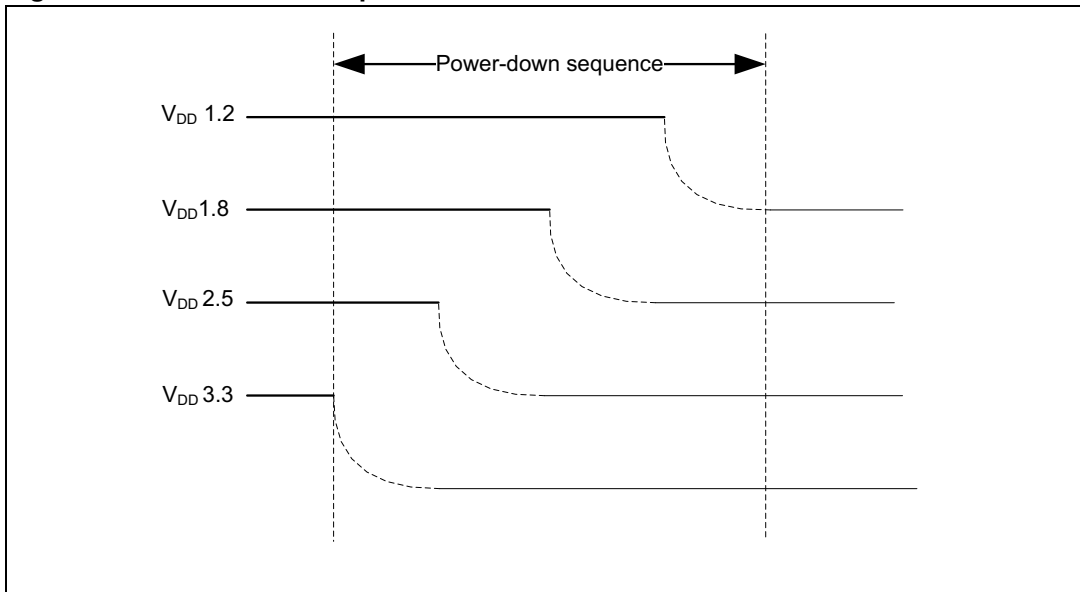
**Figure 5. Power-up sequence**



### 5.8 Removing power supplies for power saving

It is recommended to remove the the power supplies in the order shown in [Figure 6](#). So  $V_{DD} 3.3$  supply is to be removed first, then the  $V_{DD} 2.5$  supply, followed by the  $V_{DD} 1.8$  supply and last the  $V_{DD} 1.2$ .

Figure 6. Power-down sequence



### 5.9 Power on reset (MRESET)

The MRESET must remain active for at least 10 ms after all the power supplies are in the correct range and should become active in no more than 10  $\mu$ s when one of the power supplies goes out of the correct range.



## 6 Timing requirements

### 6.1 DDR2 timing characteristics

The characterization timing is done considering an output load of 10 pF on all the DDR pads. The operating conditions are in worst case  $V = 0.90\text{ V}$   $T_A = 125^\circ\text{ C}$  and in best case  $V = 1.10\text{ V}$   $T_A = 40^\circ\text{ C}$ .

#### 6.1.1 DDR2 read cycle timings

Figure 7. DDR2 Read cycle waveforms

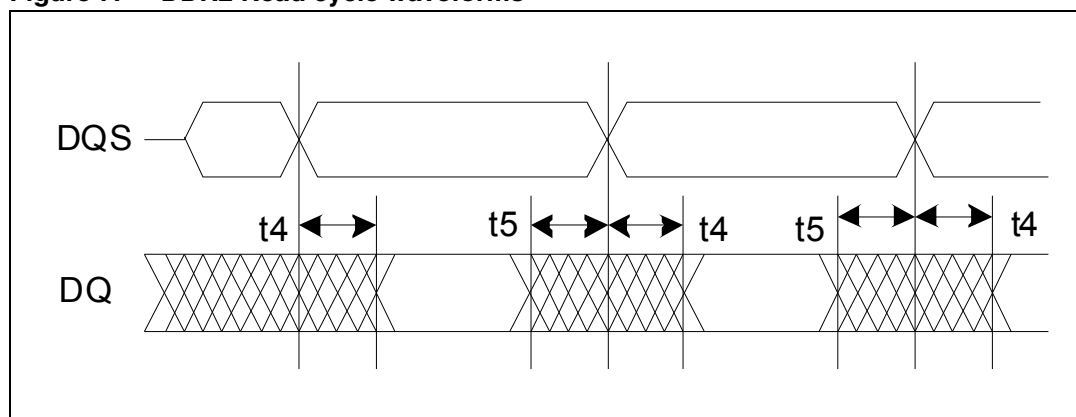


Figure 8. DDR2 Read cycle path

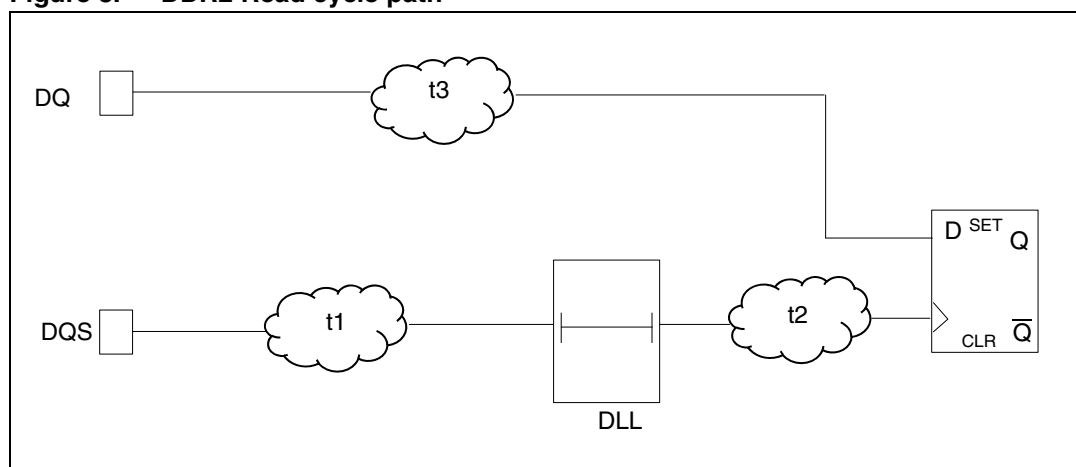


Table 26. DDR2 Read cycle timings

| Frequency | t4 max  | t5 max  |
|-----------|---------|---------|
| 333 MHz   | 1.24 ns | -495 ps |
| 266 MHz   | 1.43 ns | -306 ps |
| 200 MHz   | 1.74 ns | 4 ps    |

Table 26. DDR2 Read cycle timings (continued)

| Frequency | t4 max  | t5 max |
|-----------|---------|--------|
| 166 MHz   | 2.00 ns | 260 ps |
| 133 MHz   | 2.37 ns | 634 ps |

6.1.2 DDR2 write cycle timings

Figure 9. DDR2 Write cycle waveforms

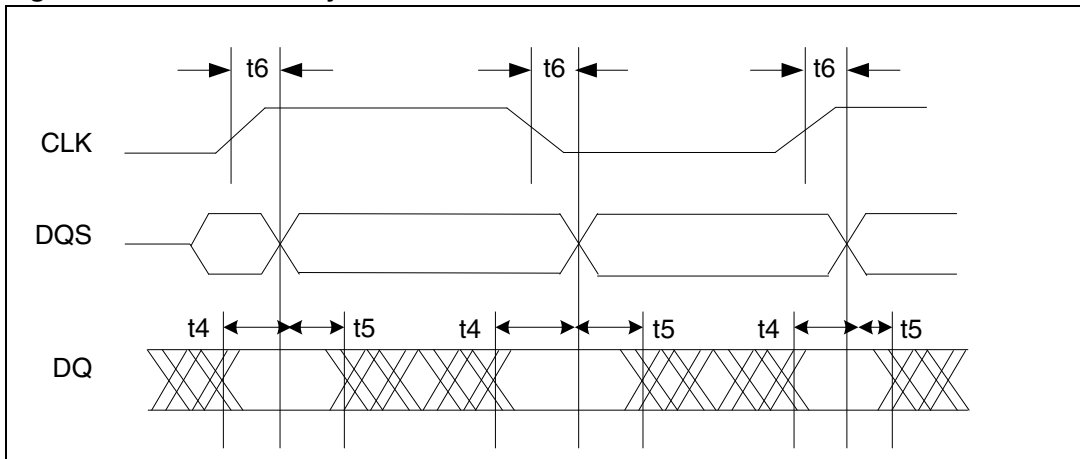


Figure 10. DDR2 Write cycle path

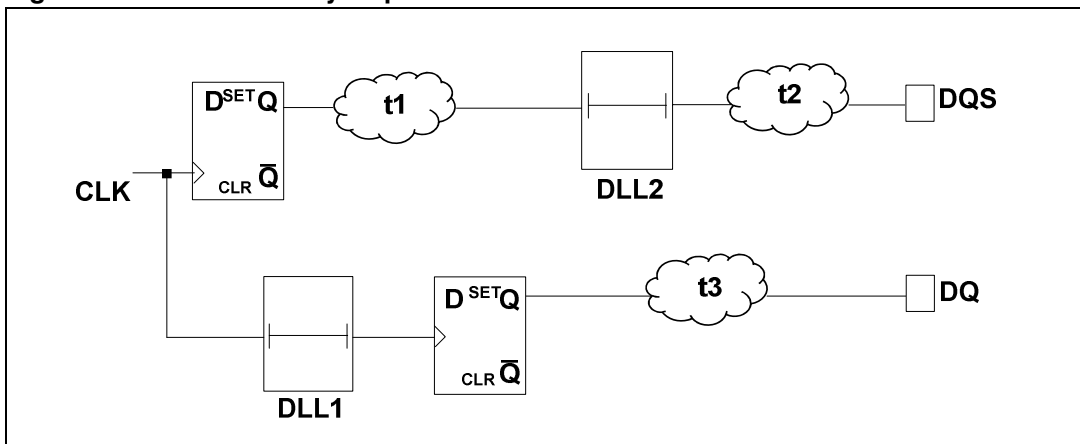


Table 27. DDR2 Write cycle timings

| Frequency | t4 max | t5 max | Unit |
|-----------|--------|--------|------|
| 333 MHz   | 1.36   | -1.55  | ns   |
| 266 MHz   | 1.55   | -1.36  | ns   |
| 200 MHz   | 1.86   | -1.05  | ns   |
| 166 MHz   | 2.11   | -794   | ns   |
| 133 MHz   | 2.49   | -420   | ns   |

### 6.1.3 DDR2 command timings

Figure 11. DDR2 Command waveforms

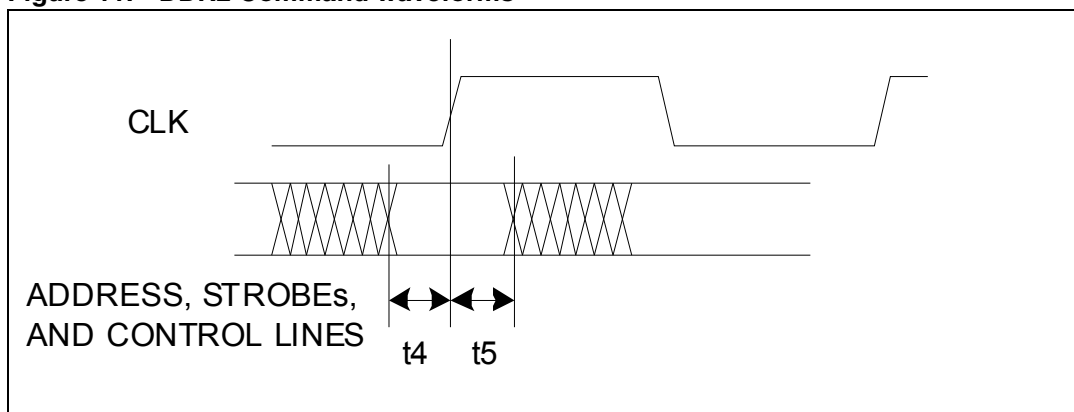


Figure 12. DDR2 Command path

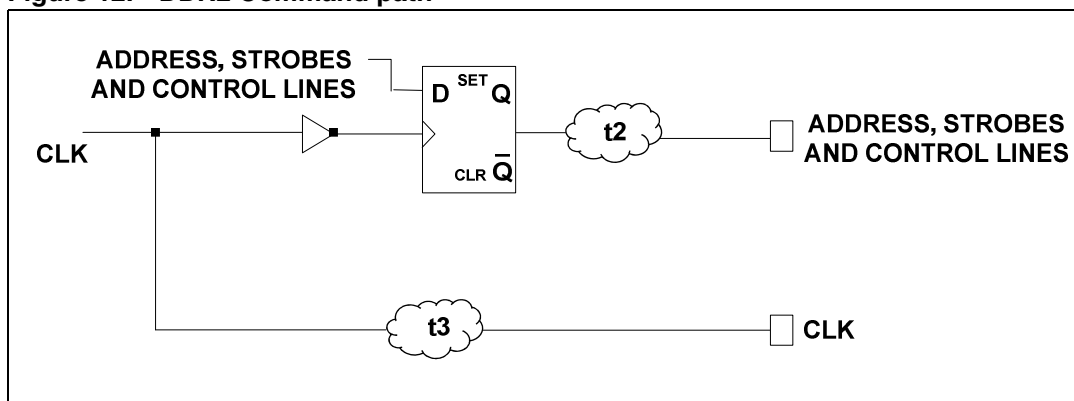


Table 28. DDR2 Command timings

| Frequency | t4 max | t5 max | Unit |
|-----------|--------|--------|------|
| 333 MHz   | 1.39   | 1.40   | ns   |
| 266 MHz   | 1.77   | 1.78   | ns   |
| 200 MHz   | 2.39   | 2.40   | ns   |
| 166 MHz   | 2.90   | 2.91   | ns   |
| 133 MHz   | 3.65   | 3.66   | ns   |

## 6.2 CLCD timing characteristics

The characterization timing is done considering an output load of 10 pF on all the outputs. The operating conditions are in worst case  $V=0.90\text{ V}$   $T=125\text{ }^\circ\text{C}$  and in best case  $V=1.10\text{ V}$   $T=40\text{ }^\circ\text{C}$ .

The CLCD has a wide variety of configurations and setting and the parameters change accordingly. Two main scenarios will be considered, one with direct clock to output (166

MHz), setting BCD bit to '1', and the second one with the clock passing through a clock divider (83 MHz), setting BCD bit to '0'.

### 6.2.1 CLCD timing characteristics direct clock

Figure 13. CLCD waveform with CLCP direct

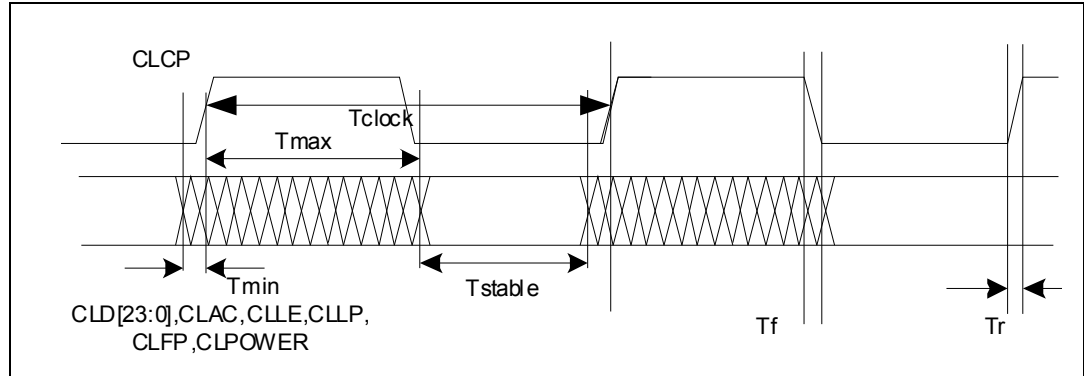


Figure 14. CLCD block diagram with CLCP direct

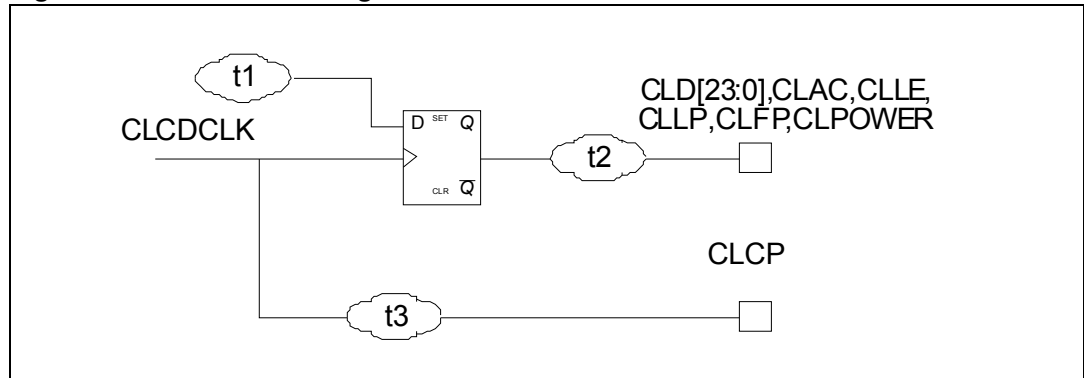


Table 29. CLCD timings with CLCP direct

| Parameter  | Value    | Frequency |
|--|----------|-----------|
| $t_{\text{CLOCK direct max}} (t_{\text{CLOCK}})$ | 6 ns     | 166 MHz   |
| $t_{\text{CLOCK direct max rise}} (t_r)$         | 0.81 ns  |           |
| $t_{\text{CLOCK direct max}} (t_f)$              | 0.87 ns  |           |
| $t_{\text{min}}$                                 | -0.04 ns |           |
| $t_{\text{max}}$                                 | 3.62 ns  |           |
| $t_{\text{STABLE}}$                              | 2.34 ns  |           |

- Note:
- $t_{\text{STABLE}} = t_{\text{CLOCK direct max}} - (t_{\text{max}} + t_{\text{min}})$
  - For  $t_{\text{max}}$  the maximum value is taken from the worst case and best case, while for  $t_{\text{min}}$  the minimum value is taken from the worst case and best case.
  - CLCP should be delayed by  $\{t_{\text{max}} + [t_{\text{CLOCK direct max}} - (t_{\text{max}} + t_{\text{min}})]/2\} = 4.7915 \text{ ns}$

### 6.2.2 CLCD timing characteristics divided clock

Figure 15. CLCD waveform with CLCP divided

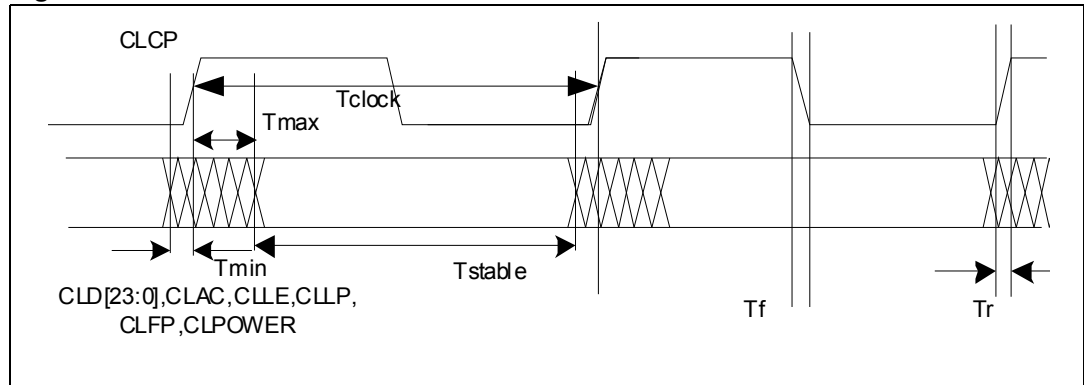


Figure 16. CLCD block diagram with CLCP divided

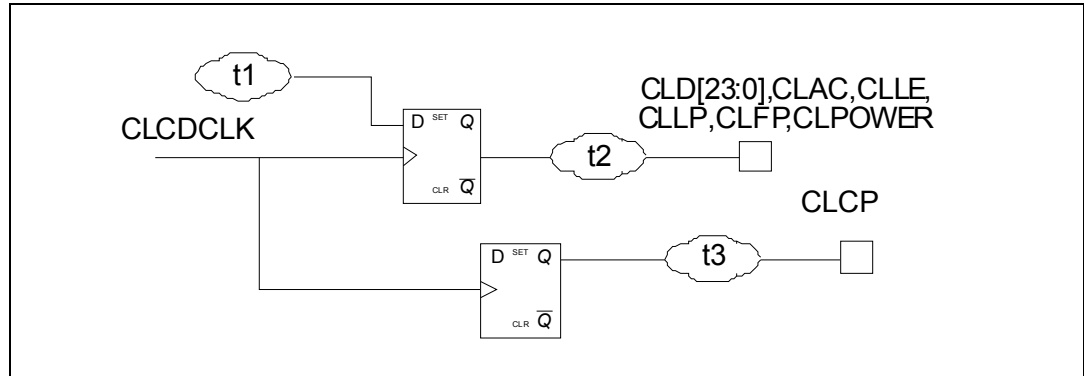


Table 30. CLCD timings with CLCP divided

| Parameter                                     | Value    | Frequency |
|---|----------|-----------|
| $t_{\text{CLOCK}}$ divided max                | 12 ns    | 83.3 MHz  |
| $t_{\text{CLOCK}}$ divided max rise ( $t_r$ ) | 0.81 ns  |           |
| $t_{\text{CLOCK}}$ divided max ( $t_f$ )      | 0.87 ns  |           |
| $t_{\text{min}}$                              | -0.49 ns |           |
| $t_{\text{max}}$                              | 2.38 ns  |           |
| $t_{\text{STABLE}}$                           | 9.13 ns  |           |

- Note:
- $t_{\text{STABLE}} = t_{\text{CLOCK direct max}} - (t_{\text{max}} + t_{\text{min}})$
  - For  $t_{\text{max}}$  the maximum value is taken from the worst case and for  $t_{\text{min}}$  the minimum value is taken from the best case.
  - CLCP should be delayed by  $\{t_{\text{max}} + [t_{\text{CLOCK direct max}} - (t_{\text{max}} + t_{\text{min}})]/2\} = 6.945 \text{ ns}$

### 6.3 I<sup>2</sup>C timing characteristics

The characterization timing is done considering an output load of 10 pF on SCL and SDA. The operating conditions are V = 0.90 V, T<sub>A</sub>=125° C in worst case and V =1.10 V, T<sub>A</sub>= 40° C in best case.

Figure 17. I<sup>2</sup>C output pins

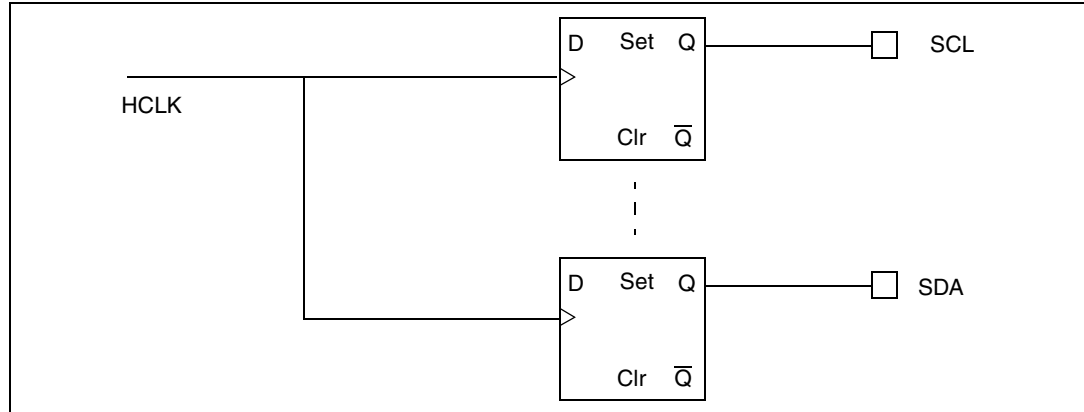
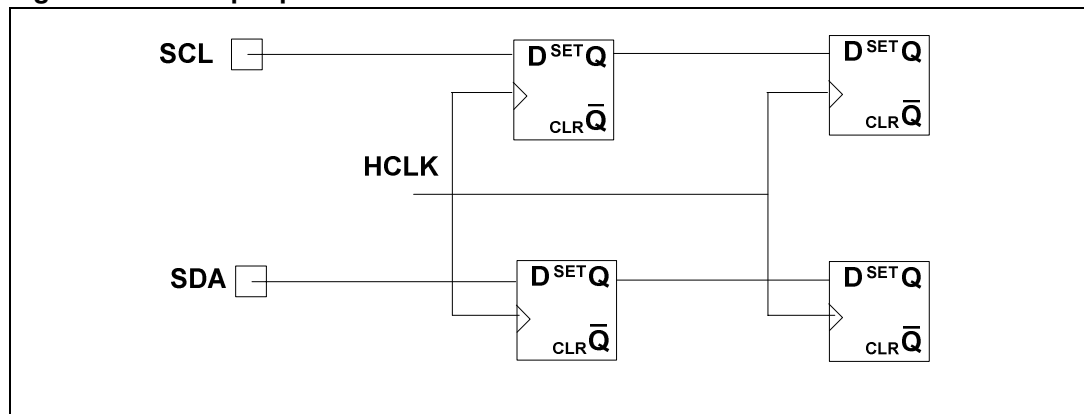


Figure 18. I<sup>2</sup>C input pins



The flip-flops used to capture the incoming signals are re-synchronized with the AHB clock (HCLK): so, no input delay calculation is required.

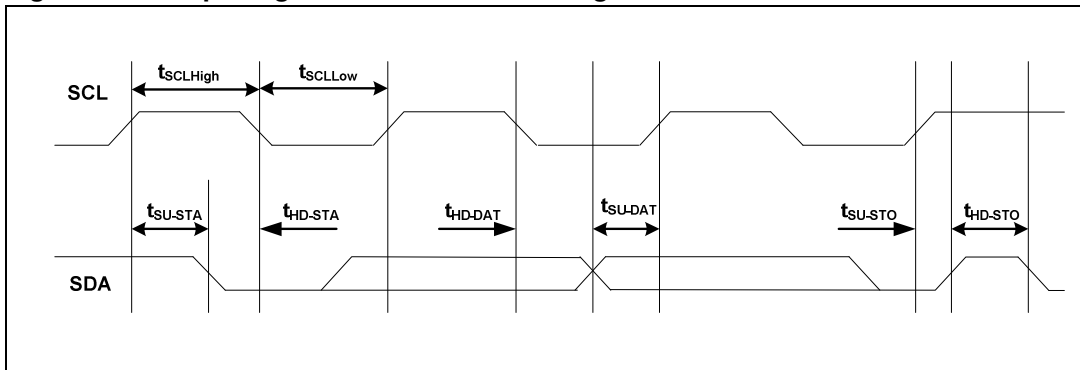
Table 31. Output delays for I<sup>2</sup>C signals

| Parameter                  | Min    | Max     | Unit |
|----------------------------|--------|---------|------|
| t <sub>HCLK-&gt;SCLH</sub> | 8.1067 | 11.8184 | ns   |
| t <sub>HCLK-&gt;SCLL</sub> | 7.9874 | 12.6269 | ns   |
| t <sub>HCLK-&gt;SDAH</sub> | 7.5274 | 11.2453 | ns   |
| t <sub>HCLK-&gt;SDAL</sub> | 7.4081 | 12.0530 | ns   |

Those values are referred to the common internal source clock which has a period of:

t<sub>HCLK</sub> = 6 ns.

Figure 19. Output signal waveforms for I<sup>2</sup>C signals



The timing of high and low level of SCL ( $t_{SCLHigh}$  and  $t_{SCLLow}$ ) are programmable.

Table 32. Time characteristics for I<sup>2</sup>C in high-speed mode

| Parameter    | Min       | Unit |
|--------------|-----------|------|
| $t_{SU-STA}$ | 157.5897  | ns   |
| $t_{HD-STA}$ | 325.9344  |      |
| $t_{SU-DAT}$ | 314.0537  |      |
| $t_{HD-DAT}$ | 0.7812    |      |
| $t_{SU-STO}$ | 637.709   |      |
| $t_{HD-STO}$ | 4742.1628 |      |

Table 33. Time characteristics for I<sup>2</sup>C in fast speed mode

| Parameter    | Min       | Unit |
|--------------|-----------|------|
| $t_{SU-STA}$ | 637.5897  | ns   |
| $t_{HD-STA}$ | 602.169   |      |
| $t_{SU-DAT}$ | 1286.0537 |      |
| $t_{HD-DAT}$ | 0.7812    |      |
| $t_{SU-STO}$ | 637.709   |      |
| $t_{HD-STO}$ | 4742.1628 |      |

Table 34. Time characteristics for I<sup>2</sup>C in standard speed mode

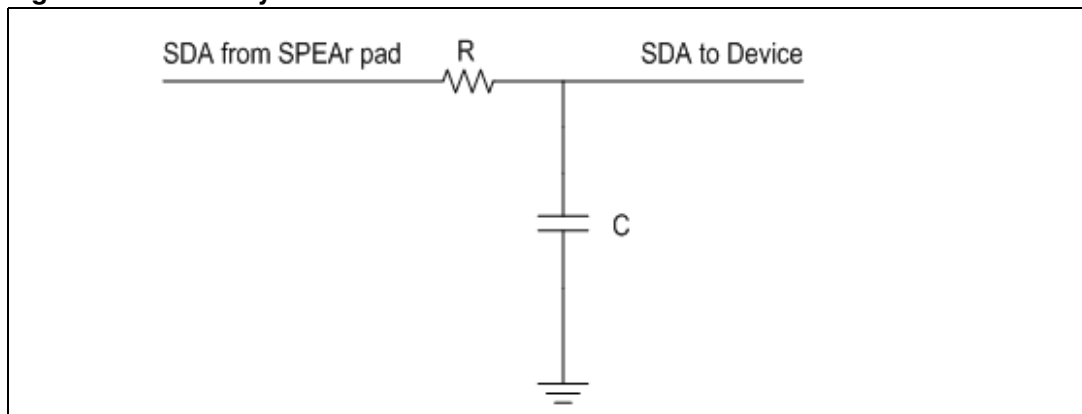
| Parameter    | Min       | Unit |
|--------------|-----------|------|
| $t_{SU-STA}$ | 4723.5897 | ns   |
| $t_{HD-STA}$ | 3991.9344 |      |
| $t_{SU-DAT}$ | 4676.0537 |      |
| $t_{HD-DAT}$ | 0.7812    |      |
| $t_{SU-STO}$ | 4027.709  |      |
| $t_{HD-STO}$ | 4742.1628 |      |

Note: 1 The timings shown in [Figure 19](#) depend on the programmed value of  $T_{SCLHigh}$  and  $T_{SCLLow}$ , so the values present in the three tables here above have been calculated using the minimum programmable values of :

$IC_{HS\_SCL\_HCNT}=19$  and  $IC_{HS\_SCL\_LCNT}=53$  registers (for High-Speed mode);  
 $IC_{FS\_SCL\_HCNT}=99$  and  $IC_{FS\_SCL\_LCNT}=215$  registers (for Fast-Speed mode);  
 $IC_{SS\_SCL\_HCNT}=664$  and  $IC_{SS\_SCL\_LCNT}=780$  registers (for Standard-Speed mode).

- Note: 1 These minimum values depend on the AHB clock (HCLK) frequency, which is 166 MHz.
- 2 A device may internally require a hold time of at least 300 ns for the SDA signal (referred to the  $V_{IHmin}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL (Please refer to the I<sup>2</sup>C Bus Specification v3-0 Jun 2007). However, the SDA data hold time in the I<sup>2</sup>C controller of SPEAr300 is one-clock cycle based (6 ns with the HCLK clock at 166 MHz). This time may be insufficient for some slave devices. A few slave devices may not receive the valid address due to the lack of SDA hold time and will not acknowledge even if the address is valid. If the SDA data hold time is insufficient, an error may occur.
- 3 **Workaround:** If a device needs more SDA data hold time than one clock cycle, an RC delay circuit is needed on the SDA line as illustrated in the following figure:

Figure 20. RC delay circuit



For example,  $R=K$  and  $C=200\text{ pF}$ .

## 6.4 FSMC timing characteristics

The characterization timing is done considering an output load of 3 pF on the data, 15 pF on NF\_CE, NF\_RE and NF\_WE and 10 pF on NF\_ALE and NF\_CLE.

The operating conditions are  $V=0.90\text{ V}$ ,  $T=125\text{ °C}$  in worst case and  $V=1.10\text{ V}$ ,  $T=40\text{ °C}$  in best case.



### 6.4.1 8-bit NAND Flash configuration

Figure 21. Output pads for 8-bit NAND Flash configuration

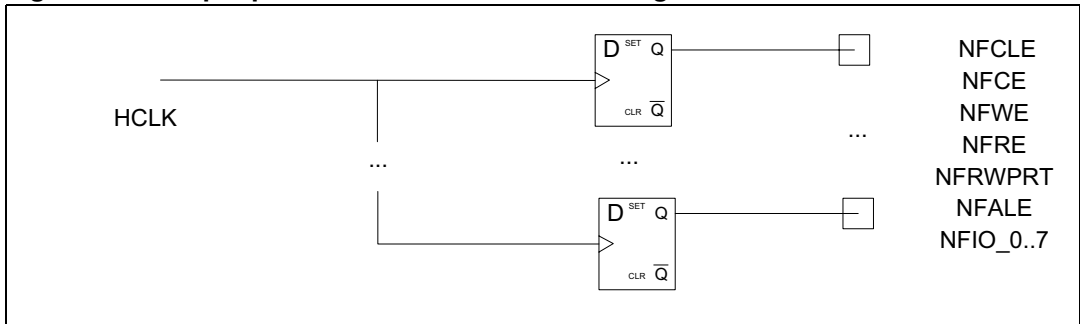


Figure 22. Input pads for 8-bit NAND Flash configuration

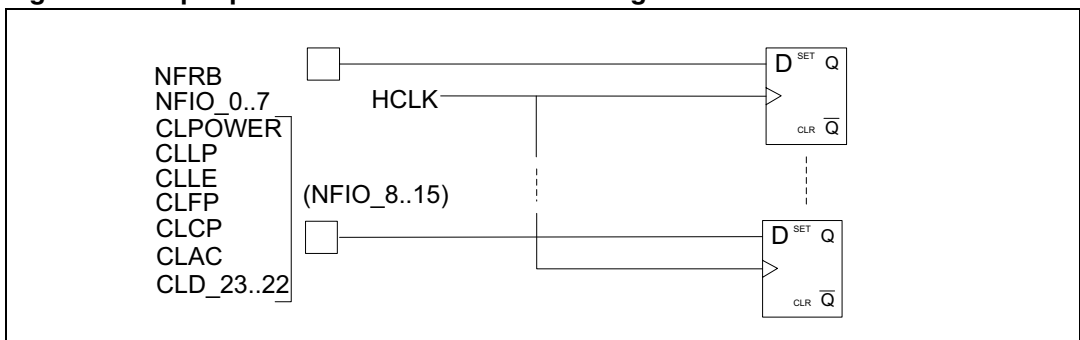


Figure 23. Output command signal waveforms for 8-bit NAND Flash configuration

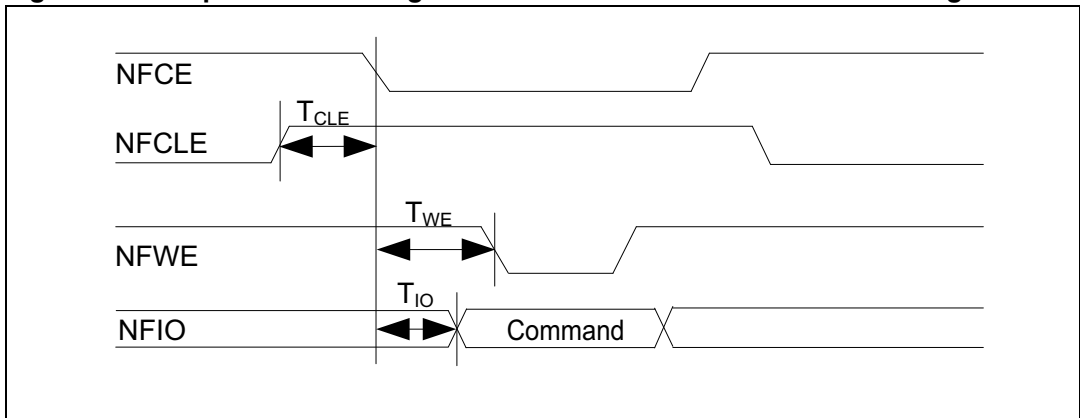


Figure 24. Output address signal waveforms for 8-bit NAND Flash configuration

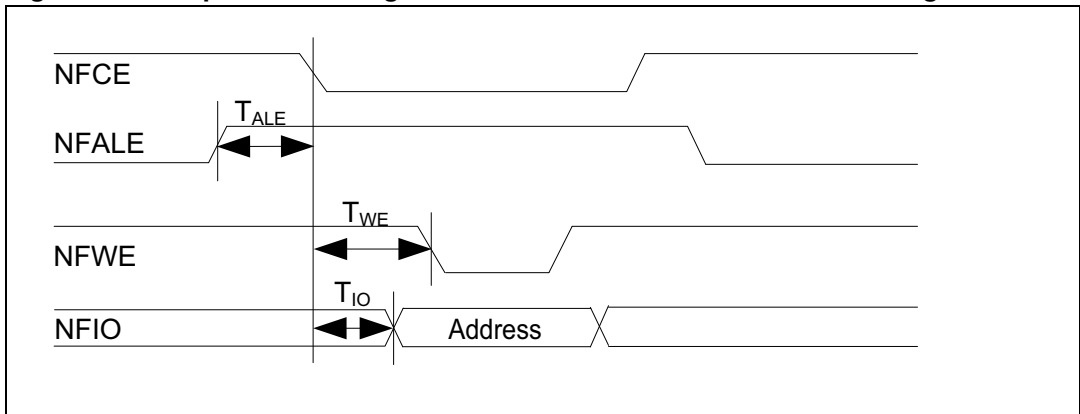


Figure 25. In/out data address signal waveforms for 8-bit NAND Flash configuration

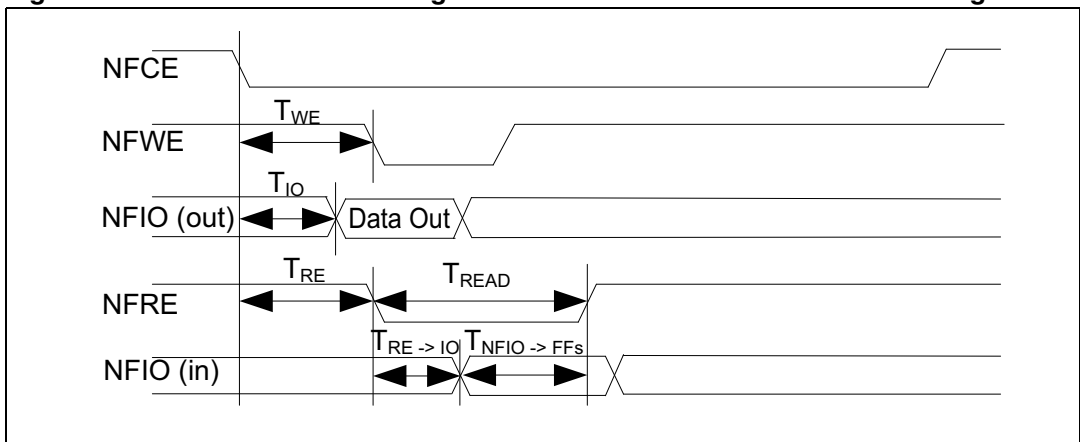


Table 35. Time characteristics for 8-bit NAND Flash configuration

| Parameter | Min       | Max       |
|-----------|-----------|-----------|
| TCLE      | -16.85 ns | -19.38 ns |
| TALE      | -16.84 ns | -19.37 ns |
| TWE (s=1) | 11.10 ns  | 13.04 ns  |
| TRE (s=1) | 11.18 ns  | 13.05 ns  |
| TIO (h=1) | 3.43 ns   | 8.86 ns   |

Note: Values in [Table 35](#) are referred to the common internal source clock which has a period of  $T_{HCLK} = 6 \text{ ns}$ .

### 6.4.2 16-bit NAND Flash configuration

Figure 26. Output pads for 16-bit NAND Flash configuration

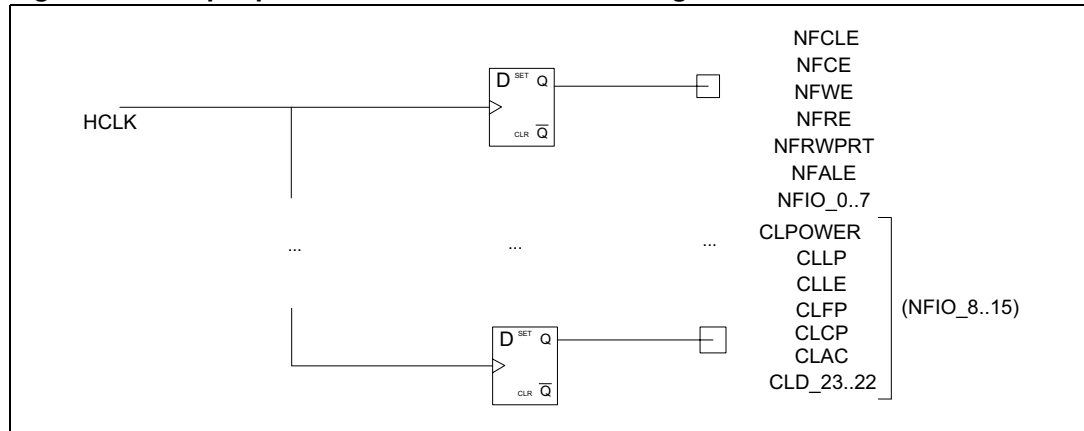


Figure 27. Input pads for 16-bit NAND Flash configuration

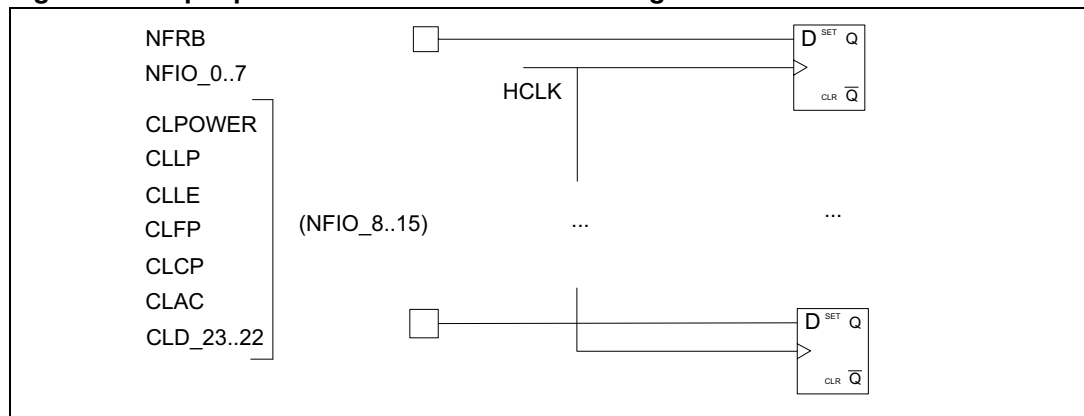


Figure 28. Output command signal waveforms 16-bit NAND Flash configuration

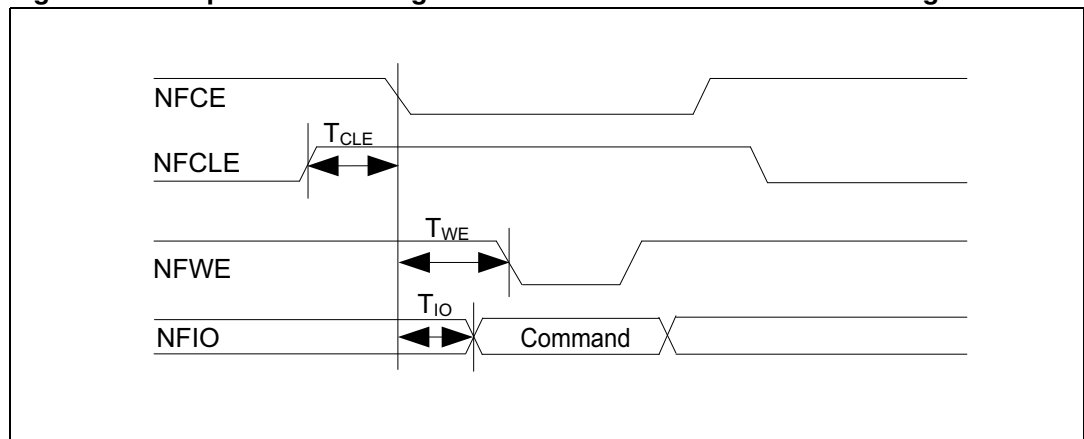


Figure 29. Output address signal waveforms 16-bit NAND Flash configuration

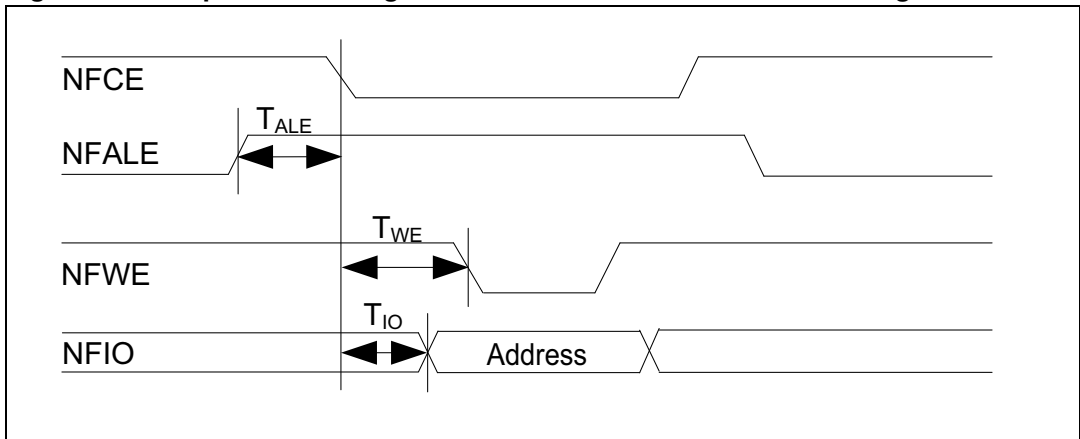


Figure 30. In/out data signal waveforms for 16-bit NAND Flash configuration

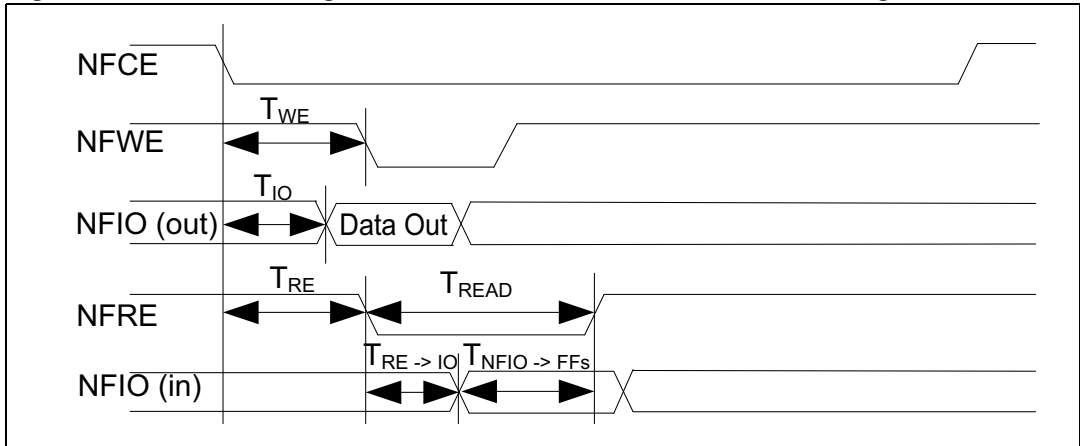


Table 36. Time characteristics for 16-bit NAND Flash configuration

| Parameter | Min       | Max       |
|-----------|-----------|-----------|
| TCLE      | -16.85 ns | -19.38 ns |
| TALE      | -16.84 ns | -19.37 ns |
| TWE (s=1) | 11.10 ns  | 13.04 ns  |
| TRE (s=1) | 11.18 ns  | 13.05 ns  |
| TIO (h=1) | 3.27 ns   | 11.35 ns  |

Note: Values in [Table 36](#) are referred to the common internal source clock which has a period of  $T_{HCLK} = 6 \text{ ns}$ .

## 6.5 Ether MAC 10/100 Mbps timing characteristics

The characterization timing is given for an output load of 5 pF on the MII TX clock and 10 pF on the other pads. The operating conditions are in worst case V=0.90 V T=125° C and in best case V=1.10 V T= 40° C.

### 6.5.1 MII transmit timing specifications

Figure 31. MII TX waveforms

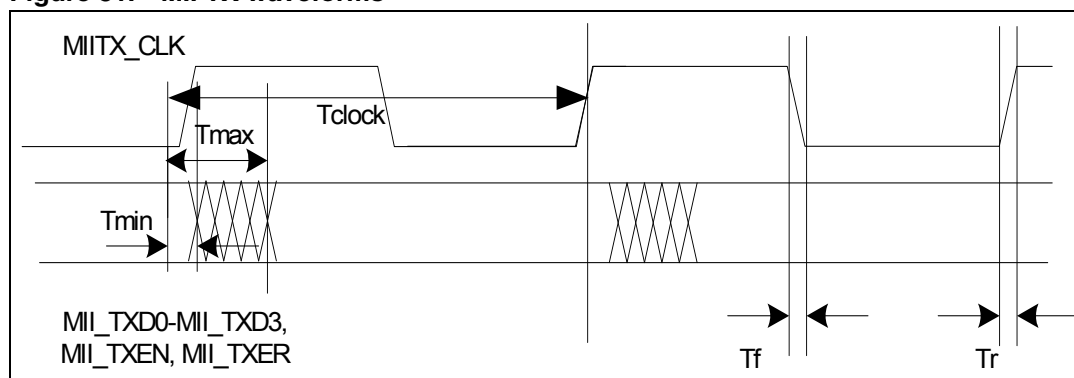


Figure 32. Block diagram of MII TX pins

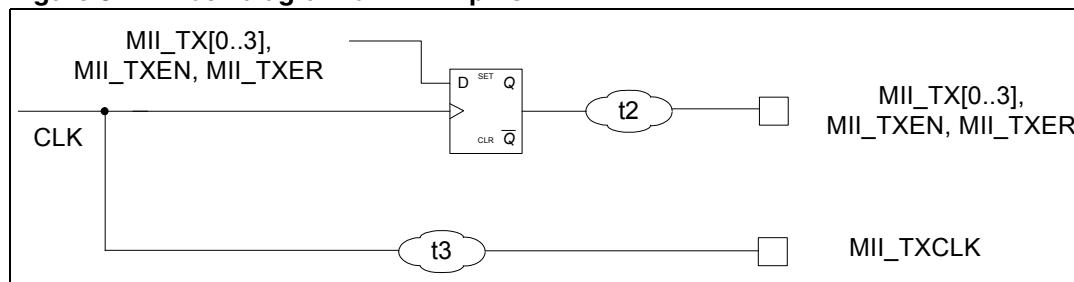


Table 37. MII TX timings

| Parameter                       | Value using MII 10 Mb [ $t_{CLK}$ period = 40 ns 25 MHz] | Value using MII 100 Mb [ $t_{CLK}$ period = 400 ns 2.5 MHz] |
|---------------------------------|--|---|
| $t_{max} = t2_{max} - t3_{min}$ | 6.8 ns   | 6.8 ns  |
| $t_{min} = t2_{min} - t3_{max}$ | 2.9 ns   | 2.9 ns  |
| $t_{SETUP}$                     | 33.2 ns  | 393.2 ns  |

Note: To calculate the  $t_{SETUP}$  value for the PHY you have to consider the next  $t_{CLK}$  rising edge, so you have to apply the following formula:  $t_{SETUP} = t_{CLK} - t_{max}$

### 6.5.2 MII receive timing specifications

Figure 33. MII RX waveforms

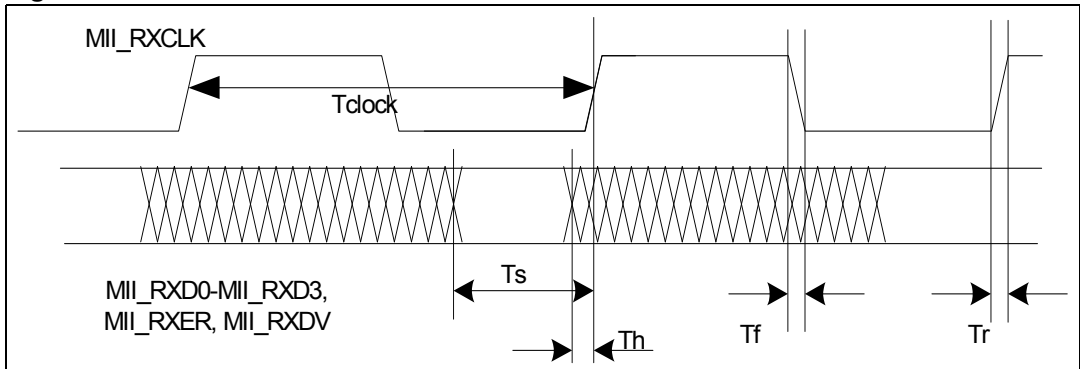
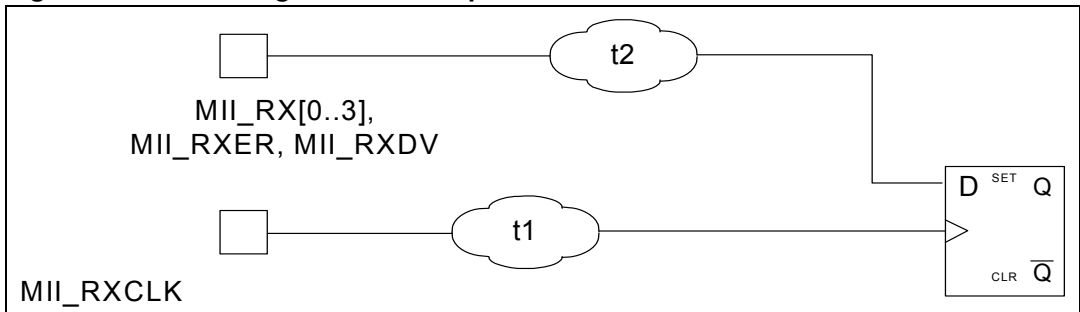


Figure 34. Block diagram of MII RX pins



### 6.5.3 MDIO timing specifications

Figure 35. MDC waveforms

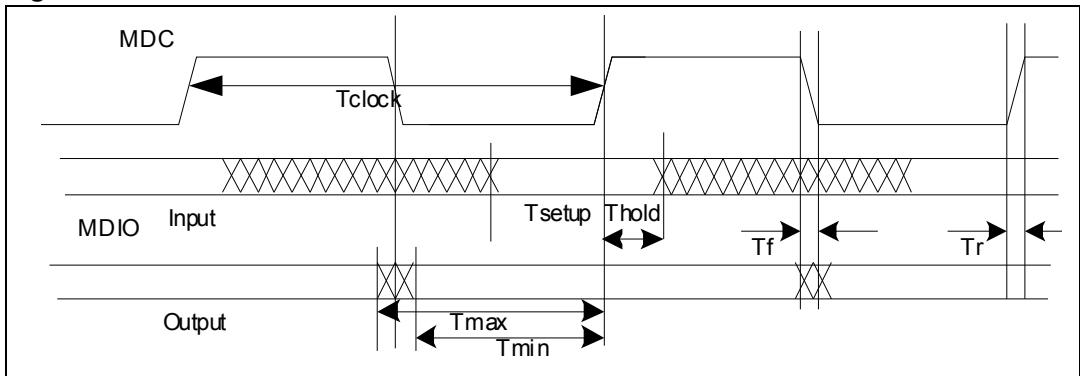


Figure 36. Paths from MDC/MDIO pads

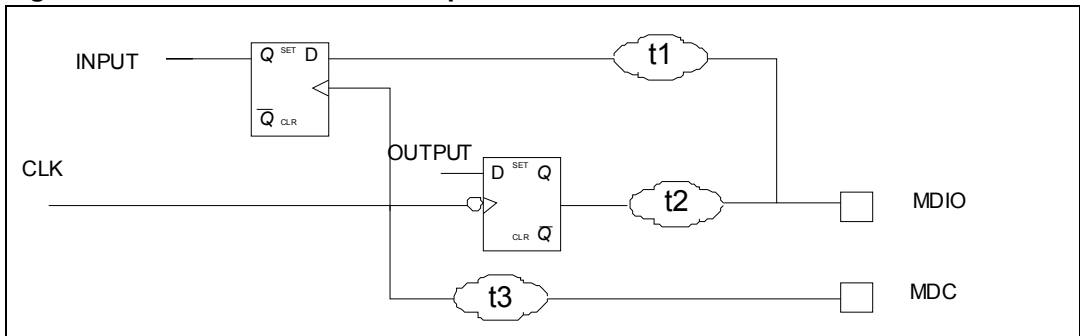


Table 38. MDC/MDIO timing

| Parameter                            | Value    | Frequency |
|--------------------------------------|----------|-----------|
| $t_{CLK}$ period                     | 614.4 ns | 1.63 MHz  |
| $t_{CLK}$ fall ( $t_f$ )             | 1.18 ns  |           |
| $t_{CLK}$ rise ( $t_r$ )             | 1.14 ns  |           |
| <b>Output</b>                        |          |           |
| $t_{max} = \sim t_{CLK} / 2$         | 307 ns   |           |
| $t_{min} = \sim t_{CLK} / 2$         | 307 ns   |           |
| <b>Input</b>                         |          |           |
| $t_{SETUPmax} = t1_{max} - t3_{min}$ | 6.88 ns  |           |
| $t_{HOLDmin} = t1_{min} - t3_{max}$  | -1.54 ns |           |

Note: When MDIO is used as output the data are launched on the falling edge of the clock as shown in Figure 35.

### 6.6 SMI - Serial memory interface

Figure 37. SMIDATAIN data path

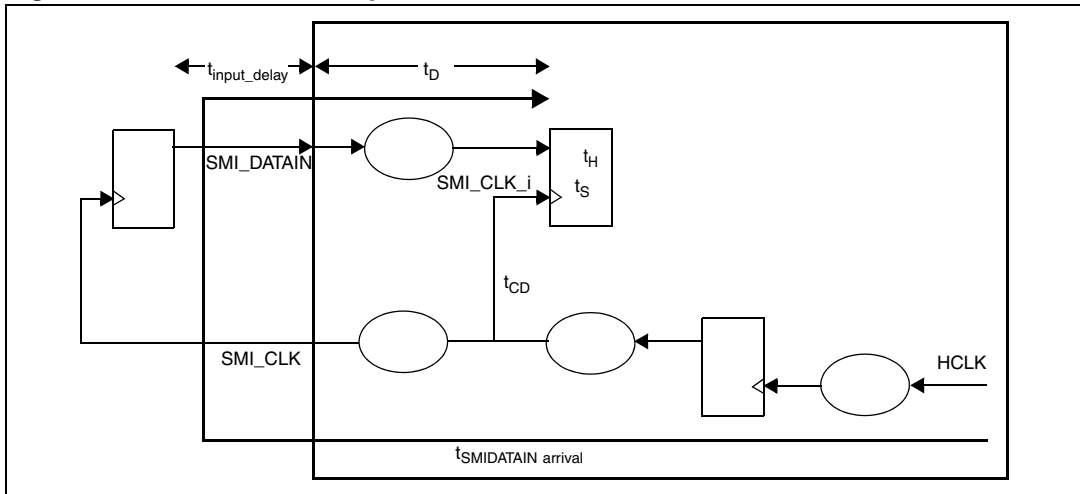


Table 39. SMIDATAIN timings

| Signal     | Parameter        | Value  |
|------------|------------------|--|
| SMI_DATAIN | $t_{d\_max}$     | $t_{SMIDATAIN\_arrival\_max} - t_{input\_delay}$ |
|            | $t_{d\_min}$     | $t_{SMIDATAIN\_arrival\_min} - t_{input\_delay}$ |
|            | $t_{cd\_min}$    | $t_{SMI\_CLK\_i\_arrival\_min}$                  |
|            | $t_{cd\_max}$    | $t_{SMI\_CLK\_i\_arrival\_max}$                  |
|            | $t_{SETUP\_max}$ | $t_s + t_{d\_max} - t_{cd\_min}$                 |
|            | $t_{HOLD\_min}$  | $t_h - t_{d\_min} + t_{cd\_max}$                 |

Figure 38. SMIDATAOUT/SMICSn data paths

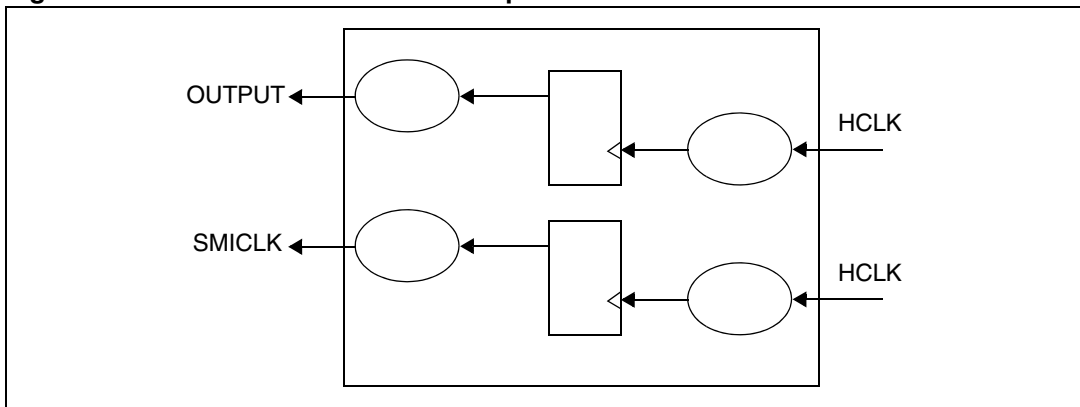




Figure 39. SMIDATAOUT timings

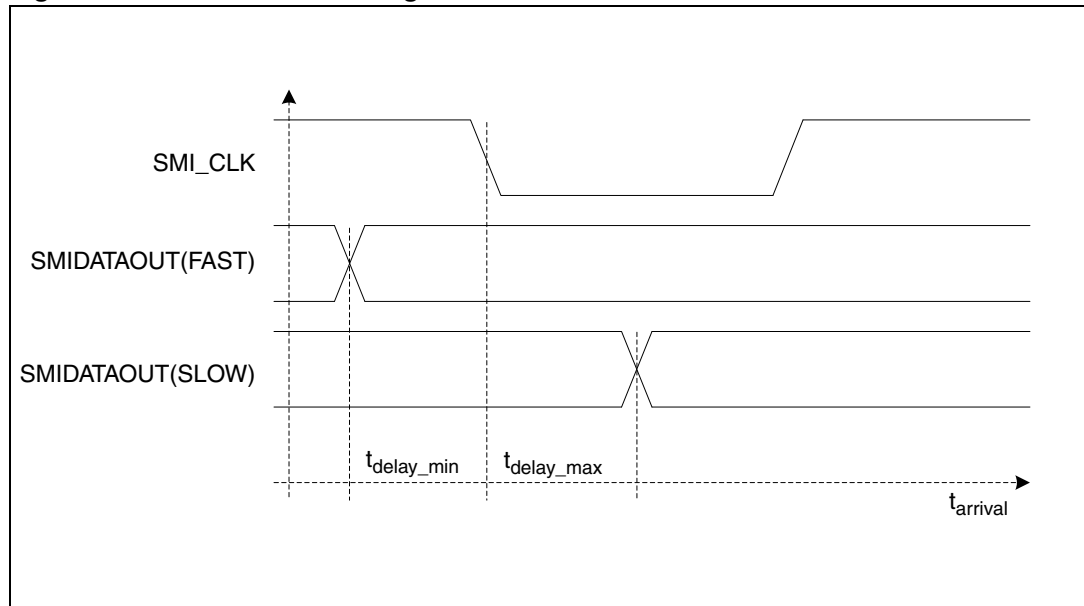


Table 40. SMIDATAIN timings

| Signal      | Parameter        | Value   |
|-------------|------------------|---|
| SMI_DATAOUT | $t_{delay\_max}$ | $t_{arrivalSMIDATAOUT\_max} - t_{arrival\_SMI\_CLK\_min}$ |
|             | $t_{delay\_min}$ | $t_{arrivalSMIDATAOUT\_min} - t_{arrival\_SMI\_CLK\_max}$ |

Figure 40. SMICSn fall timings

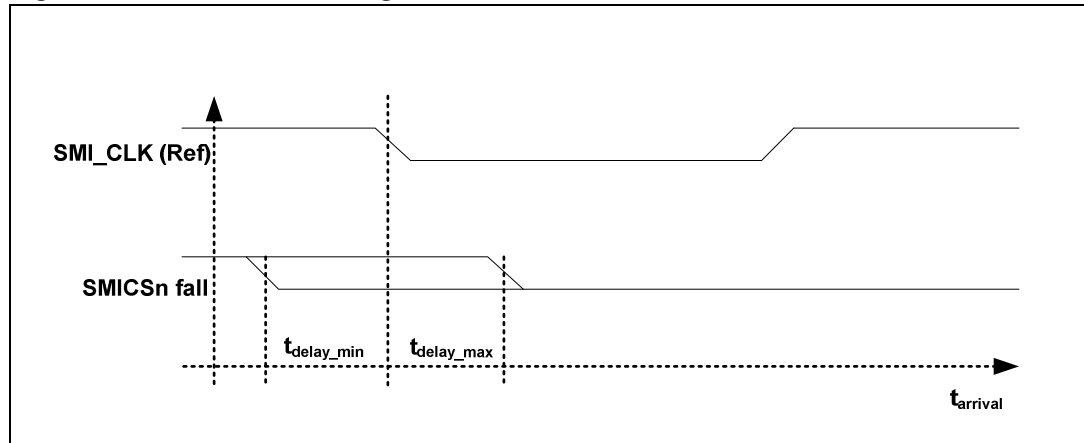


Table 41. SMICSn fall timings

| Signal                   | Parameter        | Value   |
|--------------------------|------------------|---|
| SMI_CS <sub>n</sub> fall | $t_{delay\_max}$ | $t_{arrivalSMICSn\_max\_fall} - t_{arrival\_SMI\_CLK\_min\_fall}$ |
|                          | $t_{delay\_min}$ | $t_{arrivalSMICSn\_min\_fall} - t_{arrival\_SMI\_CLK\_max\_fall}$ |

Figure 41. SMICSn rise timings

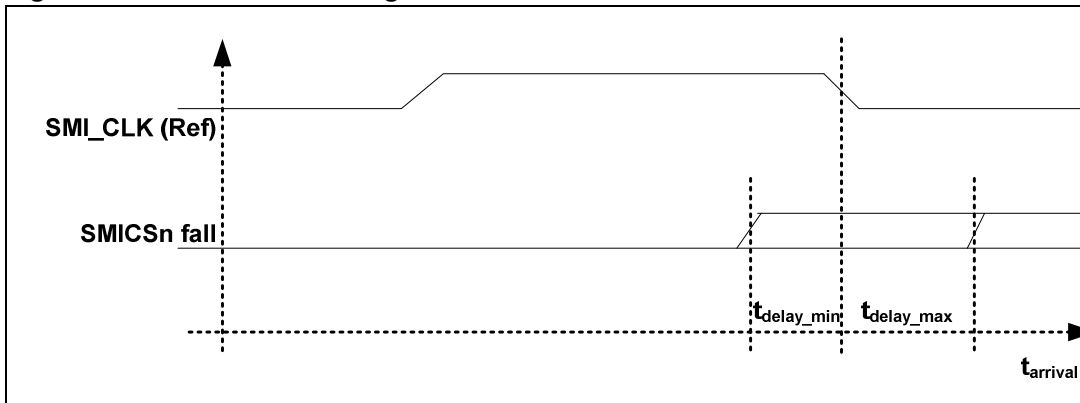


Table 42. SMICSn rise timings

| Signal                   | Parameter        | Value   |
|--------------------------|------------------|---|
| SMI_CS <sub>n</sub> rise | $t_{delay\_max}$ | $t_{arrivalSMICSn\_max\_rise} - t_{arrival\_SMI\_CLK\_min\_fall}$ |
|                          | $t_{delay\_min}$ | $t_{arrivalSMICSn\_min\_rise} - t_{arrival\_SMI\_CLK\_max\_fall}$ |

Table 43. Timing requirements for SMI

| Parameter                    |                  | Input setup-hold/output delay |      |      |
|------------------------------|------------------|-------------------------------|------|------|
|                              |                  | Max                           | Min  | Unit |
| SMI_CLK                      | Fall time        | 1.82                          | 1.40 | ns   |
|                              | Rise time        | 1.63                          | 1.19 |      |
| SMIDATAIN                    | Input setup time | 8.27                          |      |      |
|                              | Input hold time  | -2.59                         |      |      |
| SMIDATAOUT Output valid time |                  | 2.03                          |      |      |
| SMICS_0 Output valid time    | fall             | 1.92                          |      |      |
|                              | rise             | 1.69                          |      |      |
| SMICS_1 Output valid time    | fall             | 1.78                          |      |      |
|                              | rise             | 1.63                          |      |      |

## 6.7 SSP timing characteristics

This module provides a programmable length shift register which allows serial communication with other SSP devices through a 3 or 4 wire interface (SSP\_CLK, SSP\_MISO, SSP\_MOSI and SSP\_CS<sub>n</sub>). The SSP supports the following features:

- Master/Slave mode operations
- Chip-selects for interfacing to multiple slave SPI devices.
- 3 or 4 wire interface (SSP\_SCK, SSP\_MISO, SSP\_MOSI and SSP\_CS<sub>n</sub>)
- Single interrupt
- Separate DMA events for SPI Receive and Transmit
- 16-bit shift register
- Receive buffer register
- Programmable character length (2 to 16 bits)
- Programmable SSP clock frequency range
- 8-bit clock pre-scaler
- Programmable clock phase (delay or no delay)
- Programmable clock polarity

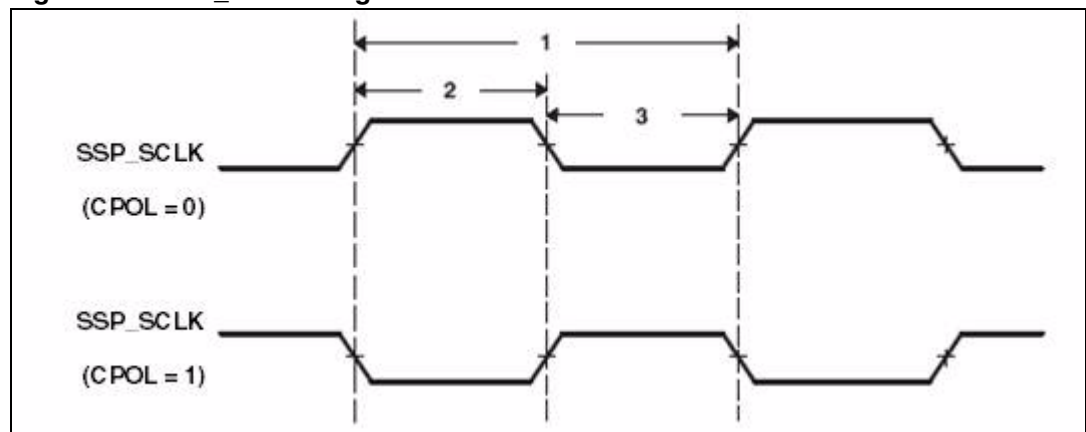
*Note:* The following tables and figures show the characterization of the SSP using the SPI protocol.

**Table 44. Timing requirements for SSP (all modes)**

| No. | Parameters    |                              | Value         | Unit |
|-----|---------------|------------------------------|---------------|------|
| 1   | $T_{c(CLK)}$  | Cycle time, SSP_CLK          | 24            | ns   |
| 2   | $T_{w(CLKH)}$ | Pulse duration, SSP_CLK high | 0.49T - 0.51T | ns   |
| 3   | $T_{w(CLKL)}$ | Pulse duration, SSP_CLK low  | 0.51T - 0.49T | ns   |

T = T<sub>c</sub>(CLK) = SSP\_CLK period is equal to the SSP module master clock divided by a configurable divider.

**Figure 42. SSP\_CLK timings**



## 6.7.1 SPI master mode timings (clock phase = 0)

Table 45. Timing requirements for SPI master mode (clock phase = 0)

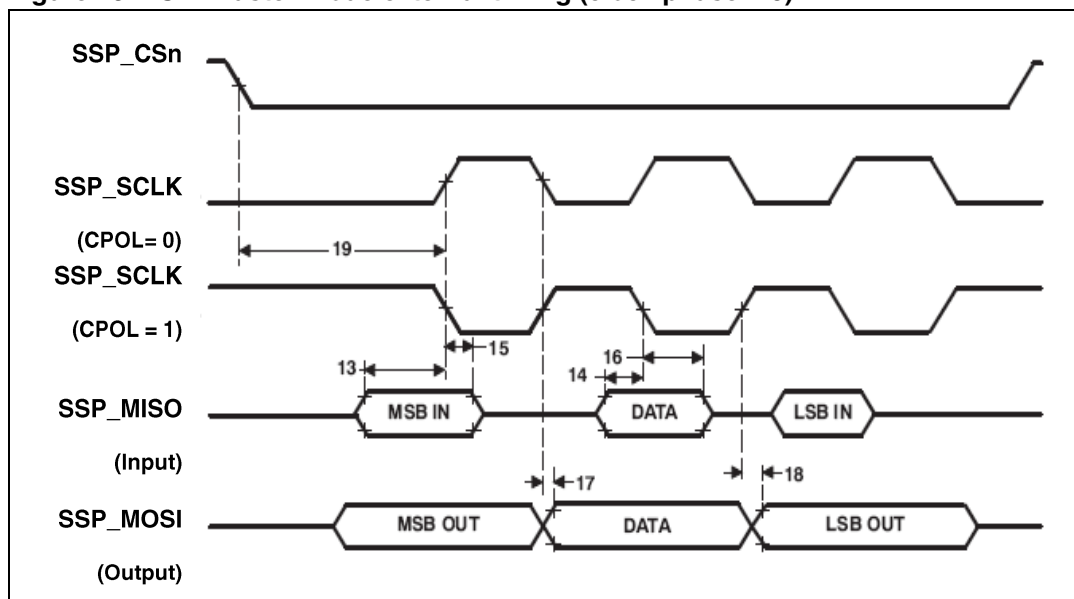
| No. | Parameters         |   | Min    | Max    | Unit |
|-----|--------------------|---|--------|--------|------|
| 13  | $t_{su(DIV-CLKL)}$ | Setup time, MISO (input) valid before SSP_CLK (output) rising edge  | -0.411 | -0.342 | ns   |
| 14  | $t_{su(DIV-CLKH)}$ | Setup time, MISO (input) valid before SSP_CLK (output) falling edge | -0.411 | -0.342 | ns   |
| 15  | $t_{h(CLKL-DIV)}$  | Hold time, MISO (input) valid after SSP_CLK (output) rising edge    | 0.912  | 1.720  | ns   |
| 16  | $t_{h(CLKH-DIV)}$  | Hold time, MISO (input) valid after SSP_CLK (output) falling edge   | 0.912  | 1.720  | ns   |

$P = 1/SSP\_CLK$  in nanoseconds (ns). For example, if the SSP\_CLK frequency is 83 MHz, use  $P = 12.048$  ns

Table 46. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 0)

| No. | Parameters          |  | Min    | Max   | Unit |
|-----|---------------------|--|--------|-------|------|
| 17  | $t_{d(CLKH-DOV)}$   | Delay time, SSP_CLK (output) falling edge to MOSI (output) transition                                  | -3.138 | 2.175 | ns   |
| 18  | $t_{d(CLKL-DOV)}$   | Delay time, SSP_CLK (output) rising edge to MOSI (output) transition                                   | -3.138 | 2.175 | ns   |
| 19  | $t_{d(ENL-CLKH/L)}$ | Delay time, SSP_CS <sub>n</sub> (output) falling edge to first SSP_CLK (output) rising or falling edge | T/2    |       | ns   |
| 20  | $t_{d(CLKH/L-ENH)}$ | Delay time, SSP_CLK (output) rising or falling edge to SSP_CS <sub>n</sub> (output) rising edge        | T      |       | ns   |

Figure 43. SPI master mode external timing (clock phase = 0)



### 6.7.2 SPI master mode timings (clock phase = 1)

Table 47. Timing requirements for SPI master mode (clock phase = 1)

| No. | Parameters         |   | Min    | Max    | Unit |
|-----|--------------------|---|--------|--------|------|
| 4   | $t_{su(DIV-CLKL)}$ | Setup time, MISO (input) valid before SSP_CLK (output) falling edge | -0.411 | -0.342 | ns   |
| 5   | $t_{su(DIV-CLKH)}$ | Setup time, MISO (input) valid before SSP_CLK (output) rising edge  | -0.411 | -0.342 | ns   |
| 6   | $t_h(CLKL-DIV)$    | Hold time, MISO (input) valid after SSP_CLK (output) falling edge   | 0.912  | 1.720  | ns   |
| 7   | $t_h(CLKH-DIV)$    | Hold time, MISO (input) valid after SSP_CLK (output) rising edge    | 0.912  | 1.720  | ns   |

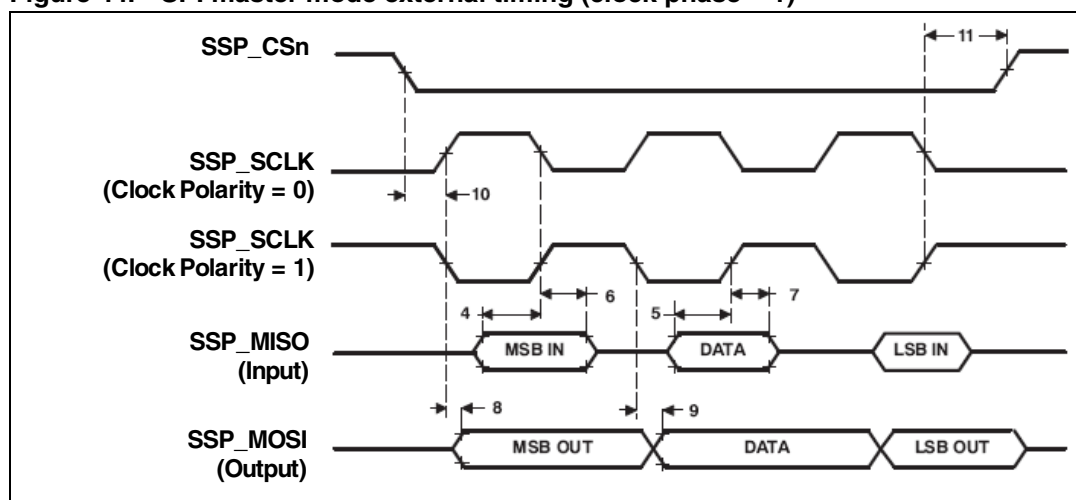
Table 48. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 1)

| No. | Parameters        |   | Min    | Max   | Unit |
|-----|-------------------|---|--------|-------|------|
| 8   | $t_{d(CLKH-DOV)}$ | Delay time, SSP_CLK (output) rising edge to MOSI (output) transition  | -3.138 | 2.175 | ns   |
| 9   | $t_{d(CLKL-DOV)}$ | Delay time, SSP_CLK (output) falling edge to MOSI (output) transition | -3.138 | 2.175 | ns   |

**Table 48. Switching characteristics over recommended operating conditions for SPI master mode (clock phase = 1) (continued)**

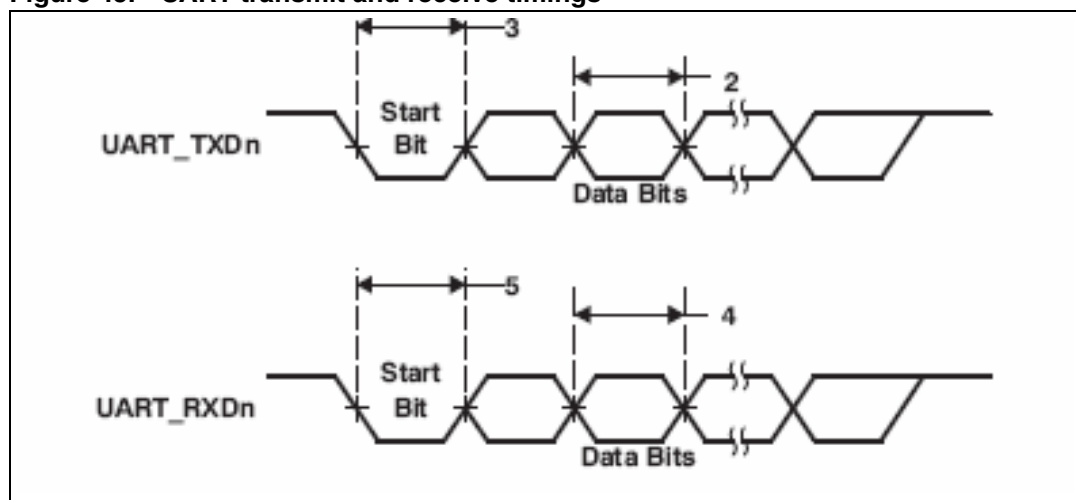
| No. | Parameters          |  | Min | Max | Unit |
|-----|---------------------|--|-----|-----|------|
| 10  | $t_{d(ENL-CLKH/L)}$ | Delay time, SSP_CS <sub>n</sub> (output) falling edge to first SSP_CLK (output) rising or falling edge |     | T   | ns   |
| 11  | $t_{d(CLKH/L-ENH)}$ | Delay time, SSP_CLK (output) rising or falling edge to SSP_CS <sub>n</sub> (output) rising edge        |     | T/2 | ns   |

**Figure 44. SPI master mode external timing (clock phase = 1)**



## 6.8 UART (Universal asynchronous receiver/transmitter)

**Figure 45. UART transmit and receive timings**



**Table 49. UART transmit timing characteristics**

| S.No. | Parameters                              | Min           | Max       | Unit |
|-------|---|---------------|-----------|------|
| 1     | UART Maximum Baud Rate                  |               | 3         | Mbps |
| 2     | UART Pulse Duration Transmit Data (TxD) | $0.99B_{(1)}$ | $B_{(1)}$ | ns   |
| 3     | UART Transmit Start Bit                 | $0.99B_{(1)}$ | $B_{(1)}$ | ns   |

**Table 50. UART receive timing characteristics**

| S.No. | Parameters                             | Min           | Max           | Units |
|-------|--|---------------|---------------|-------|
| 4     | UART Pulse Duration Receive Data (RxD) | $0.97B_{(1)}$ | $1.06B_{(1)}$ | ns    |
| 5     | UART Receive Start Bit                 | $0.97B_{(1)}$ | $1.06B_{(1)}$ | ns    |

where (1) B = UART baud rate

## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**Table 51. LFBGA289 (15 x 15 x 1.7 mm) mechanical data**

| Dim. | mm     |        |        | inches |        |        |
|------|--------|--------|--------|--------|--------|--------|
|      | Min.   | Typ.   | Max.   | Min.   | Typ.   | Max.   |
| A    |        |        | 1.700  |        |        | 0.0669 |
| A1   | 0.270  |        |        | 0.0106 |        |        |
| A2   |        | 0.985  |        |        | 0.0387 |        |
| A3   |        | 0.200  |        |        | 0.0078 |        |
| A4   |        |        | 0.800  |        |        | 0.0315 |
| b    | 0.450  | 0.500  | 0.550  | 0.0177 | 0.0197 | 0.0217 |
| D    | 14.850 | 15.000 | 15.150 | 0.5846 | 0.5906 | 0.5965 |
| D1   |        | 12.800 |        |        | 0.5039 |        |
| E    | 14.850 | 15.000 | 15.150 | 0.5846 | 0.5906 | 0.5965 |
| E1   |        | 12.800 |        |        | 0.5039 |        |
| e    |        | 0.800  |        |        | 0.0315 |        |
| F    |        | 1.100  |        |        | 0.0433 |        |
| ddd  |        |        | 0.200  |        |        | 0.0078 |
| eee  |        |        | 0.150  |        |        | 0.0059 |
| fff  |        |        | 0.080  |        |        | 0.0031 |



Figure 46. LFBGA289 package dimensions

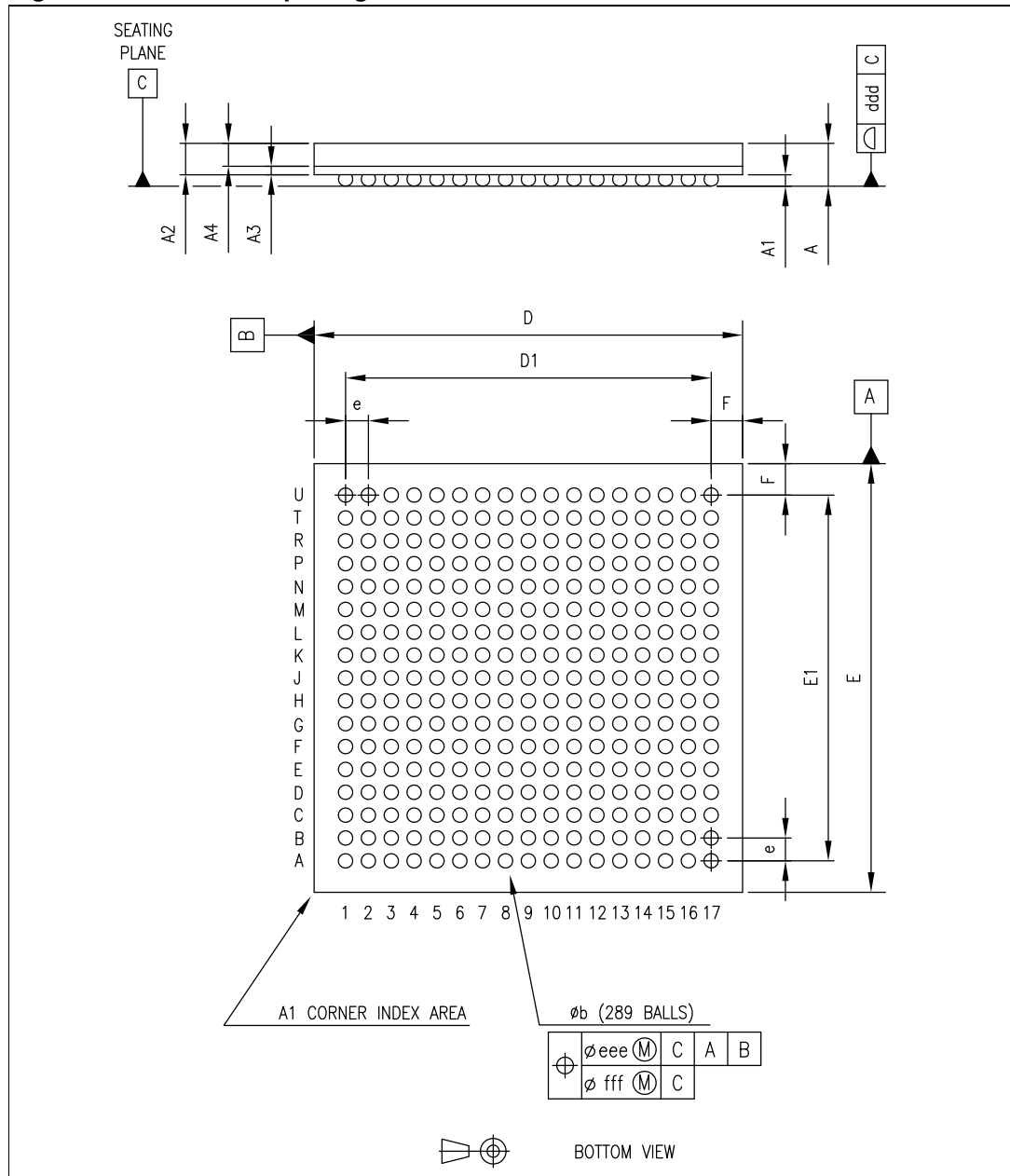


Table 52. Thermal resistance characteristics

| Package  | $\Theta_{JC}$ (°C/W) | $\Theta_{JB}$ (°C/W) |
|----------|----------------------|----------------------|
| LFBGA289 | 18.5                 | 24.5                 |

## 8 Revision history

**Table 53. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 15-Oct-2009 | 1        | Initial release.   |
| 29-Apr-2010 | 2        | Changed the order of chapters in <a href="#">Section 2: Architecture overview</a><br>Updated <a href="#">Section 3.3: Shared I/O pins (PL_GPIOs) on page 35</a><br>Updated number of GPIOs in <a href="#">Table 10 on page 41</a><br>Updated <a href="#">Table 11: PL_GPIO multiplexing scheme on page 42</a><br>Added <a href="#">Section 3.4: PL_GPIO pin sharing for debug modes on page 47</a><br>Updated <a href="#">Section 5: Electrical characteristics</a> , <a href="#">Section 6.1: DDR2 timing characteristics</a> , <a href="#">Section 6.3: I<sup>2</sup>C timing characteristics</a> , <a href="#">Section 6.4: FSMC timing characteristics</a> and <a href="#">Section 6.7: SSP timing characteristics</a><br>Added <a href="#">Table 52: Thermal resistance characteristics</a> in Package information. |

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