CHT-OPA

Revision: 02.00
Apr. 06, 2009

High-Temperature General-Purpose Quad Operational Amplifier

General Description

The CHT-OPA is a general-purpose quad operational amplifier for applications over the temperature range from -55 to 225°C. This circuit is fabricated using a CMOS SOI process, assuring latchup-free operation for all operation conditions.

The CHT-OPA can operate with both single and symmetrical power supplies. The supply voltages range goes from 4.5 to 20V.

Parts are still operational up to 300°C with derated performance (see Typical Performance Characteristics section).

The CHT-OPA uses internal metal lines presenting extremely high immunity to electromigration, improving product lifetime.

Features

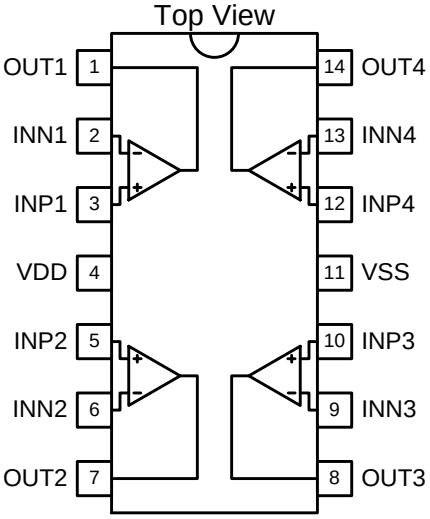
- Qualified from -55 to +225°C (Tj)
- Operational up to +300°C (Tj)
- 4.5 to 20V supply voltages
- Single or symmetrical supply operation
- Latchup-free at any supply and temperature condition
- Available in DIL14 and SOIC16 hermetic ceramic standard packages
- Improved internal metallization for extended reliability

Applications

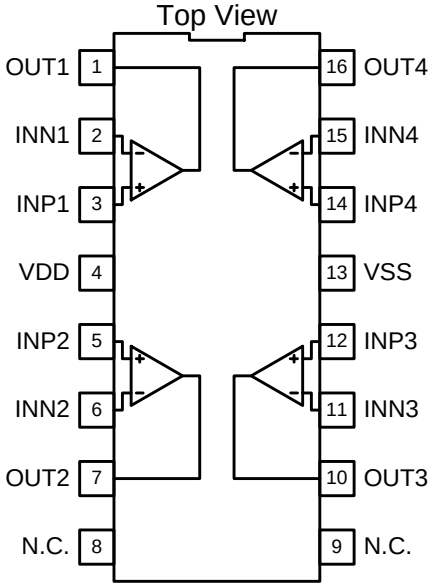
- Well logging, Automotive, Aeronautics & Aerospace
- Harsh Environments

Package Configurations[1]

DIL14
Top View



SOIC16
Top View



[1] Other packages available upon request.

Absolute Maximum Ratings

Supply Voltage VDD to VSS	-0.5 to 25V
Voltage on any Pin to VSS	-0.5 to V_{DD}+0.5V

ESD Rating (expected)

Human Body Model	1kV

Operating Conditions

Supply Voltage VDD to VSS	4.5V to 20V
Junction temperature	-55°C to +225°C

Operation up to +300°C (T_j) can be obtained with some derating on performance.

DC Electrical Characteristics

Unless otherwise stated: VDD=10V, VSS=0V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage **VDD-VSS**		4.5		20	V
Supply current (full package) **Idd**	T_j=25°C			1.7	mA
	T_j=-55 to 225°C			**2.2**	
Output voltage swing **V_O**	RL=2kΩ, THD[1]=1%	0.15		VDD-0.18	V
	RL=∞, THD=0.1%	0.03		VDD-0.02	
Output current[2,3] **I_O**	T_j=-55 to 225°C			**±15**	mA
Common mode input range **V_{CM}**	T_j=225°C	2.0		VDD-0.1	V
	T_j=-55°C	1.5		VDD-0.2	
Input offset voltage[4] **V_{IOFF}**	T_j=25°C		<±2.5	±8	mV
Input offset drift[3] **TC_{VIOFF}**	T_j=25°C		<±5	±15	µV/°C
Input bias current[5] **I_B**	T_j=-55 to 225°C			**±10**	nA
Input offset current[4] **I_{OFF}**	T_j=25°C			±0.01	nA
	T_j=225°C			±10	

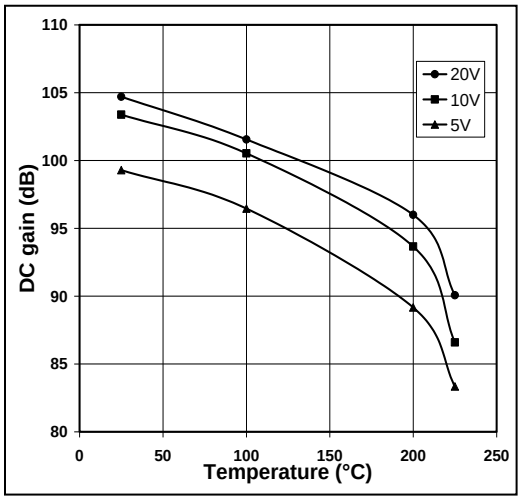
[1] Total Harmonic Distortion.
[2] Source or sink.
[3] Output current is not internally limited. Value given indicate the maximum recommended conditions.
[4] The absolute value of the input offset voltage, $|V_{IOFF}|$, decreases as temperature increases. TC_{VIOFF} must be used so that $|V_{IOFF}|$ decreases with temperature, i.e. TC_{VIOFF} has opposite sign than V_{IOFF}.
[5] Due to ESD structures. Under full characterization.

AC Electrical Characteristics

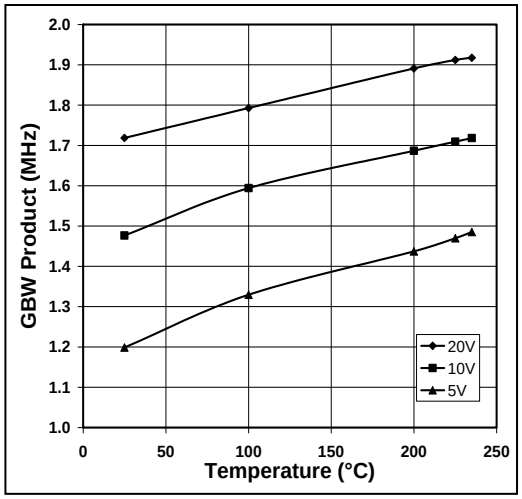
Unless otherwise stated: VDD=10V, VSS=0V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
DC gain **A_o**	RL=2kΩ, T_j=25°C	90	100		dB
	RL=2kΩ, T_j=225°C	80	87		
Gain-bandwidth product **GBW**	RL=2kΩ, CL=30pF	**1.3**	**1.5**		MHz
Common mode rejection ratio **CMRR**	DC to 1kHz	**86**			dB
Power supply rejection ratio **PSRR**	Positive or negative. DC to 100Hz	**78**			dB
Slew rate **SR**	RL=2kΩ, CL=30pF T_j=25°C	1.0	1.2		V/µsec
	RL=2kΩ, CL=30pF T_j=225°C	1.6	1.7		
Phase margin Φ_M	RL=2kΩ, CL=30pF	**50**	**>60**		Degree
Input noise spectral density	F=1Hz		11.0		µV/√Hz
	F=100Hz		1.2		
	F=1kHz		0.43		
	F=10kHz		0.19		
Integrated input noise **e_n**	DC to 10Hz, T_j=-55 to 225°C		25		μV_{RMS}

Typical Performance Characteristics



DC Gain vs. Temperature for V_{DD} = 5/10/20V



GBW vs. Temperature for V_{DD} = 5/10/20V

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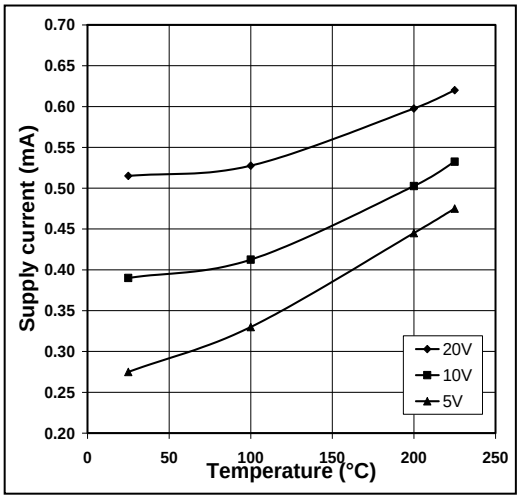
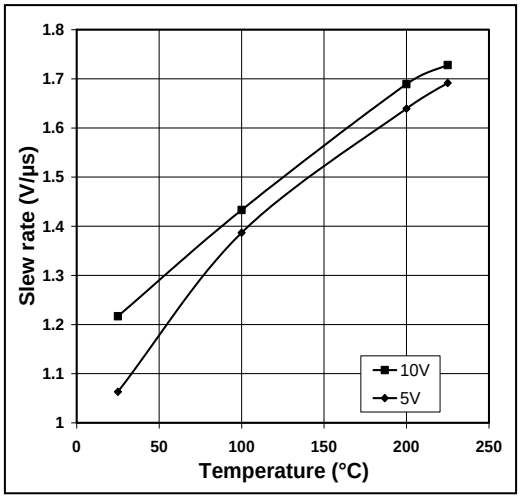
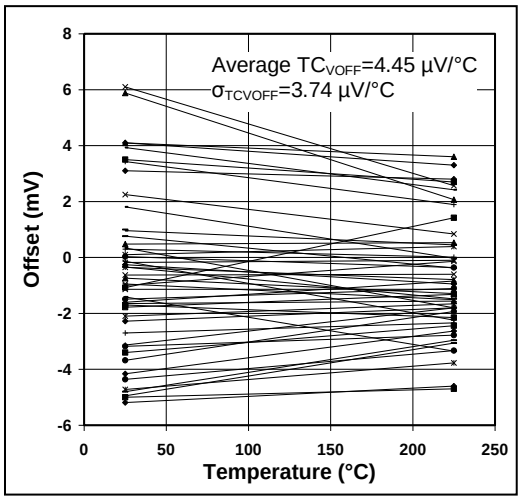


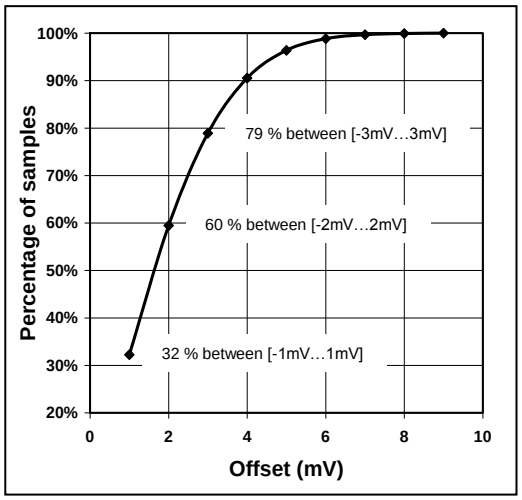
Current consumption per amplifier vs. Temperature for V_{DD} = 5/10/20V



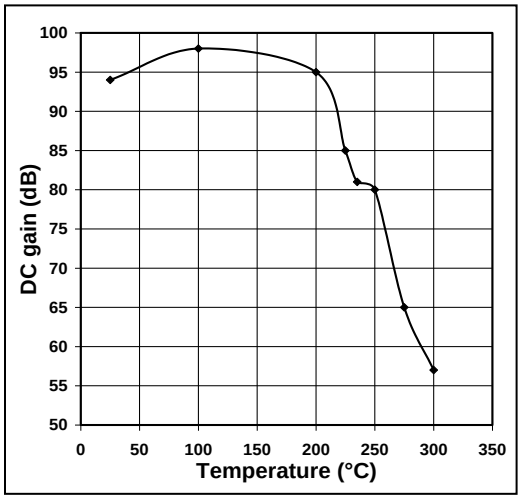
Slew Rate vs. Temperature for V_{DD} = 5/10V



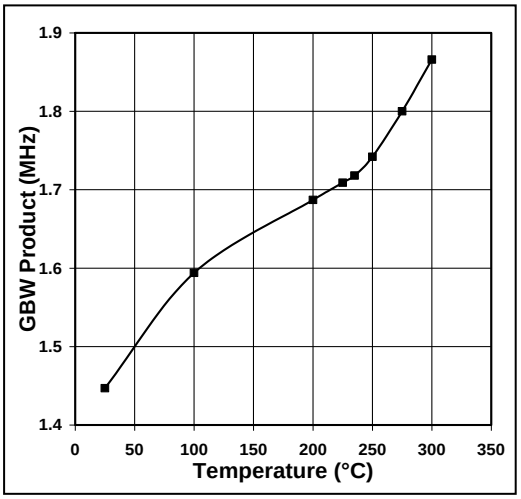
Offset voltage vs. Temperature



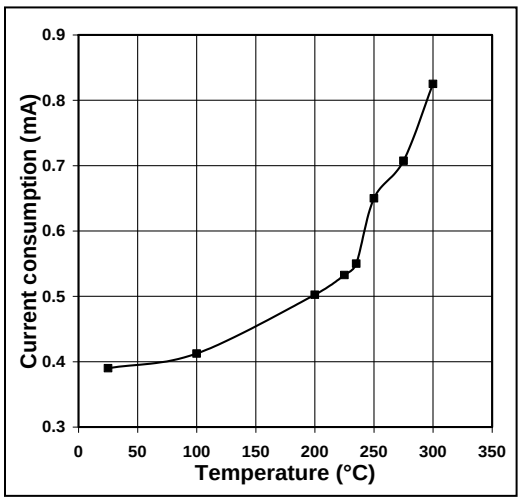
Sample size vs. Offset voltage



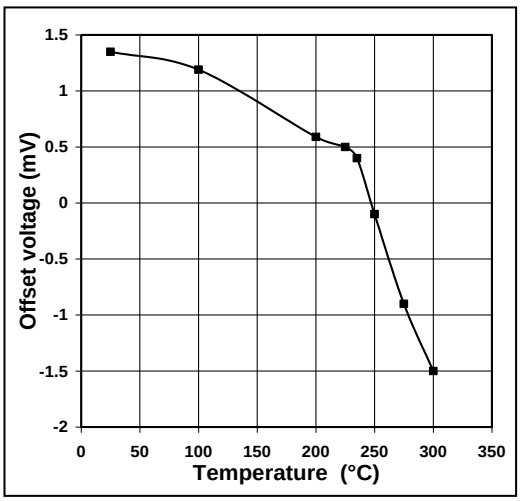
DC Gain vs. Temperature for V_{DD} = 10V. Typical



GBW vs. Temperature for V_{DD} = 10V. Typical



Current consumption per aplifier vs. Temperature for V_{DD} = 10V. Typical



Offset voltage vs. Temperature. Typical

Circuit Functionality

Operating conditions
The CHT-OPA has been qualified to operate with supply voltages ranging from 4.5V to 20V and temperatures from -55°C to 225°C. Device characteristics vary smoothly outside the qualification temperature range. Operation down to cryogenic temperatures has been achieved. On the other side of the temperature scale, operation up to 300°C has also been reached.

The CHT-OPA has been conceived to operate in closed loop configuration under linear regime. This limitation only applies for supply voltages above 5.5V. When operating with supply voltages above 5.5V, internal circuitry prevents exceeding "Safe Operating Area" conditions inside the circuit. Nevertheless, continuous or repetitive operation outside linear regime could permanently damage the part.

For supply voltages bellow 5.5V, no limitation on the operation regime exists and the part can even be used as comparator.

Specific Operating Conditions
The CHT-OPA presents slightly different positive and negative slewing values. This makes that when a square wave is used as input signal, the output presents an additional DC offset due to the slight change of the output duty cycle.

Additionally, for square input signals with frequencies above 10kHz, the circuit presents an output DC offset which increases with the input frequency. At 30kHz, the input referred offset increases by about 20mV.

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-OPA-DIL14-T	Ceramic DIL14	-55°C to +225°C	CHT-OPA
CHT-OPA-CSOIC16-T	Ceramic SOIC16	-55°C to +225°C	CHT-OPA

Contact & Ordering

CISSOID S.A.

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Document history

Revision	Modification	Author	Date
01.00	First issue	NPT	27/05/08
01.01	Updated Contact & Ordering information	GPN	19 Jan 09
02.00	Added pinout of SOIC16 packaged device. Updated features list and Ordering information table.	GPN	06 Apr 09

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Quality Manager: Laurent Demeûs	Date: Apr. 06, 09