Fully Integrated, 8-Channel Ultrasound Analog Front End for Ultrasound with Passive CW Mixer, 0.75 nV/rtHz, 12/14-Bit, 65 MSPS, 141 mW/CH

Check for Samples: AFE5807

FEATURES

- **8-Channel Complete Analog Front-End**
  - **LNA, VCA, PGA, LPF, ADC, and CW Mixer**
- **Programmable Gain Low-Noise Amplifier (LNA)**
  - **24/18/12 dB Gain**
  - **0.25/0.5/1.0 Vpp Linear Input Range**
  - **0.63/0.7/0.9 nV/rtHz Input Refered Noise**
  - **Programmable Active Termination**
- **40 dB Low Noise Voltage Controlled Attenuator (VCA)**
- **24/30 dB Programmable Gain Amplifier (PGA)**
- **3rd Order Linear Phase Low-Pass Filter (LPF)**
  - **10, 15, 20, 30 MHz**
- **14-bit Analog to Digital Converter (ADC)**
  - **74 dBFS SNR at 65 MSPS**
  - **LVDS Outputs**
- **Noise/Power Optimizations (Full Chain)**
  - **141 mW/CH at 0.75 nV/rtHz, 65 MSPS**
  - **88 mW/CH at 1.1 nV/rtHz, 40 MSPS**
  - **80 mW/CH at CW Mode**
- **Excellent Device-to-Device Gain Matching**
  - **±0.5 dB(typical) and ±0.9 dB(max)**
- **Low Harmonic Distortion**
- **Fast and Consistent Overload Recovery**
- **Passive Mixer for Continuous Wave Doppler(CWD)**
  - **Low Close-in Phase Noise –156 dBc/Hz at 1 KHz off 2.5 MHz Carrier**
  - **Phase Resolution of 1/16λ**
  - **Support 16X, 8X, 4X and 1X CW Clocks**
  - **12dB Suppression on 3rd and 5th Harmonics**
  - **Flexible Input Clocks**
- **Small Package: 15 mm x 9 mm, 135-BGA**

APPLICATIONS

- **Medical Ultrasound Imaging**
- **Nondestructive Evaluation Equipments**

DESCRIPTION

The AFE5807 is a highly integrated Analog Front-End (AFE) solution specifically designed for ultrasound systems in which high performance and small size are required. The AFE5807 integrates a complete time-gain-control (TGC) imaging path and a continuous wave Doppler (CWD) path. It also enables users to select one of various power/noise combinations to optimize system performance. Therefore, the AFE5807 is a suitable ultrasound analog front end solution not only for high-end systems, but also for portable ones.

The AFE5807 contains eight channels of Low-noise amplifier (LNA), Voltage Controlled Attenuator (VCA), Programmable Gain Amplifier (PGA), Low-pass Filter (LPF), 12/14-bit Analog-to-Digital Converter (ADC), and CW mixer. The LNA gain is programmable to support 250 mVpp to 1 Vpp input signals. Programmable active termination is also supported by the LNA. The ultra-low noise VCA provides an attenuation control range of 40dB and improves overall low gain SNR which benefits harmonic imaging and near field imaging. The PGA provides gain options of 24 dB and 30 dB. Before the ADC, a LPF can be configured as 10 MHz, 15 MHz, 20 MHz or 30 MHz to support ultrasound applications with different frequencies. The high-performance 14 bit/65 MSPS ADC in the AFE5807 achieves 74 dBFS SNR. It ensures good SNR at low chain gain. The ADC's LVDS outputs enable flexible system integration desired for miniaturized systems. The AFE5807 also integrates a low power passive mixer and a low noise summing amplifier to accomplish on-chip CWD beamformer. 16 selectable phase-delays can be applied to each analog input signal. Meanwhile a unique 3rd and 5th order harmonic suppression filter is implemented to enhance CW sensitivity.

The AFE5807 is available in a 15mm × 9mm, 135-pin BGA package and it is specified for operation from 0°C to 85°C. It is also pin-to-pin compatible to the AFE5808.

PRODUCT PREVIEW

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

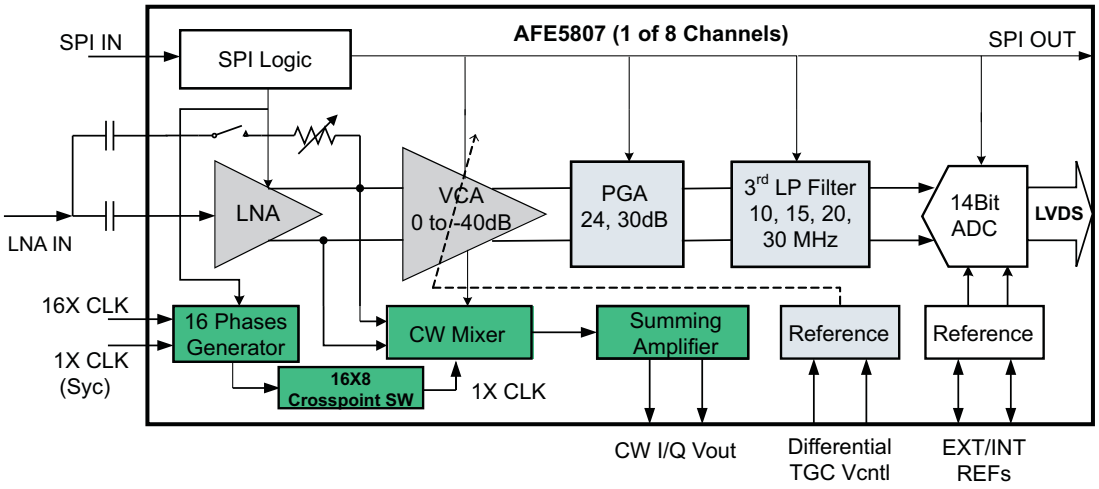

Figure 1. Block Diagram

PACKAGING/ORDERING INFORMATION(1)(2)

PRODUCT	PACKAGE TYPE	OPERATING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY	ECO STATUS(1)
AFE5807	ZCF	0°C to 85°C	AFE5807ZCF	Tray, 160	Pb-Free, Green

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree. GREEN: TI defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1%of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree . Pb-FREE: TI defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage range	AVDD	–0.3 to 3.9	V
	AVDD_ADC	–0.3 to 2.2	V
	AVDD_5V	–0.3 to 6	V
	DVDD	–0.3 to 2.2	V
Voltage between AVSS and LVSS		–0.3 to 0.3	V
Voltage at analog inputs and digital inputs		–0.3 to min [3.6,AVDD+0.3]	V
Voltage at digital outputs		–0.3 to min [2.2,AVDD_ADC+0.3]	V
Peak solder temperature(2)		260	°C
Maximum junction temperature (T_J), any condition		105	°C
Storage temperature range		–55 to 150	°C
Operating temperature range		0 to 85	°C
ESD Ratings	HBM	2000	V
	CDM	500	V
	MM	100	V

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied Exposure to absolute maximum rated conditions for extended periods may degrade device reliability.
(2) Device complies with JSTD-020D.

THERMAL INFORMATION

THERMAL METRIC(1)		AFE5807 BGA 135 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	5	
θ_{JB}	Junction-to-board thermal resistance	11.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	10.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	MAX	UNIT
AVDD	3.15	3.45	V
AVDD_ADC	1.7	1.9	V
DVDD	1.7	1.9	V
AVDD_5V	4.75	5.25	V
Ambient Temperature, T_A	0	85	°C

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DEVICE INFORMATION

PIN CONFIGURATION
Top View
ZCF (BGA-135)

	1	2	3	4	5	6	7	8	9
A	AVDD	INP8	INP7	INP6	INP5	INP4	INP3	INP2	INP1
B	CM_BYP	ACT8	ACT7	ACT6	ACT5	ACT4	ACT3	ACT2	ACT1
C	AVSS	INM8	INM7	INM6	INM5	INM4	INM3	INM2	INM1
D	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
E	CW_IP_AMPINP	CW_IP_AMPINM	AVSS	AVSS	AVSS	AVSS	AVSS	AVDD	AVDD
F	CW_IP_OUTM	CW_IP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_16X	CLKM_16X
G	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	AVSS	CLKP_1X	CLKM_1X
H	CW_QP_OUTM	CW_QP_OUTP	AVSS	AVSS	AVSS	AVSS	AVSS	PDN_GLOBAL	RESET
J	CW_QP_AMPINP	CW_QP_AMPINM	AVSS	AVSS	AVSS	AVDD_ADC	AVDD_ADC	PDN_VCA	SCLK
K	AVDD	AVDD_5V	VCNTLP	VCNTLM	VHIGH	AVSS	DNC	AVDD_ADC	SDATA
L	CLKP_ADC	CLKM_ADC	AVDD_ADC	REFM	DNC	DNC	DNC	PDN_ADC	SEN
M	AVDD_ADC	AVDD_ADC	VREF_IN	REFP	DNC	DNC	DNC	DNC	SDOUT
N	D8P	D8M	DVDD	DNC	DVSS	DNC	DVDD	D1M	D1P
P	D7M	D6M	D5M	FCLKM	DVSS	DCLKM	D4M	D3M	D2M
R	D7P	D6P	D5P	FCLKP	DVSS	DCLKP	D4P	D3P	D2P

PIN FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
B9~ B2	ACT1...ACT8	Active termination input pins for CH1~8.
A1, D8, D9, E8, E9, K1	AVDD	3.3V Analog supply for LNA, VCA, PGA, LPF and CWD blocks.
K2	AVDD_5V	5.0V Analog supply for LNA, VCA, PGA, LPF and CWD blocks.
J6, J7, K8, L3, M1, M2	AVDD_ADC	1.8V Analog power supply for ADC.
C1, D1~D7, E3~E7, F3~F7, G1~G7, H3~H7,J3~J5, K6	AVSS	Analog ground.
L2	CLKM_ADC	Negative input of differential ADC clock. In the single-end clock mode, it can be tied to GND directly or through a 0.1µF capacitor.
L1	CLKP_ADC	Positive input of differential ADC clock. In the single-end clock mode, it can be tied to clock signal directly or through a 0.1µF capacitor.
F9	CLKM_16X	Negative input of differential CW 16X clock. Tie to GND when the CMOS clock mode is enabled. In the 4X and 8X CW clock modes, this pin becomes the 4X or 8X CLKM input. In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
F8	CLKP_16X	Positive input of differential CW 16X clock. In 4X and 8X clock modes, this pin becomes the 4X or 8X CLKP input. In the 1X CW clock mode, this pin becomes the quadrature-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
G9	CLKM_1X	Negative input of differential CW 1X clock. Tie to GND when the CMOS clock mode is enabled. In the 1X clock mode, this pin is the In-phase 1X CLKM for the CW mixer. Can be floated if CW mode is not used.
G8	CLKP_1X	Positive input of differential CW 1X clock. In the 1X clock mode, this pin is the In-phase 1X CLKP for the CW mixer. Can be floated if CW mode is not used.
B1	CM_BYP	Bias voltage and >0.1µF bypass to ground. 1µF is recommended.
E2	CW_IP_AMPINM	Negative differential input of the In-phase summing amplifier. External LPF capacitor is connected. This pin becomes the CH7 PGA negative output when PGA test mode is enabled. Can be floated if not used.
E1	CW_IP_AMPINP	Positive differential input of the In-phase summing amplifier. External LPF capacitor is connected. This pin becomes the CH7 PGA positive output when PGA test mode is enabled. Can be floated if not used.

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PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NO.	NAME	
F1	CW_IP_OUTM	Negative differential output for the In-phase summing amplifier. External LPF capacitor is connected. Can be floated if not used.
F2	CW_IP_OUTP	Positive differential output for the In-phase summing amplifier. External LPF capacitor is connected. Can be floated if not used.
J2	CW_QP_AMPINM	Negative differential input of the quadrature-phase summing amplifier. External LPF capacitor is connected. This pin becomes CH8 PGA negative output when PGA test mode is enabled. Can be floated if not used.
J1	CW_QP_AMPINP	Positive differential input of the quadrature-phase summing amplifier. External LPF capacitor is connected. This pin becomes CH8 PGA positive output when PGA test mode is enabled. Can be floated if not used.
H1	CW_QP_OUTM	Negative differential output for the quadrature-phase summing amplifier. Can be floated if not used.
H2	CW_QP_OUTP	Positive differential output for the quadrature-phase summing amplifier. Can be floated if not used.
N8, P9~P7, P3~P1, N2	D1M~D8M	ADC CH1~8 LVDS negative outputs
N9, R9~R7, R3~R1, N1	D1P~D8P	ADC CH1~8 LVDS positive outputs
P6	DCLKM	LVDS bit clock (7x) negative output
R6	DCLKP	LVDS bit clock (7x) positive output
K7, L5~L7,M5~M8, N4, N6	DNC	Do not connect. Must leave floated
N3, N7	DVDD	ADC digital and I/O power supply, 1.8V
N5, P5, R5	DVSS	ADC digital ground
P4	FCLKM	LVDS frame clock (1X) negative output
R4	FCLKP	LVDS frame clock (1X) positive output
C9~C2	INM1…INM8	CH1~8 complimentary analog inputs. Bypass to ground with ≥ 0.015µF capacitors. The HPF response of the LNA depends on the capacitors.
A9~A2	INP1...INP8	CH1~8 analog inputs. AC coupled to T/R switch outputs with ≥ 0.1µF capacitors.
L8	PDN_ADC	ADC partial (fast) power down control pin with an internal pull down resistor of 100kΩ. Active High.
J8	PDN_VCA	VCA partial (fast) power down control pin with an internal pull down resistor of 20kΩ. Active High.
H8	PDN_GLOBAL	Global (complete) power-down control pin for the entire chip with an internal pull down resistor of 20kΩ. Active High.
L4	REFM	0.5V reference output in the internal reference mode. Must leave floated in the internal reference mode.
M4	REFP	1.5V reference output in the internal reference mode. Must leave floated in the internal reference mode.
H9	RESET	Hardware reset pin with an internal pull-down resistor of 100kΩ. Active high.
J9	SCLK	Serial interface clock input with an internal pull-down resistor of 100kΩ
K9	SDATA	Serial interface data input with an internal pull-down resistor of 100kΩ
M9	SDOUT	Serial interface data readout. High impedance when it is not activated by register 0
L9	SEN	Serial interface enable with an internal pull up resistor of 100kΩ. Active low.
K4	VCNTLM	Negative differential VCA attenuation control pin.
K3	VCNTLP	Positive differential VCA attenuation control pin
K5	VHIGH	Bias voltage; bypass to ground with ≥1µF.
M3	VREF_IN	ADC 1.4V reference input in the external reference mode; bypass to ground with 0.1µF.
K7, L5~L7, M5~M8, N4, N6	DNC	Do not connect. Must leave floated

PRODUCT PREVIEW

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
AFE5807ZCF	PREVIEW	BGA	ZCF	135		TBD	Call TI	Call TI	Samples Not Available
PAFE5807ZCF	PREVIEW	BGA	ZCF	135		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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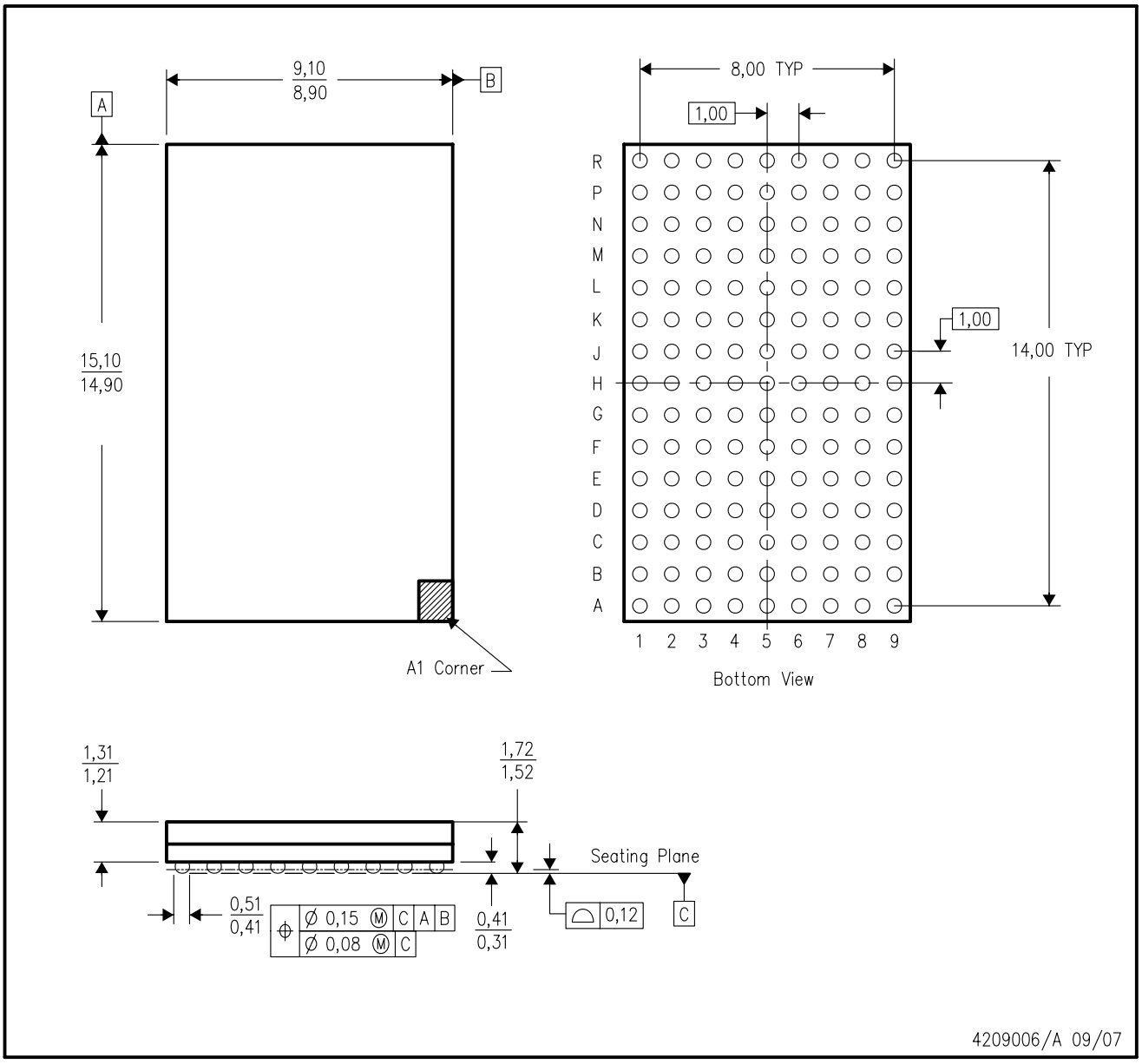
ZCF (R–PBGA–N135) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994 .
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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