AFBR-5978Z

Digital Diagnostic 650nm Transceiver for Fast Ethernet (10/100 Mbps) with SC-RJ connector

Data Sheet

Description

The AFBR-5978Z transceiver provides the system designer with the ability to implement Fast Ethernet (100 Mbps) or Ethernet (10 Mbps) over 50 meter standard bandwidth 0.5±0.05 NA POF and 100 meter standard bandwidth 0.37±0.04 NA HCS fiber. The connectivity available for the transceiver is SC-RJ. This product is lead free and compliant with RoHS.

Transmitter

The transmitter contains a 650nm LED with an integrated driver. The LED driver operates at 3.3 V. It receives a LVPECL compatible electrical input, and converts it into a modulated current driving the LED. The LED is packaged in an optical subassembly, part of the transmitter section. The optical subassembly couples the output optical power efficiently into POF or HCS fiber.

Receiver

The receiver utilizes a Si PIN photodiode. The PIN photodiode is packaged in an optical sub-assembly, part of the receiver section. This optical subassembly couples the optical power efficiently from POF or HCS fiber to the receiving PIN. The integrated IC operates at 3.3 V and converts the photocurrent into LVPECL compatible electrical output.

Package

The transceiver package consist of four basic elements; two optical subassemblies, an electrical subassembly and the housing as illustrated in the block diagrams in Figure 1. The package outline drawing and pin out are shown in Figures 2 and 3.

Features

- Compatible with electrical and optical performance of the POFAC recommendations for the Fast Ethernet over Plastic Optical Fiber (POF).
- Compatible with the Electrical and Optical performance of the ProfiNet recommendations the Fast Ethernet over POF and Hard-Clad Silica Fiber (HCS).
- Manufactured in an ISO 9001 certified facility
- DMI [Digital Diagnostics Monitoring Interface, SFF-8472 Rev 9.3], provides real-time monitoring of:
  - Temperature
  - Supply voltage
  - Received Optical Power (Alarm/Warning flag)
- LVPECL Signal Detect Output
- Temperature range –25 to +85 °C

Applications

- Factory automation at Fast Ethernet speeds
- Fast Ethernet networking over POF and HCS
- Link Distance up to 50 m POF or 100 m HCS (See application note 5290 for details)

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AFBR-5978Z is compatible with the SC-RJ Connecting System from Reichle & De-Massari AG, Switzerland

Block diagram

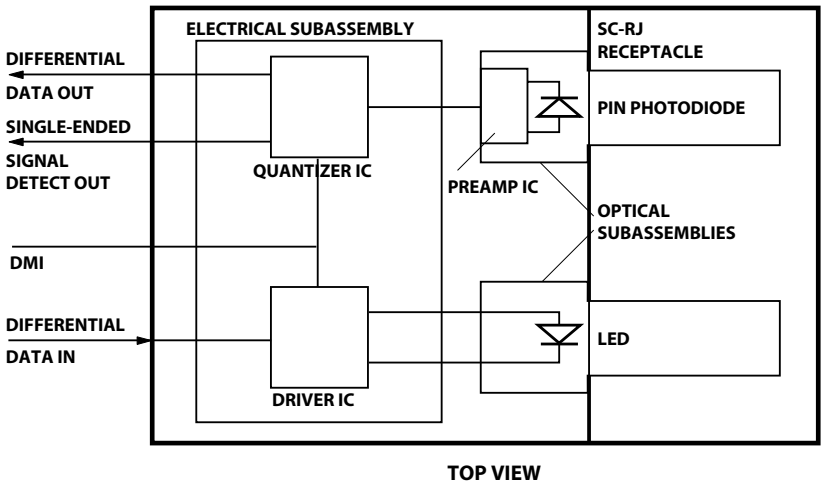

Figure 1. Block diagram

The optical subassemblies utilize a high volume assembly process together with low cost lens elements which result in a cost effective building block.

The electrical subassembly consists of a high volume multilayer printed circuit board on which the IC chips and various surface mounted passive circuit elements are attached.

The housing includes internal shields for the electrical and optical subassemblies to insure low EMI emissions and high immunity to external EMI fields. The outer housing including the duplex SC-RJ connector is molded of filled non-conductive plastic to provide mechanical strength and electrical isolation. The low profile of the Avago Technologies transceiver design complies with the maximum height allowed for the duplex SC-RJ connector over the entire length of the package.

The transceiver is attached to a printed circuit board with twelve signal pins and the two solder posts, which exit the bottom of the housing. The two solder posts provide the primary mechanical strength to withstand the mechanical loads imposed on the transceiver by mating with the SC-RJ connectored fiber cables. The solder posts are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board

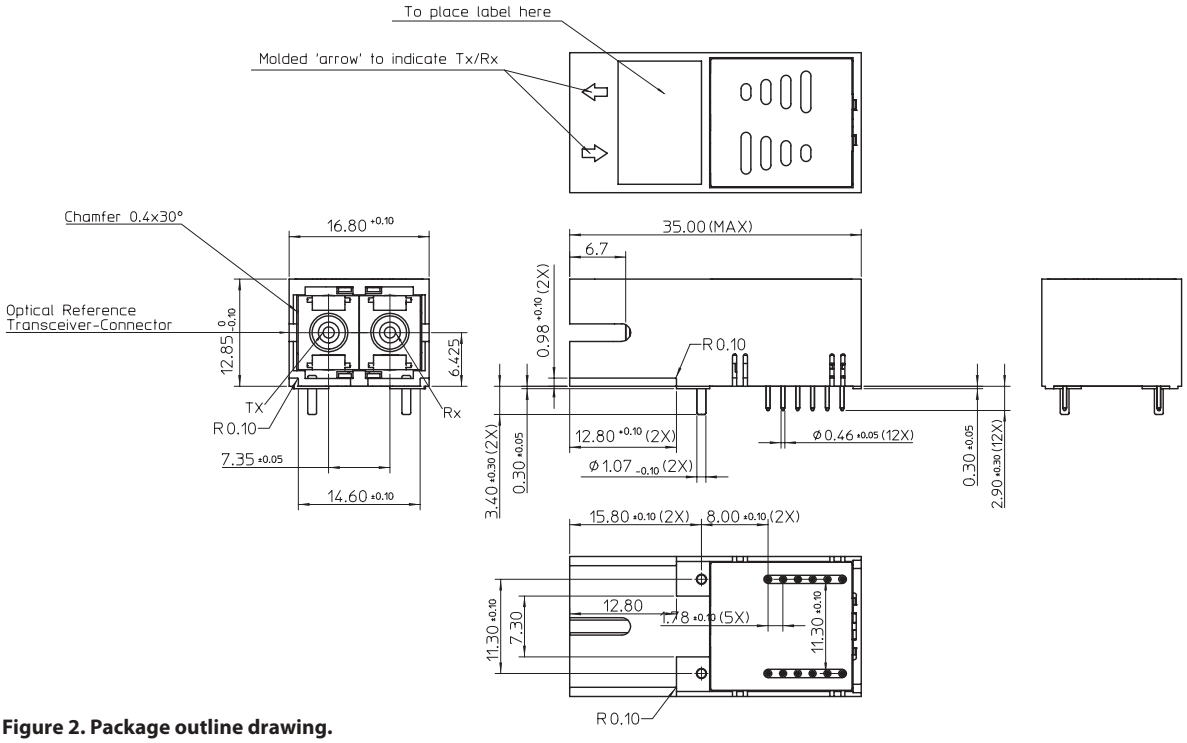

Figure 2. Package outline drawing.

Pin Descriptions

Pin 1 Sda: the data line of the two wire serial interface. This data line should be pulled up with a 4.7k–10kΩ resistor on the host board to a supply of 3.3V ±10%.

Pin 2 Rx GND: receiver ground pin. Directly connect this pin to the receiver ground plane of the host board.

Pin 3 Rx Vcc: receiver power supply pin. Provide +3.3 V DC via a receiver power supply filter circuit. Locate the power supply filter circuit as close as possible to the Vcc Rx pin.

Pin 4 Sd: signal detect pin. If an optical signal is present at the input of the receiver, Sd output is a logic "1". Absence of an optical signal to the receiver results in a logic "0" output. This signal detect output can be used to drive a LVPECL input on an upstream circuit, such as Signal Detect input or Loss of Signal–bar. Proper LVPECL termination should be in place. See figure 4.

Pin 5 Rdata-: receiver data out bar. This data line is a 3.3V LVPECL compatible differential line which should be properly terminated with a 130Ω pull up to Vcc and 82Ω pull down to ground.

Pin 6 Rdata+: receiver data out. This data line is a 3.3V LVPECL compatible differential line which should be properly terminated with a 130Ω pull up to Vcc and 82Ω pull down to ground.

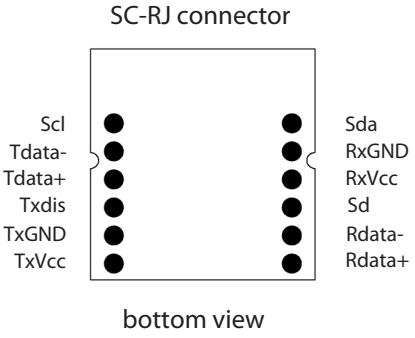

Figure 3. Pin Out diagram

Pin 7 Tx Vcc: transmitter power supply. Provide +3.3V DC via a transmitter power supply filter circuit. Locate the power supply filter circuit as close as possible to the Vcc Tx pin.

Pin 8 Tx GND: transmitter ground. Directly connect this pin to the transmitter ground plane on the host board.

Pin 9 Txdis: transmitter disable input. This input is used to shut down the transmitter light output. It is internally pulled up with a ~8 kΩ resistor.

Low (0-0.8 V) - transmitter on

Between (0.8-2.0 V) - undefined

High (2.0-3.63 V) – transmitter off

Open – transmitter off

Pin 10 Tdata+: transmitter data in. This data line is an AC coupled 100Ω differential line which does not need any termination at the user SERDES. The AC coupling is done inside the module and therefore not required on the host board.

Pin 11 Tdata-: transmitter data in bar. This data line is an AC coupled 100Ω differential line which does not need any termination at the user SERDES. The AC coupling is done inside the module and therefore not required on the host board.

Pin 12 Scl: the clock line of the two wire serial interface. This data line should be pulled up with a 4.7k – 10 kΩ resistor on the host board to a supply of 3.3V ±10%.

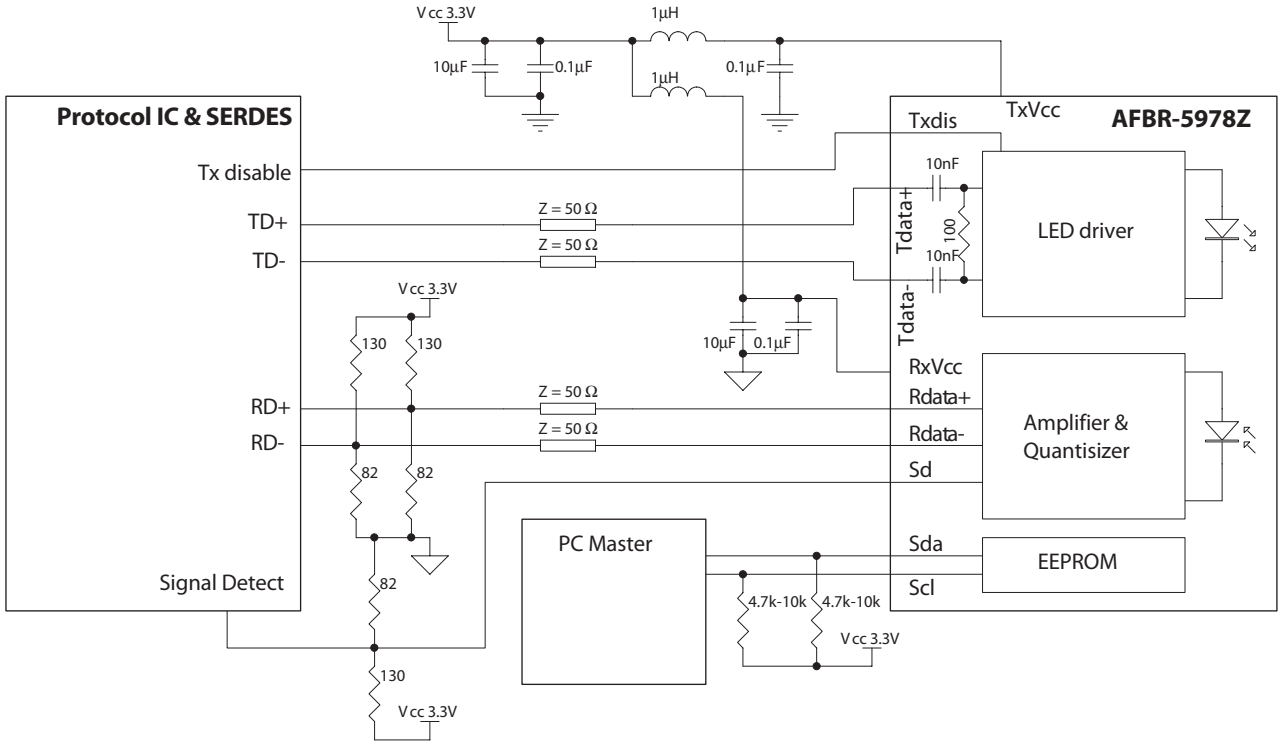

Figure 4. Recommended termination circuit.

Board Layout – Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from the transceiver. A power supply decoupling circuit is recommended to filter out noise to assure optimal product performance. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

Functional Data I/O

The LVPECL receiver output of the Avago Technologies transceiver can be DC-coupled to the LVPECL compliant network interface through a Thèvenin equivalent transformation. For a 3.3V power supply the LVPECL outputs should be pulled up to Vcc with a 130Ω resistor and pulled down to ground with an 82Ω resistor. Both coupling resistors are preferably placed close to the network interface IC, see figure 4. AC-coupling can be used for systems in which the transceiver and connected logic are at different supply voltages. For AC coupling, the coupling capacitor should be large enough to avoid excessive low-frequency droop when the data signal contains long strings of consecutive identical digits. The LVPECL outputs have to be pulled down to ground first to DC bias the output before AC coupling. Because the LVPECL output common-mode voltage is fixed at Vcc – 1.3V, the DC-biasing resistor can be selected by assuming 14 mA DC current. This results in a bias-resistor value of 142Ω - 200Ω. After the AC-coupling capacitors, a Thèvenin equivalent transformation connects to the LVPECL compatible network interface, equal to the one used in DC-coupling.

Digital Diagnostics Monitoring Interface

The AFBR-5978Z transceiver features an enhanced digital diagnostic interface, compliant to the "Digital Diagnostic Monitoring Interface for Optical Transceivers" SFF-8472 Multi-source Agreement (MSA). Please refer to the MSA document to access information on the range of options, both hardware and software, available to the host system for exploiting the available digital diagnostic features.

The enhanced digital interface allows real-time access to device operating parameters, and includes optional digital features such as soft control and monitoring of I/O signals. In addition, it fully incorporates the functionality needed to implement digital alarms and warnings, as defined by the SFF-8472 MSA. With the digital diagnostic monitoring interface, the user has capability of performing component monitoring, fault isolation and failure prediction in their transceiver-based applications.

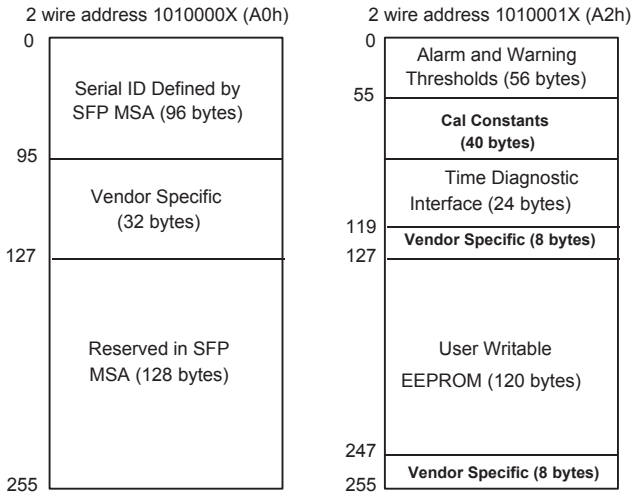

Figure 5. Digital diagnostic memory map – specific data field description (from SFF-8472 MSA)

The diagnostic monitoring interface (DMI) has two 256 byte memory maps in EEPROM which are accessible over a two wire interface: the serial ID memory map at address 1010000X (0xA0) and the digital diagnostic memory map at address 1010001X (0xA2).

The serial ID memory map contains a serial identification and vendor specific information and is read only.

The digital diagnostic memory map contains device operating parameters and alarm and warning flags. The operating parameters are to be retrieved through a sequential read command ensuring that the MSB and LSB of each parameter are "coherent". Furthermore, it contains 120 bytes that can be written by the user as well as a writable soft control byte.

Tables 1 to 6 detail memory contents, timing characteristics, soft commands and alarm/warning flags.

Table 1. Transceiver soft diagnostics Timing characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Hardware TX_DISABLE assert time	t_off		10	µs	Note 1, Figure 6
Hardware TX_DISABLE negate time	t_on		1	ms	Note 2, Figure 6
Time to initialize	t_init		100	ms	Note 3, Figure 6
Hardware RX_SD assert time	t_sd_on		100	µs	Note 4
Hardware RX_SD de-assert time	t_sd_off		100	µs	Note 5
Software TX_DISABLE assert time	t_off_soft		100	ms	Note 6
Software TX_DISABLE negate time	t_on_soft		100	ms	Note 7
Software RX_SD assert time	t_sd_on_soft		100	ms	Note 8
Software RX_SD de-assert time	t_sd_off_soft		100	ms	Note 9
Analog parameter data ready	t_data		1000	ms	Note 10
Serial bus hardware ready	t_serial		300	ms	Note 11
Write cycle time	t_write		10	ms	Note 12
Serial ID clock rate	f_serial_clock		400	kHz	Note 13

Notes:
1. Time from rising edge of TX_DISABLE to when the optical output falls below 10% of nominal.
2. Time from falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
3. Time from Power on or falling edge of TX_DISABLE to when the modulated optical output rises above 90% of nominal.
4. Time from valid optical signal to RX_SD assertion.
5. Time from loss of optical signal to RX_SD de-assertion.
6. Time from two-wire interface assertion of TX_DISABLE (A2h, byte 110, bit 6) to when the optical output falls below 10% of nominal. Measured from falling clock edge after stop bit of write transaction.
7. Time from two-wire interface de-assertion of TX_DISABLE (A2h, byte110, bit 6) to when the modulated optical output rises above 90% of nominal.
8. Time for two-wire interface assertion of RX_SD (A2h, byte 110, bit 1) from presence of valid optical signal.
9. Time for two-wire interface de-assertion of RX_SD (A2h, byte 110, bit 1) from loss of optical signal.
10. From power on to data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is operational.
11. Time from power on until module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
12. Time from stop bit to completion of a 1-8 byte write command.
13. Contact Avago Technologies for applications at faster (>400 kHz) Serial ID clock rates.

Table 2. Transceiver Digital Diagnostic Monitor Characteristics

Parameter	Symbol	Min.	Unit	Notes
Transceiver internal temperature accuracy	T_{INT}	5.0	°C	Temperature is measured internal to the transceiver. Valid from -25°C to 85°C case temperature.
Transceiver internal supply voltage accuracy	V_{INT}	0.1	V	Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the Vcc pin. Valid over 3.3V ± 10%.

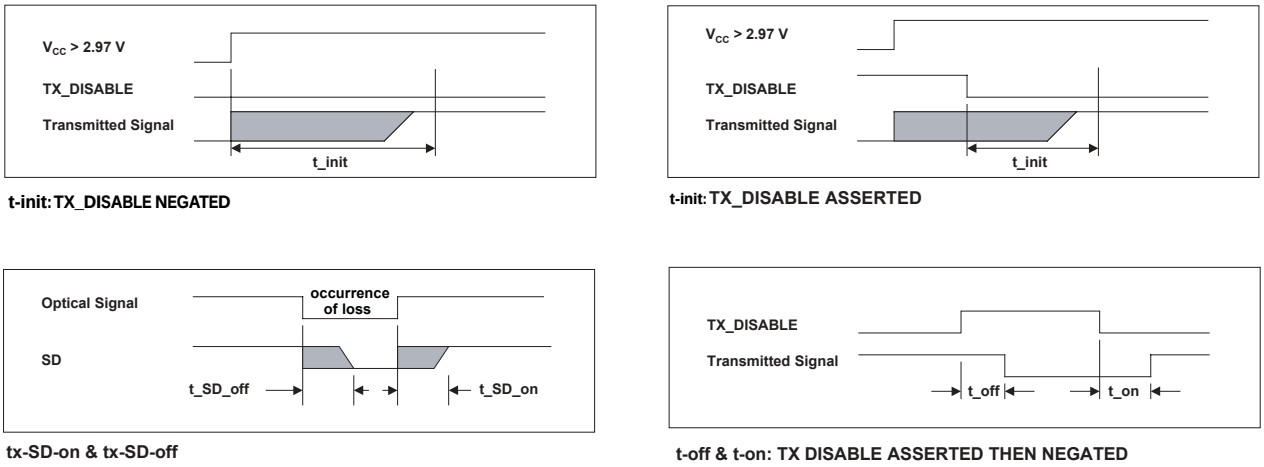

Figure 6. Transceiver timing diagrams.

Table 3. EEPROM Serial ID Memory Contents – Address A0h

Addr	Hex	ASCII	Description	Addr	Hex	ASCII	Description
0	00			40	41	A	
1	00			41	46	F	
2	00			42	42	B	
3	00			43	52	R	
4	00			44	2D	-	
5	00			45	35	5	
6	00			46	39	9	
7	00			47	37	7	
8	00			48	38	8	
9	00			49	5A	Z	
10	00			50	20		
11	00			51	20		
12	00			52	20		
13	00			53	20		
14	00			54	20		
15	00			55	20		
16	00			56	20		
17	00			57	20		
18	00			58	20		
19	00			59	20		
20	41	A		60	02		Note 1
21	56	V		61	8A		Note 1
22	41	A		62	00		Note 1
23	47	G		63			Note 4
24	4F	O		64	00		
25	20			65	14		
26	54	T		66	00		
27	45	E		67	00		
28	43	C		68 - 83			Note 2
29	48	H		84 - 91			Note 3
30	20			92	68	h	
31	20			93	D0		
32	20			94	01		
33	20			95			Note 4
34	20			96 - 127			Note 5
35	20						
36	00						
37	00						
38	17						
39	6A						

Notes:
1. LED wavelength is represented in 16 unsigned bits. The hex representation of 650 (nm) is 0x28A.
2. Address 68-83 specify a unique module serial number.
3. Address 84-91 specify the date code.
4. Address 63 is the checksum for bytes 0-62 and address 95 is the checksum for bytes 64-94. They are calculated (per SFF-8472) and stored prior to product shipment.
5. Address 96-127 is vendor specific.

Table 4. EEPROM DMI Memory Contents – Address A2h

Addr	Hex	Dec	Description	Addr	Hex	Dec	Description
0	73	115	Temp H alarm MSB[1,5]	95			Checksum for bytes 0 to 94[7]
1	00	0	Temp H alarm LSB[1,5]	96			Real time temperature MSB[1]
2	D8	216	Temp L alarm MSB[1,5]	97			Real time temperature LSB[1]
3	00	0	Temp L alarm LSB[1,5]	98			Real time Vcc MSB[2]
4	69	105	Temp H warning MSB[1,5]	99			Real time Vcc LSB[2]
5	00	0	Temp H warning LSB[1,5]	100 to 109			Reserved[8]
6	E7	231	Temp L warning MSB[1,5]	110			Status control - see table 5
7	00	0	Temp L warning LSB[1,5]	111			Reserved[8]
8	98	152	Vcc H alarm MSB[2,5]	112			Flag bit - see table 6
9	58	88	Vcc H alarm LSB[2,5]	113			Flag bit - see table 6
10	69	105	Vcc L alarm MSB[2,5]	114			Reserved[8]
11	78	120	Vcc L alarm LSB[2,5]	115			Reserved[8]
12	8D	141	Vcc H warning MSB[2,5]	116			Flag bit - see table 6
13	CC	204	Vcc H warning LSB[2,5]	117			Flag bit - see table 6
14	74	116	Vcc L warning MSB[2,5]	118			Reserved[8]
15	04	4	Vcc L warning LSB[2,5]	119 to 127			Vendor specific
16 to 39			Reserved[8]	128 to 247			Customer writable
40	08	8	Rx OMA Margin L alarm[3,4,5]	248 to 255			Vendor specific
41	12	18	Rx OMA Margin L warning[3,4,5]				
42 to 55			Reserved[8]				
56 to 94			Note 6				

Notes:
1. Temperature (Temp) is decoded as a 16 bit signed twos complement integer in increments of 1/256 °C.
2. Supply voltage (Vcc) is decoded as a 16 bit unsigned integer in increments of 100 µV.
3. Received optical modulation amplitude margin or Rx OMA margin is a measure for the reserve in OMA to Sensitivity.
4. Received OMA margin is decoded as an 8 bit signed twos compliment integer in increments of 0.2 dB.
5. This register is read only. A write will be acknowledged but not stored.
6. Bytes 56-94 are not intended for use with AFBR-5978Z, but have been set to default values per SFF-8472.
7. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.
8. Reserved registers will return “00” when read. A write to a reserved register will be acknowledged but not stored.

Table 5. EEPROM Serial ID Memory Contents – Soft Commands (Address A2h, byte 110)

Bit #	Status / Control name	Description	Notes
7	TX_DISABLE State	Digital state of TX_DISABLE input pin (logic 1 = TX_DISABLE asserted)	Note 1
6	Soft TX_DISABLE	Read/write bit for changing digital state of TX_DISABLE function	Note 1,2
5	Reserved		Note 3
4	Not supported		Note 4
3	Not supported		Note 5
2	Not supported		Note 6
1	RX_SD State	Digital state of the RX_SD output pin (logic 0 = RX_SD asserted)	Note 1
0	Data Ready (Bar)	Indicates transceiver is powered and real time sense data is ready (0 = ready)	Note 7

Notes:
1. The response time for soft commands of the AFBR-5978Z is 100 ms as specified by the MSA SFF-8472.
2. Bit 6 is logic OR'd with the TX_DISABLED input pin. Either asserted will disable the transmitter.
3. Reserved bits will return "0" when read. A write to a reserved bit will be acknowledged but not stored.
4. A read from bit 4 will return "1". A write will be acknowledged but not stored.
5. A read/write from/to bit 3 will be acknowledged and stored but will be ignored by the transceiver.
6. A read from bit 2 will return "0". A write will be acknowledged but not stored.
7. AFBR-5978Z meets the MSA SFF-8471 data ready timing of 1000 ms.

Table 6. EEPROM Serial ID Memory Contents – Alarm and Warnings (Address A2h, bytes 112, 113, 116, 117)

Byte	Bit	Flag bit name	Description
112	7	Temp high alarm	Set when transceiver internal temperature exceeds high alarm threshold
	6	Temp low alarm	Set when transceiver internal temperature exceeds low alarm threshold
	5	Vcc high alarm	Set when transceiver internal supply voltage exceeds high alarm threshold
	4	Vcc low alarm	Set when transceiver internal supply voltage exceeds low alarm threshold
	3-0	Reserved	Note 1
113	7-6	Reserved	Note 1
	5	Rx OMA Margin low alarm	Set when received Rx OMA Margin exceeds low alarm threshold, Note 2
	4-0	Reserved	Note 1
116	7	Temp high warning	Set when transceiver internal temperature exceeds high warning threshold
	6	Temp low warning	Set when transceiver internal temperature exceeds low warning threshold
	5	Vcc high warning	Set when transceiver internal supply voltage exceeds high warning threshold
	4	Vcc low warning	Set when transceiver internal supply voltage exceeds low warning threshold
	3-0	Reserved	Note 1
117	7-6	Reserved	Note 1
	5	Rx OMA Margin low warning	Set when receiver Rx OMA Margin exceeds low warning threshold, Note 2
	4-0	Reserved	Note 1

Notes:
1. Reserved bits will return "0" when read. A write to a reserved bit will be acknowledged but not stored.
2. Received optical modulation amplitude margin or Rx OMA margin is a measure for the reserve in OMA to Sensitivity.

Regulatory Compliance Table

Feature	Test Method	Performance
MIL-STD 883	Method 3015, 100 pF / 1.5 k 5 pulse per polarity	ESD resistance Human Body Model ±2 kV
IEC 61000-4-2	Typically withstand an electrostatic discharge without damage when the SC-RJ connector receptacle is contacted by a Human Body Model probe	Level 3 Air discharge ESD resistance ±8 kV Contact discharge ESD resistance ±6 kV
IEC 61000-4-3	Typically show no measurable effect from an electric field applied to the transceiver when mounted to a circuit board without chassis enclosure.	Level 3 10 V/m Electric field immunity:
EN60825-1	As specified in IEC 60825-1 version 1.2.	AEL Class 1 TÜV Certificate number R72062581

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause catastrophic damage to the device. Limits apply to each parameter in isolation, all other parameters having values within the recommended operation conditions. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time. Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_s	-40	+100	°C	
Case Operating Temperature	T_C	-25	+85	°C	
Lead Soldering Temperature	T_{sold}		260	°C	Note 1
Lead Soldering Time	t_{sold}		10	s	Note 1
Supply Voltage	V_{cc}	-0.5	4.0	V	
Data Input Voltage	V_i	-0.5	V_{CC}	V	
Differential Input Voltage	V_D		2.0	V	peak to peak
Output Current PECL	I_{Dout}	-50	50	mA	
ESD-Resistance - Human Body Model	V_{ESD}	-2	+2	kV	Note 2
ESD-Resistance - Air Discharge	V_{ESD}	-8	+8	kV	Note 3
ESD-Resistance - Contact Discharge	V_{ESD}	-6	+6	kV	Note 4
Electric Field Immunity	V_{EMI}		15	V/m	IEC 61000-4-3

Notes:
1. The transceiver is Pb-free wave solderable.
2. Human Body Model: 100pF/1.5kΩ, 5 pulse / polarity; MIL-STD.883 Meth. 3015.
3. Air discharge IEC 61000-4-2 level 3 ESD-Resistance for the transceiver.
4. Contact discharge IEC 61000-4-2 level 3 ESD Resistance for the transceiver.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Case Operating Temperature	T_C	-25		+85	°C	
Supply Voltage	V_{cc}	2.97	3.3	3.63	V	
Differential Input Voltage	V_D	0.4	0.800	1.6	V	peak to peak
Data and Signal Detect Output Load	R_L		50		Ω	
Signalling rate (Fast-Ethernet)	B		125		MBd	4B/5B, 5
Signalling rate (Ethernet)	B		20		MBd	Manchester, 5
Humidity		5		95	%	

Notes:
5. Ethernet and Fast Ethernet optical auto-negotiation signals over a 1 MHz carrier are supported.

Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Current	I_{cc}		250	300	mA	
Power Dissipation	P_{DISS}		825		mW	
Power Supply Noise Reduction	PSNI	50			mV	peak to peak

Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data In Current - Low	I_{Din}		-2		µA	
Data In Current - High	I_{Din}		18		µA	

Transmitter Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Average Launched Power (1mm POF, NA=0.5)	Po	-8.5	-4.5	-2	dBm	note 6
Average Launched Power (200um HCS, NA=0.37)	Po	-19.5	-15	-11	dBm	note 6
Optical Modulation Amplitude (POF)	OMA	-6.5	-3	-0.5	dBm	peak to peak, note 6
Optical Modulation Amplitude (HCS)	OMA	-17.5	-13.5	-9.5	dBm	peak to peak, note 6
Central Wavelength	λ_c	635	650	660	nm	note 6, 7
Spectrum RMS	$\Delta\lambda$			17	nm	note 6, 8
Optical Rise Time (10%-90%)	t_r		2.7	6.5	ns	note 6
Optical Fall Time (10%-90%)	t_f		2.7	6.5	ns	note 6
Duty Cycle Distortion Contributed by the Transmitter	DCD	-1		+1	ns	peak to peak, note 6
Random Jitter Contributed by the Transmitter	RJ			0.2	ns	peak to peak, note 6
Overshoot	Ov			40	%	note 6

Notes:

6. Measured at the end of 1 meter optical fiber.
7. Central wavelength is defined as:

$$\lambda_c = \frac{\sum_{i=1}^{N} P_i \lambda_i}{\sum_{i=1}^{N} P_i}$$

Ref: EIA/TIA standard FOTP-127/6.1, 1991

8. Spectrum RMS is defined as:

$$\Delta\lambda = \left[\left(\frac{\sum_{i=1}^{N} P_i \lambda_i^2}{\sum_{i=1}^{N} P_i} \right) - \lambda_c^2 \right]^{\frac{1}{2}}$$

Ref: EIA/TIA standard FOTP-127/6.3, 1991

Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Data Output Voltage - Low	V_{OL}-V_{cc}		-1.63		V	
Data Output Voltage - High	V_{OH}-V_{cc}		-0.99		V	
Data Output Voltage Swing	$\|V_{OH}$-$V_{OL}\|$	400		800	mV	single ended
Data Output Rise Time	t_r		1.45	2.20	ns	
Data Output Fall Time	t_f		0.98	2.20	ns	
Duty Cycle Distortion	DCD	-1		+1	ns	peak to peak
Data Dependent Jitter (rise/fall)	DDJ		0.6	1.5	ns	peak to peak
Random Jitter	RJ		0.1	0.2	ns	peak to peak
Signal Detect Output Voltage - Low	V_{OL}-V_{cc}	-2.2	-1.63	-1.5	V	
Signal Detect Output Voltage - High	V_{OH}-V_{cc}	-1.2	-0.99	-0.7	V	

Receiver Optical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unstressed receiver sensitivity, OMA (POF)	OMA	-22.5	-25		dBm	peak-peak, note 9
Unstressed receiver sensitivity, OMA (HCS)	OMA	-26.3	-29.3		dBm	peak-peak, note 9
Input Optical Power Maximum, OMA (POF)	$P_{IN\ MAX}$			+1	dBm	peak-peak, note 10
Input Optical Power Maximum, OMA (HCS)	$P_{IN\ MAX}$			-4	dBm	peak-peak, note 10
Operating Wavelength	$_R$	635	650	660	nm	
Signal Detect Asserted	P_A		2		dB	note 11
Signal Detect De-asserted	P_D		5		dB	note 11
Signal Detect Hysteresis	P_A - P_D	1.5	3		dB	

Notes:
9. Measured with PRBS 2^7-1 sequence, BER < $2.5x10^{-10}$.
10. Input Optical Power Maximum is defined as the maximum optical modulation amplitude where the receiver duty cycle distortion reaches ±1 ns.
11. Signal Detect Asserted and De-asserted levels are indicated as dB below unstressed receiver sensitivity level for either POF or HCS.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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