AFBR-720XPDZ
10Gbps 850nm XFP Transceiver

Application Note 5369

1. Introduction

The 850nm XFP transceiver is a high performance, cost effective module for serial optical data communications applications specified for signal rate of 10.3125 Gb/s. It is compliant to XFP MSA Rev 4.5. The module is designed for multi-mode fiber and operates at a nominal wavelength of 850nm. The transmitter section incorporates a directly modulated 850nm vertical cavity side emitting laser (VCSEL). The receiver section uses a GaAs PIN photodetector. Integrated Tx and Rx eye openers provide high jitter-tolerance and low jitter-generation and transfer for full XFI compliance. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry. The electrical interface is made using an industry standard 0.8 mm pitch 30-pin right angle connector. Optical connection is made via the duplex LC connector.

Figure 1 shows the XFP in comparison with a few other 10G transceiver form factors.

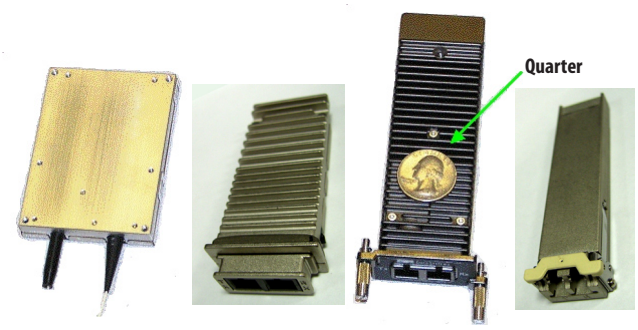

Figure 1. Left-Right, (a) 300 pin Transponder (b) X2 (c) Xenpak (d) XFP

It is intended for optical links of up to 300m on 50/125um OM3 fiber.

The dimensions of the XFP transceiver are shown in comparison with transceiver dimensions from other Multi-Source Agreements.

This document should be used in conjunction with the following other documents

- Avago AFBR-720XPDZ Product Datasheet
- Avago AFBR-720XPDZ Characterization Report
- XFP MSA Rev 4.5
- TIA/EIA-604-10A
- IEEE 802.3ae 10Gbase-SR Specifications
- HFCT-5014 XFP Evaluation Board User Guide
- XFP GUI User Manual
- Avago Technologies White Paper "Considerations for High Speed PCB Track Design in 10Gb/s Serial Data Transmission," Steve Bowers and Herbert Lage
- Interoperability Reports and Reference Design documents

Table 1. 10G Optical Transceiver Form-Factor Comparison

	Height	Width	Length
XFP	8.5 mm	18.35 mm	78 mm
X2	19.5 mm	42 mm	91 mm
Xenpak	22 mm	51.3 mm	121 mm

1.1. Getting Additional Help

If you require additional help in designing the module into your system, please contact an Avago Technologies Field representative.

2. Module Description

This application note is intended for use as a design guide for system designers. It also details some important results of the Avago Technologies AFBR-720XPDZ characterization that will facilitate a better understanding of the XFP's performance.

2.1. Functional Description

The XFP uses the high-speed XFI interface to convert 10Gbps serial electrical data into an optical serial bit stream.

2.2. Transmitter Path Summary

The transmitter section of the AFBR-720XPDZ houses a fully hermetic Transmitter Optical Sub Assembly. The source used in this product is a Vertical Cavity Side Emitting Laser (VCSEL). The VCSEL operates at a nominal center wavelength of 850nm.

2.3. Receiver Path Summary

The receiver section of the AFBR-720XPDZ houses a GaAs p-i-n receiver photodiode and an electronic pre-amplifier for excellent responsivity characteristics.

2.4. High-Speed (XFI) Path Summary

Tx and Rx eye openers provide high jitter-tolerance and low jitter generation and transfer for full XFI compliance. The internally ac coupled high speed serial I/O simplifies interfacing to external circuitry.

2.5. Low-Speed Signals

The XFP provides 7 low-speed signals that are used for reporting status as well as a means for the host board to control the XFP.

- Mod_NR
- Mod_DeSel
- Interrupt
- TX_DIS
- Mod_ABS
- RX_LOS
- P_Down/RST

All the 7 pins are LVTTL compatible.

2.6. 2-wire interface

The XFP has static and dynamic memory contents that are accessible through a 2-wire interface. The 2-wire interface follows the communication protocol as outlined in the XFP MSA. The signaling scheme is based on Low Voltage TTL operating at a nominal voltage of 3.3V.

For a detailed description of the 2-wire communication protocol, please refer to the XFP MSA Rev 4.5.

3. Applications

The Avago AFBR-720XPDZ is designed for 10Gigabit Ethernet Application.

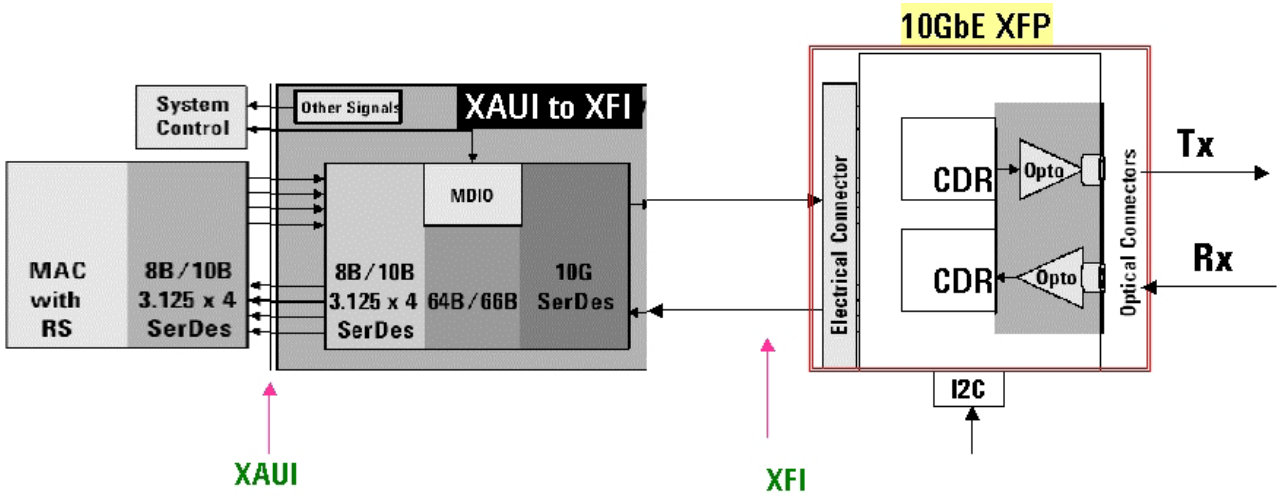

Figure 2. The AFBR-720XPDZ configured in a 10GbEthernet Application

4. Design Guidelines

4.1. PCB layout

Description

The XFP requires high-speed traces between the ASIC/SERDES and the XFP. This is referred to as the 'XFI Channel.' The channel provides a reliable high-speed connection between the ASIC and the XFP module on the host board.

Design Tips

There are many factors affecting the signal integrity of high-speed data links: -

1. Track dimensions
2. Dielectric material properties of the PCB
3. The physical design of the pluggable connector (effects of implementation)
4. Discontinuities between the track and component pads (reflections)
5. Type and length of track used, microstrip / strip line
6. Physical configuration of vias
7. Data pattern - dependency of the signal quality – jitter
8. Temperature Dependency

The most common material used for designing tracks is FR-4. At 5.5 GHz, the e (dielectric constant) of FR-4 is ~ 4.2. For high-data rate systems, dielectric losses are higher than skin-effect losses. For short trace lengths, the use of lossy material may introduce additional attenuation that improves return loss in the XFI channel.

The introduction of vias into the high-speed path will lead to multiple reflections that degrade the quality of the signal.

For XFI channels where the transceiver and the Avago Technologies XFPs are close to each other, the use of standard FR-4 micro-strip lines with high losses becomes feasible.

For XFI channels that are much longer, the use of stripline interconnects incorporating low loss FR-4 material may be required. It is also important to follow the essential rules of via design, including (a) appropriate clearances and (b) back-drilling to reduce via stub lengths.

Please refer to Avago Technologies white paper on "Considerations for High Speed PCB Track Design in 10 Gbps Serial Data Transmission" for more detailed analysis and information.

The XFP MSA also offers useful design tips regarding the construction of the high-speed lines and vias, that will help minimize back-reflections, jitter and maintain signal integrity.

Module Characterization Data

The Avago Technologies XFP has been tested to all the XFI high-speed parameters.

Table 2. XFI Input Characterization Results

Transceiver Electrical Input	Datasheet Min	Datasheet Max	Nominal	Min	Max	Sample Size
Differential Input sensitivity (mV)			40	30	45	5
Differential Input Return Loss (SDD11)			> 14 dB margin	2.0 dB margin	-	3
Common Mode Input Return Loss (SCC11)			> 12 dB margin	2.3 dB margin	-	3

Table 3. XFI Output Characterization Results

Transceiver Electrical Input	Datasheet Min	Datasheet Max	Nominal	Min	Max	Sample Size
Differential Output Amplitude (mV)			652	614	690	30
XFI Fall Time	24 ps		33.2	33.2	35	30
XFI Rise Time	24 ps		35.1	33.6	36.9	30
Common Mode Output Return Loss (SCC22)			> 12 dB margin	2.0 dB margin	-	3
Differential Output Return Loss (SDD22)			> 19 dB margin	1.6 dB margin	-	3
XFI Mask (%)	0		24	17	35	5

4.2. Power Supply Filtering

Description

The XFP module requires the presence of a Host supplied power supply filtering scheme to reduce noise present in the power supply rails to the XFP transceiver.

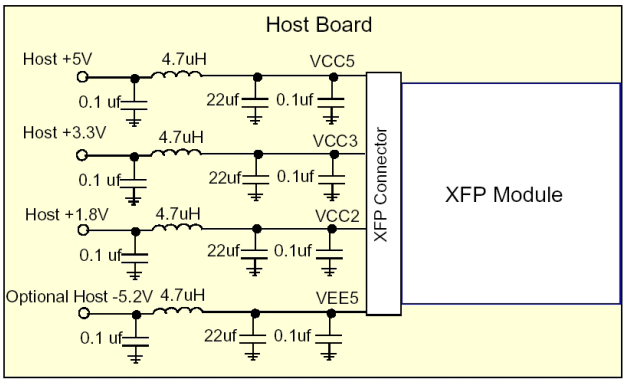

Figure 3. XFP MSA Filtering Scheme (courtesy : XFP MSA Association)

Design Tips

Avago recommends that the system designer use the power supply filter recommended by the XFP MSA.

Module Characterization Data

Module characterization data shows that, in the absence of any filtering and when applied with MSA required power noise in the frequency range of 3kHz to 10MHz, the sensitivity of the XFP receiver degrades by less than 2dB.

4.3. EMI considerations

Design Tips

4.3.1. Gasketing

While designing for EMC considerations, it is recommended that the customer use both the front and rear EMI gaskets as called out in the XFP MSA.

The front gasket acts as an EMC seal that sits between the Bezel and the front of the XFP cage.

The rear EMI gaskets are provided along with the XFP cage to prevent any emissions from escaping the rear of the transceiver or the XFI connector.

4.3.2. Layout Considerations

For XFI channels where the transceiver and the Avago Technologies XFPs are close to each other, radiations from the traces will be minimal and contribute very little to the overall EMI of the system. In these cases, the use of standard FR-4 micro-strip lines with high losses becomes feasible.

For XFI channels that are much longer, the use of stripline interconnects incorporating low loss FR-4 material may be required. It is also important to follow the essential rules of via design, including (a) appropriate clearances and (b) back-drilling to reduce via stub lengths.

Module Characterization Data

The Avago 850nm XFP transceiver shows a nominal of 15dB margin at 5.1GHz and 7dB margin at 15.4GHz to the FCC Class B specifications for radiated emissions. The tests for radiated emissions were carried out in a GTEM test cell.

4.4. Low-speed signaling

Description

The XFP provides 7 low-speed signals that are used for reporting status as well as a means for the host board to control the XFP.

- Mod_NR
- Mod_DeSel
- Interrupt
- TX_DIS
- Mod_ABS
- RX_LOS
- P_Down/RST

Design Tips

All the 7 pins are LVTTL compatible (working on a nominal supply of 3.3V). Please ensure that the LVTTL output pins — Mod_ABS, Mod_NR, Rx_LOS, Interrupt pins are pulled up to Vcc on board using a resistor between 4.7k-10k ohms.

Module Characterization Data

Parameter	Timing at Room Temp
Tx ON	20 us
Tx OFF	1 us
Rx LOS Assert	30 us
Rx LOS Negate	33 us

4.5. Optical Link Guidelines

The link length that the Avago AFBR-720XPDZ transceiver can be used for is dependent upon the fiber type used. For 10 Gigabit Ethernet traffic, the maximum link length specified in the IEEE802.3ae standard is 300m with OM3 fiber, 82m with OM2 fiber and 33m with OM1 fiber.

4.6. 2-wire Interface Design & Usage Guidelines

The Avago Technologies XFP module performs all the Read/Write functional capabilities outlined in the MSA. This includes:

- Current Address Read
- Random Read
- Multiple Read
- 4-byte Sequential Write

The XFP module always operates in a 'slave' mode and hence needs a master that can provide a clock for serial communication. Please note that the XFP module is allowed to hold the clock low for up to 500 us before continuing to execute a read or write command issued by the master.

Figure 4 below shows the memory map of the XFP module.

The lower 128 bytes of the EEPROM contain, among other things:

- Thresholds for Alarms & Warnings
- Digital Diagnostic Information
- Interrupts and flags
- Control/Status bits
- Page Select byte

Module Characterization Data

Table 4 shows a snapshot of the XFP software timing characteristics.

Table 4. XFP Software Timing Characteristics

Parameter (2-wire)	AFBR-720XPDZ	MSA values
TX_Disable assert time	< 1 ms	< 100 ms
TX_Disable deassert time	< 50 ms	< 100 ms
P_Down assert time	< 1 ms	< 100 ms
P_Down deassert time	< 110 ms	< 300 ms
RX_LOS assert time	< 1 ms	< 100 ms
RX_LOS deassert time	< 10 ms	< 100 ms
MOD_NR assert time	< 2 ms	< 100 ms
MOD_NR deassert time	< 5 ms	< 100 ms
Analog parameter data ready	< 200 ms	< 1000 ms

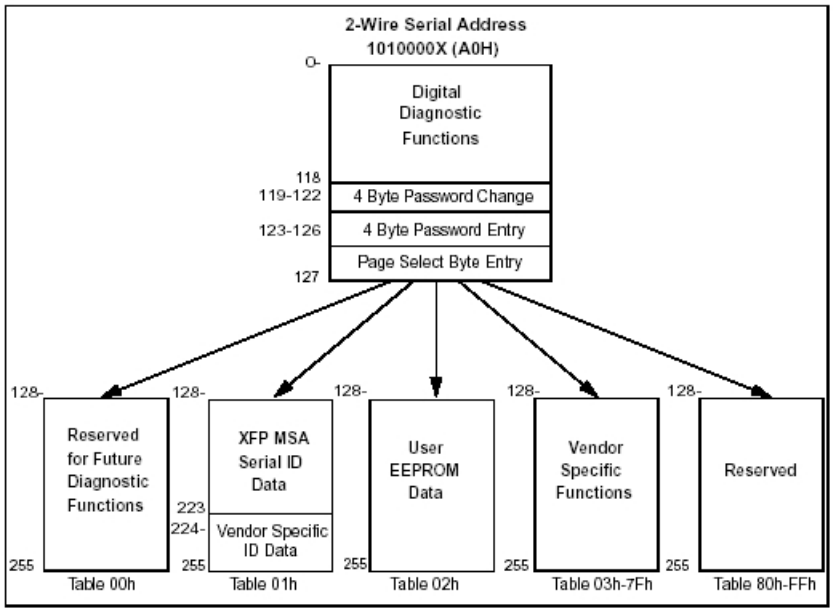

Figure 4. XFP EEPROM Content Map (courtesy: XFP MSA Association)

4.7. Mechanical Design Guidelines

The Avago Technologies AFBR-720XPDZ transceiver conforms to the mechanical dimensions of the XFP 10 Gigabit Small Form Factor Pluggable Module MSA specification, revision 4.5, dated August 2005. They also conform to the TIA/EIA-604-10A specification for the LC fiber optic connector (FOCIS 10A).

Mechanical Tests

As required by the XFP MSA Revision 4.5, Avago Technologies has performed interoperability testing with EMI cages from several XFP cage vendors. For more information on interoperability testing data, please contact your local Avago Technologies Field Sales Engineer.

Avago Technologies has also performed several tests of the optical connector system to ensure robust design and reliability. Several tests are based on Telcordia GR-326, which is a single-mode connector specification, but components of it have been adopted for transceiver testing.

4.8. Thermal Design Guidelines

Avago Technologies specifies an XFP module case temperature range of 0°C to 70°C, measured on the top surface of the module, and guarantees performance within this temperature range. The application environment should be designed (module density, heatsink size, air flow rate, flow bypass, upstream components, PCB conductivity, etc.) to ensure the case temperature does not exceed this requirement.

To facilitate design, a FloTherm thermal model is available for the XFP transceiver.

Table 5. EMI Cage Mechanical Testing Results

TEST	SPECIFICATIONS	Avago PERFORMANCE
Transceiver Retention	Axial pull on module in cage with force gauge.XFP MSA Specification of 90 N minimum.	Tested > 90 N.
Transceiver Insertion/ Extraction Force	Insert/remove module with force gauge from known cage vendors. XFP MSA specification - insertion: 40 N, extraction: 30N.	Insertion < 35N Extraction < 27N

Table 6. Optical Mechanical Testing Results

TEST	SPECIFICATIONS	Avago PERFORMANCE
Fiber Connector Side-Load	Based on Telcordia GR-326 Rev 3, Sect. 4.4.3.4 Proof Test. <0.5 dB optical power loss increase. 20N (5lbf), N-S-E-W loading with duplex connector substitute. Check optical power before & after loading. Test at both initial and retest with 168H 85C/85RH pre-conditioning. Tests structural strength of module/optics.	Max 0.17 dB variation during side load after 85/85.
Fiber Connector Retention	Based on Telcordia GR-326 Rev 3, Sect. 4.4.3.4 Proof Test. 68N (15 lbf) axial pull on fiber, unpowered. Tests structural strength of module/retention of cable.	Tested > 68 N.
Transmission Under Applied Load - Axial	Based on Bellcore GR-326 Rev 3, Sect. 4.4.3.5. < 0.5 dB optical power loss increase during load. 4.5 N (1.125 lbf) axial pull on Tx (simplex) fiber.	0.03 dB max attenuation under load.

5. XFP Testing Guidelines

5.1. AFBR-720XPDZ Evaluation Board

The HFCT-5014 evaluation board can be used to test the Avago Technologies XFP transceivers for a variety of performance characteristics, including optical, electrical, low-speed hardware timings as well as 2-wire performance.

5.2. XFP Transmitter Eye Mask Measurement

Avago Technologies recommends customers using the Agilent 86105C optical plug-in to perform mask margin measurements on the Avago Technologies XFP transceivers.

The optical power at the input of the DCA should be at least above –4 dBm in order to avoid too a big impact of the plug in noise on the eye diagram measurement.

It is also important to configure the plug-in for the appropriate mask alignment method. The Eye Boundary method is the recommended way of aligning the Tx eye to the mask.

Vertical mask alignment using 0 and 1 level determined from the central 20% of the eye diagram (i.e. Eye Boundary) has gained wide industry acceptance. The 10 GB Ethernet standard (802.3ae-2002) reference OFSTP-4A (TIA/EIA-526-4A), which specifies this alignment technique.

Proper triggering is also required for reliable measurement of the eye diagram. The Agilent 83495A optical plug in with clock recovery could be used in conjunction with the 86105C for optimal performance.

In case the 83495A is not available at the customer's lab, triggering directly from the pattern generator 10 GHz clock is recommended (high speed triggering option on the DCA mainframe is required.

Additional information on using the 86100A for eye diagram measurements can be found in the application note, "Characterizing High Speed Optical Transmitters: Compliance Testing with the Agilent Technologies 86100A Infiniium DCA", which is available on the Agilent Technologies Web Site:

http://www.agilent .com

5.3. XFP Stressed Eye Sensitivity

The IEEE 802.3ae Stressed Receiver Sensitivity test is one of the normative requirements for 10G optical receivers. The Stressed Receiver Sensitivity for AFBR-720XPDZ was measured using Circadiant A3301 Optical Standards Test Controller and Circadiant A3318 850nm/Electrical OST interface.

Results

5 Avago Technologies XFP modules were tested for Stressed Receiver Sensitivity performance using the set-up described above. The results are shown in table 7 below:

Table 7. Avago XFP Stressed Receiver Test Results

	Temp [0C]		Temp [25C]	Temp [70C]		
No.	Vnom-5% OMA [dBm]	Vnom+5% OMA [dBm]	Vnom OMA [dBm]	Vnom-5% OMA [dBm]	nom+5% OMA [dBm]	Min Margin dB
1	-12.23	-12.13	-12.08	-11.80	-11.74	4.24
2	-12.02	-12.05	-11.77	-11.55	-11.61	4.11
3	-12.07	-12.26	-12.16	-11.63	-12.02	4.13
4	-12.33	-12.29	-12.32	-11.73	-11.73	4.23
5	-12.16	-12.16	-11.96	-11.75	-11.63	4.13

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